BUFFER INTERLACE CONTROLLER

an option for the

Varian Data Machines

Computer Systems

Specifications Subject to Change Without Notice

varian data machines/a varian subsidiary
printed in USA

98 A 9902 114

NOVEMBER 1972

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INTRODUCTION

1.1 GENERAL DESCRIPTION

The buffer Interlace Controller (BIC) is a special-purpose hardware option for use with Varian computer systems. The BIC contains two address registers, a sequence control unit, and necessary hardware interface (see figure 1-1).

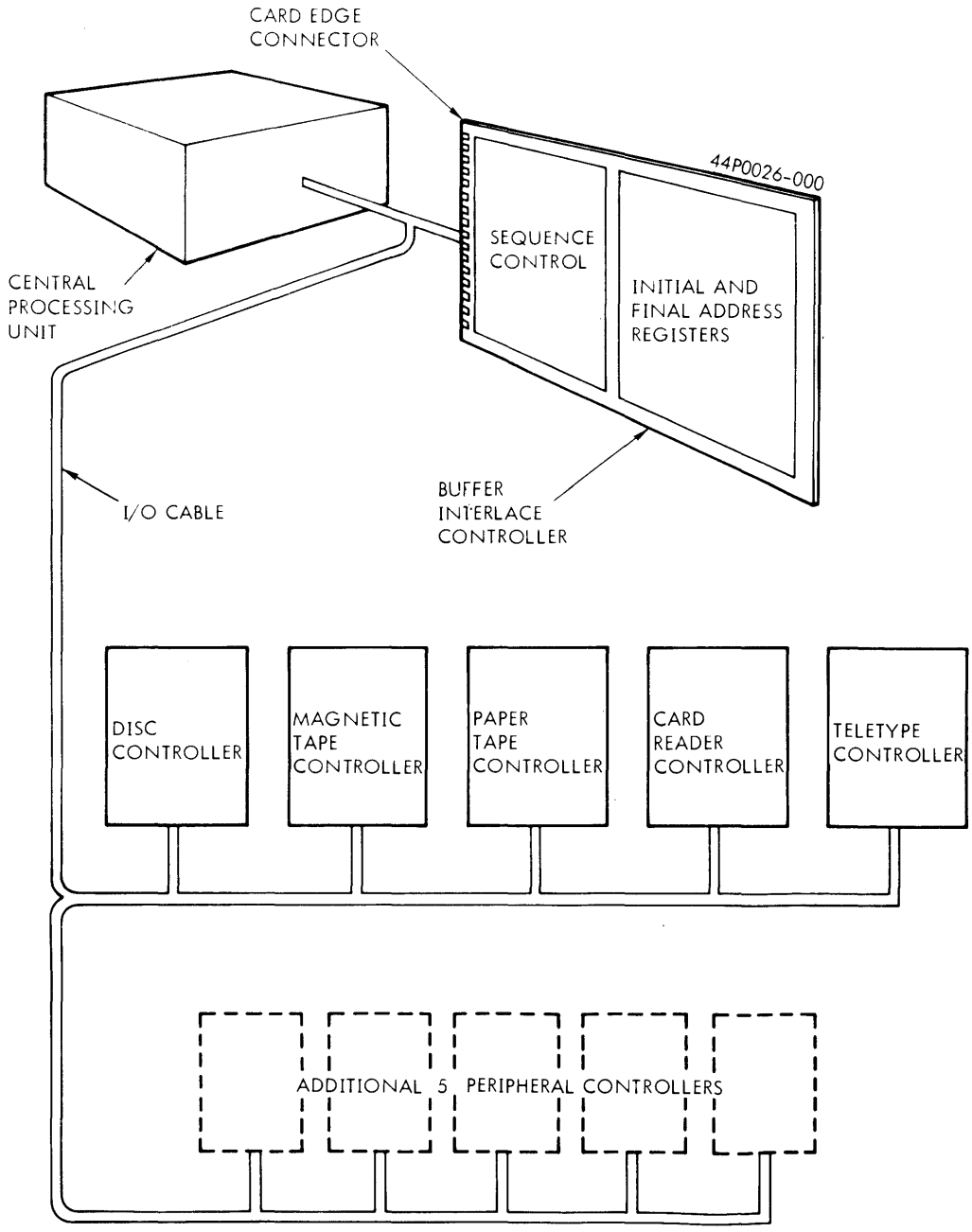

Figure 1-1 Configuration with BIC

This manual explains and illustrates the BIC in a 620 system. Where necessary to explain the BIC in conjunction with the Varian 73, the V73 handbook is referenced.

The function of the BIC is to free the central processing unit (CPU) to perform other program functions during block word transfers. To do this, the BIC controls data transfers (16- or 18-bit words) between memory and peripheral controllers. These transfers occur at a maximum rate of 382,720 words per second; the typical transfer rate without BIC is 56,604 words per second.

The BIC is contained on a single printed circuit card utilizing integrated circuit (IC) components. The card plugs into a 620 I/O Expansion Chassis (figure 1-2). Reference Varian 73 Handbook for BIC installation.

1.2 FUNCTIONAL DESCRIPTION

The BIC is functionally divided into two circuits: address registers and sequence control. A functional description of these circuits is provided in the following paragraphs.

1.2.1 Address Registers

The two address registers contain the memory locations of output or input data, depending on the command. The initial (I) register stores the address of the first input or output word. This register is incremented during each data word transfer. When the block transfer is complete, the I register contains the address plus one of the last data word to be transferred.

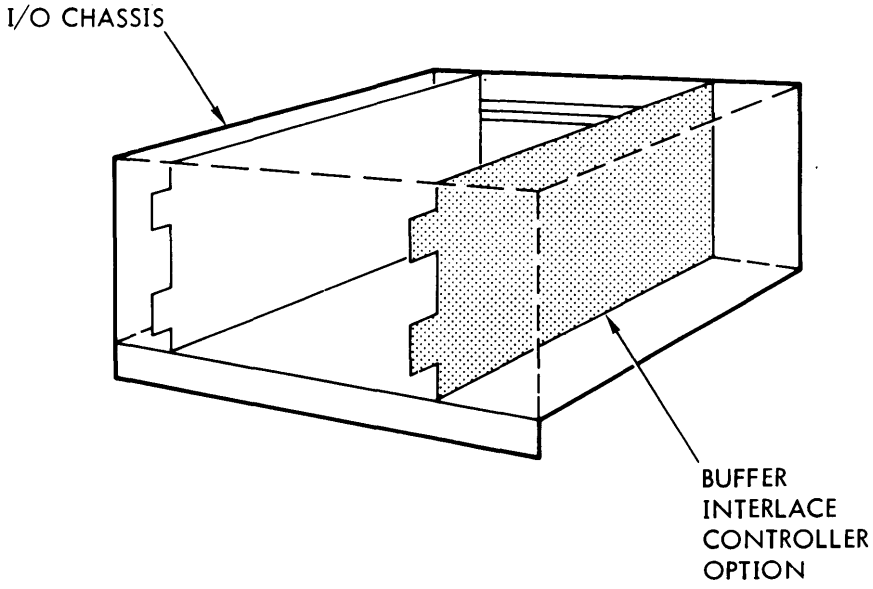

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Figure 1-2. BIC Option Installation

Up to ten peripheral controllers can be connected to one BIC. Using standard I/O device addressing, a computer system can include up to four BICs.

As part of an expansion chassis configuration, the BIC is considered an I/O controller. Priorities for optional controllers having trap or interrupt capabilities are established by the order of their placement on the I/O bus. The BIC is a system priority device; however, the peripheral devices connected to it have no priority of their own.

NOTE

In this manual, numbers beginning with a digit other than zero are decimal numbers and numbers with a leading zero are octal.

The final (F) register stores the address of the last word to be transferred. Unless the peripheral device is abnormally stopped, the address in the F register will be one less than the address in the I register when the block transfer is complete. When the I and F registers reach comparison, the block word transfer is complete.

1.2.2 Sequence Control

The sequence control circuit generates the control signals which coordinate address and data transfer between the CPU and the BIC and peripheral device controllers. The data are not routed through the BIC but are directly transferred between the device controller and memory.

Under program control, the CPU senses that the BIC is not busy and prepares the BIC to receive the initial and final data addresses. The CPU then senses that the selected peripheral device is not busy and loads the I and F registers. The BIC is then activated and the peripheral controller is started. The BIC then assumes control of the data transmission, allowing computer operational registers to be used by the program for other functions.

Data transfer is accomplished between memory and the device controller via the E bus in the I/O cable. The BIC counts the words transferred and, when the data block transfer is complete, disconnects the device controller and assumes a not busy state. Data transfer may also be terminated upon request from the peripheral device controller.

1.3 SPECIFICATIONS

The physical, electrical, and operational specifications of the BIC are listed in table 1-1.

Table 1-1. BIC Specifications

Parameter	Description
Organization	Contains input receivers and output drivers, two 15-bit address registers and a sequence control circuit
Control capability	Up to ten device controllers
I/O capability	Two external control (EXC) commands Eleven transfer commands Two sense (SEN) commands
I/O transfer rate	Synchronized to peripheral device rate; maximum 382,720 words per second
I/O signal limits (rise/fall)	Minimum 10 nanoseconds; maximum 100 nanoseconds
Logic levels	
To the I/O bus	Negative logic Logic 1 (low): 0.0 to +0.5V dc Logic 0 (high): +2.5 to +3.7V dc
Internal	Positive logic Logic 1 (high): +2.5 to +5.0V dc Logic 0 (low): 0.0 to 0.5V dc
Size	One 7-3/4-inch-by-12-inch printed circuit card
Interconnection*	Interfaces with I/O cable through backplane connector; connects to peripheral controllers through B cable
Connectors*	One 122-terminal card-edge connector (mates with female connector at back-plane) and two 44-terminal card-edge connectors (mate with 44-terminal connector on B cable)
Input power requirement	+5V dc at 0.6A
Operational environment	0 to 50 degrees C; 10 to 90 percent relative humidity

* Varian 73 Handbook

SECTION 2
OPERATION

2.1 GENERAL

There are no operating controls or indicators on the BIC. This section contains programming considerations, theory of operation, and mnemonic definitions.

2.2 PROGRAMMING CONSIDERATIONS

The user writes the programs that use the BIC. When preparing a program for use with the BIC, the programmer first initializes then senses the status of the BIC and the selected peripheral controller. After a not-busy response is received from both the BIC and the peripheral controller, the BIC address registers are loaded with the initial and final memory addresses of the block of data to be transferred, a BIC activate enable instruction is placed on the I/O cable, and the transfer is started. Although the program requires loops for use with sense instructions and to handle abnormal conditions, transfer of the data block is accomplished by the BIC without further program instructions.

2.3 DESCRIPTION OF COMMANDS

The BIC responds to the commands listed in table 2-1. Two device addresses are assigned to each BIC to differentiate functions directed by the I/O instruction. Addresses 020 through 027 are reserved for BICs. Address/instruction codes in table 2-1 are for the first BIC in a system. If additional BICs are installed, the addresses shown should be incremented by two for each additional BIC (i.e., second BIC addresses should be 022 and 023).

2.4 SAMPLE PROGRAM

Table 2-2 shows a typical service routine for the BIC, a teletype paper tape punch operation under BIC control. Using DAS symbols with corresponding machine language octal codes, the program covers memory locations 01000 through 01034.

Table 2-1. BIC Commands

Mnemonic	Octal Code	Description
	External Control	
EXC 020	100020	Active enable
EXC 021	100021	Initialize
	Transfer	
OAR 020	103120	Load initial register from A
OBR 020	103220	Load initial register from B
OME 020	103020	Load initial register from memory
OAR 021	103121	Load final register from A
OBR 021	103221	Load final register from B
OME 021	103021	Load final register from memory
INA 020	102120	Read initial register into A
INB 020	102220	Read initial register into B
IME 020	102020	Read initial register into memory
CIA 020	102520	Read initial register into cleared A
CIB 020	102620	Read initial register into cleared B
	Sense	
SEN 020	101020	Sense BIC not busy
SEN 021	101021	Sense abnormal device stop

Table 2-2. Typical Service Routine

Memory Location	Octal Code		Label	Operation	Variable Field	Comments
001000				,ORG	,01000	
001000	101020		BIC0	,SEN	,020,BIC1	CK BIC NOT BUSY
001001	001007	R				
001002	100401			,EXC	,0401	INIT TTY
001003	100021			,EXC	,021	INIT BIC
001004	005000			,NOP	,	
001005	001000			,JMP	,*-3	
001006	001002	R				
001007	101101		BIC1	,SEN	,0101, ,BIC2	CK TTY WRITE READY
001010	001014	R				
001011	005000			,NOP	,	
001012	001000			,JMP	,*-3	
001013	001007	R				
001014	103120		BIC2	,OAR	,020	SET BIC I REG
001015	103221			,OBR	,021	SET BIC F REG
001016	100020			,EXC	,020	ACTIVATE BIC
001017	100101			,EXC	,0101	CONNECT WRITE REG
001020	101020			,SEN	,020,BIC3	CK BIC NOT BUSY
001021	001025	R				
001022	005000			,NOP	,	
001023	001000			,JMP	,*-3	
001024	001020	R				
001025	101021		BIC3	,SEN	,021,BIC5	CK ABN STOP
001026	001032	R				
001027	007400			,ROF	,	
001030	102520		BIC4	,CIA	,020	INPUT BIC I REG
001031	000000			,HLT	,	
001032	007401		BIC5	,SOF	,	SET ABN FLAG
001033	001000			,JMP	,BIC4	
001034	001030	R				
	000000			,END		

Once the program is loaded, the operator must insert the initial punch buffer address into the A register and the final address into the B register for each run. When started, the program will:

a. initialize the BIC and Teletype punch

b. initiate the data transfer

c. read the contents of the BIC initial register into the A register at the completion of the transfer

d. set the overflow indicator if the termination was abnormal

e. halt

The punch buffer must contain only ASCII characters. The first character is 0222 (punch on) and the last is 0224 (punch off).

2.5 THEORY OF OPERATION

The theory of operation is described as a series of sequences that exercise the entire BIC. Refer to logic diagram 95D0020. Three-digit numbers in parentheses indicate the location of circuit elements on the diagram. The first number locates the sheet; the following letter and number indicate the area on that sheet. Figure 2-1 supplies a timing diagram.

Signal levels referred to in the theory of operation are the levels of the signals at their point of origin or their entry into the BIC. Stages of inversion are disregarded for the purpose of clarity. Flip-flop outputs are designated FF set signal and FF reset signal if they are high when the flip-flop is set or reset, respectively.

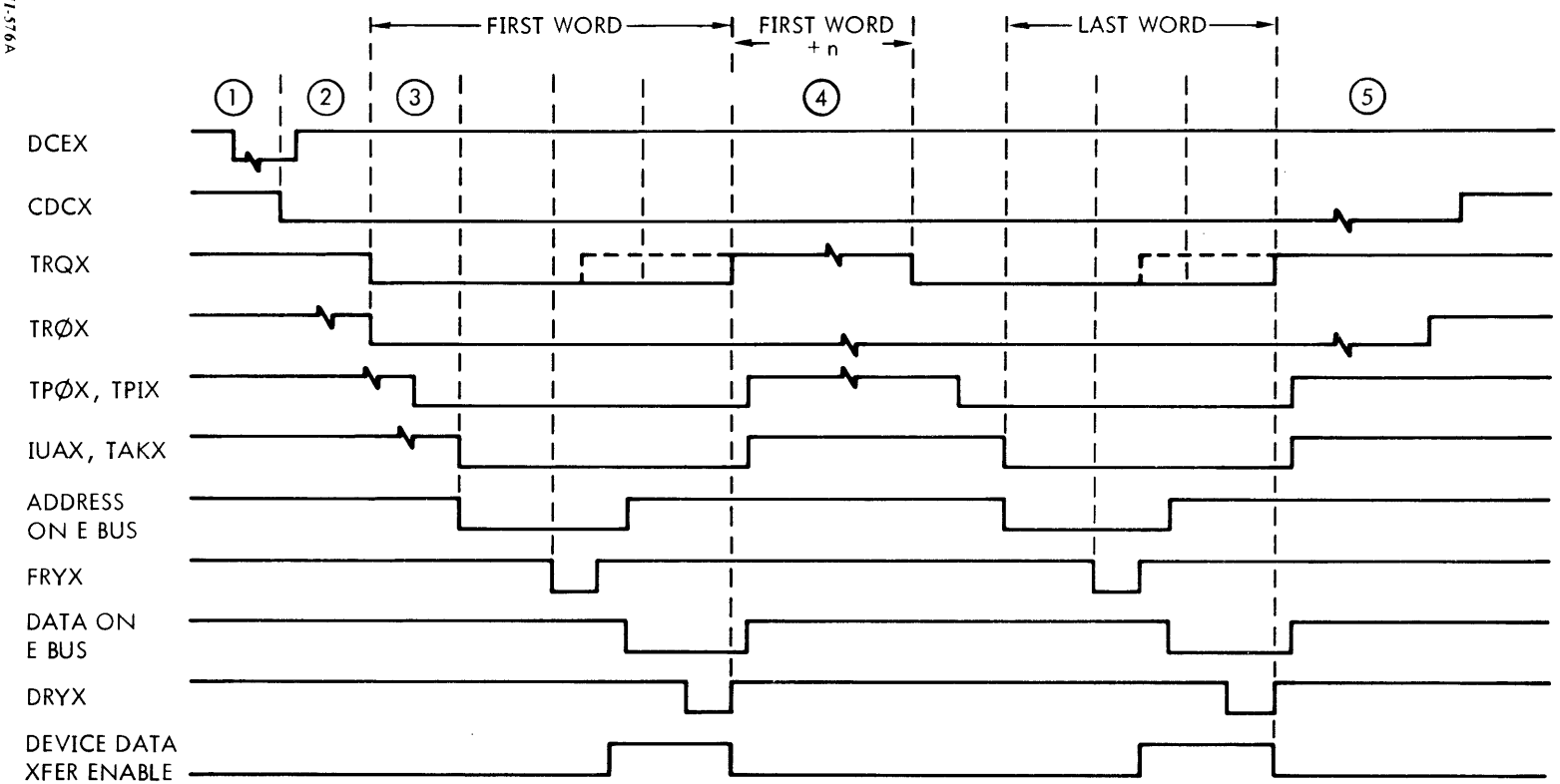


Figure 2-1. BIC Trap Sequence Timing

NOTES:

(1) TIMING REQUIRED TO ISSUE THE COMMAND TO CONNECT THE DEVICE.

(2) TIME REQUIRED FOR DEVICE TO REQUEST FIRST DATA TRANSFER AFTER STARTING.

(3) TIME REQUIRED TO SERVICE CURRENT AND/OR HIGHER PRIORITY REQUESTS FOR I/O ACCESSES.

(4) TO ACHIEVE MAXIMUM RATE OF DATA TRANSFER, SIGNAL TRQX NEED BE LOW FOR ONLY 400 NANOSECONDS.

(5) END OF DATA BLOCK. SIGNAL CDCX MAY REMAIN HIGH BETWEEN BLOCKS.

6 FOR DMA TIMING REFER TO THE APPLICABLE SYSTEM HANDBOOK.

2.5.1 Initial Conditions

The CPU executes the sense BIC not busy command which generates the BIC device address and a function code on the E bus (2D8). The BIC responds with signal SERX low (2D5). The processor then executes an initialize command (2B8) which generates signal INIT low (2A6). Signal INIT low, which may also be enabled by signal SYRT low, sets flip-flop DSTX and resets the following flip-flops: ACEX, BCAX, ADSX, TPDX, TCOX, TAOX, LIXX, LFXX, RIXX, and IFMX.

FF set signal TCOX low generates signal TAKX low (1C5) which resets flip-flop EBDX. FF set signal EBDX low generates signal EBD1 high (1B2). FF set signal LIXX high generates signal LIRX high (2C5). FF set signal LFXX low generates signal LFRX low (2B5). Signals EBD1 high, LIRX high, and LFRX low enable the I and F registers to be loaded from the E bus with the initial and final addresses of the block of data to be transferred.

2.5.2 Device Selection

The CPU executes an active enable command which sets flip-flop ACEX (2C4). The high ACEX+ is gated with high CDCX- and ADSX- signals to provide a low DCEX-B which is sent to all peripheral controllers connected to the BIC. The processor then executes a command to select a peripheral device. This command with signal DCEX low connects the selected device to the BIC and starts the device.

The connected peripheral device controller sends signals CDCX low (2D4) and TROX (1D5) to the BIC. Signal CDCX low causes signal DCEX to go high, disabling the selection of any other peripheral device controllers. A low CDCX- also causes SERX-I to go high and INTX- to go low. A high SERX-I indicates that the BIC is busy; a low INTX- initiates an interrupt request. The state of signal TROX determines whether data will be transferred to or from memory; this signals partially enables either signal TPIX low (1D3) or TOPX low (1C3). A low CDCX-B and a high ACEX+ sets flip-flop BCAX.

When the connected device controller is ready for the data transfer, it sends signal TRQX low (1D8) to the BIC. FF set signal BCAX high and signal TROX low set flip-flop TPDX (1D5). FF reset signal TPDX low and signal IUCX low set flip-flop TCOX. FF set signal TCOX high and signal PRMX low complete the enabling of either signal TPIX low (1D3) or TPOX low (1C3) to the processor.

2.5.3 Data Address

When the CPU is ready for the data transfer, it sends signal IUAX low (2C8) to the BIC. Signal IUAX low generates signal TAKX high (1C5) which is sent to the peripheral device to initiate the transfer. The BIC then enables signal OIRX high (2B5) which gates the memory address that was in the I register onto the E bus. The connected peripheral device controller is thus enabled. Pulse signal FRYX terminates the address phase of the BIC and sets either flip-flop DTIX or flip-flop DTOX inside the selected peripheral controller. The trailing edge of signal FRYX causes the I register to be incremented to the next memory address.

2.5.4 Data Transfer

The data transfer may be an output from or an input to the CPU. For output, the processor places the data on the E bus, and the data is strobed into the peripheral device controller by pulse signal DRYX. For input, the peripheral device controller places the data on the E bus at pulse signal FRYX and removes the data at signal DRYX. BIC signal TAKX remains high until the end of the transfer when signal IUAX goes low.

2.5.5 Transfer Termination

Normally when the contents of the I and F registers become equal, the comparator circuit generates signal IEFX low (3C2). This signal sets flip-flop IFMX (2A6). FF set signal IFMX high generates signal IEF2 low which resets flip-flop BCAX (2C3). FF set signal BCAX low sets flip-flop DSTX (1B5). FF set signal DSTX high sets flip-flop DESX (1B4). The output of this flip-flop is inverted and sent to the peripheral device controller. The peripheral controller then causes signal CDCX (2D4) to go high, and the BIC assumes the not busy state. The transfer of data is thus terminated.

Abnormally, the peripheral device terminates the transfer without regard to the contents of the I and F registers. The peripheral device controller generates signal BCDX low (2A5) which sets flip-flop ADSX (2B3). FF set signal ADSX high generates signal IEF2 low (2C4) which indirectly causes signal DESX to be sent to the peripheral device controller. The peripheral device controller then causes signal CDCX (2D4) to go high, and the BIC assumes the not busy state. The transfer of data is thus terminated. After an abnormal device stop, the CPU can read the contents of the I register to determine the number of words that were transferred.

An abnormal device stop can occur as a result of any of the following situations: the length of the data block is unknown, and the device has detected the end of the data; the peripheral device controller has detected an invalid operation of the device; the CPU has issued a command to stop the operation of the peripheral device.

2.6 MNEMONICS

The mnemonics used in the BIC are listed alphabetically in table 2-3. A brief description of each signal's function is given as well as the proper signal name.

Table 2-3. Mnemonic Definitions

Mnemonic	Name	Function
ACEX	Activate enable	Stores activation of BIC
ADSX	Abnormal device stop	Stores end of data from peripheral controller
BCAX	Buffer controller activate	Stores the activation of the BIC and the peripheral device controller
BCDX	Buffer controller deactivate	Initiates termination of data transfer by the peripheral device controller
CDCX	Controller device connected	Indicates that the peripheral device is connected
CIRX	Clear I register	Resets the flip-flops in the I register
CLEX	Clock enable	Enables incrementation of the I register
CLEZ	Clock enable	Enables end of data sequence
DCEX	Device connect enable	Enables selection of a peripheral device
DESX	Device stop	Stores the requirement to stop the peripheral device
DRYX	Data ready	Indicates the E bus contains a word of data
DSTX	Device stop permit	Stores the end of the data transfer
EBD1	E bus drive 1	Enables loading of the F register
EBDX	E bus drive	Stores the need to initially load the F register from the E bus
EBii	E bus bit	Data or address to be transferred
EBil	E bus bit inverted	Part of the BIC device address
FRYX	Function ready	Indicates the E bus contains an address
FiiX	F register flip-flop	Stores final data address bit
IEFX	Initial equals final	Indicates content of the I register is equal to content of F register
IEF2	Initial equals final 2	Initiates deactivation of the BIC and the peripheral device controller
IFMX	Initial equals final memory	Stores the incrementation of the I register to the value of the F register
INIT	Initialize	Sets and resets BIC flip-flops to their initial condition

Table 2-3. Mnemonic Definitions *(continued)*

Mnemonic	Name	Function
INTX	Interrupt	Requests interrupt
IUAX	Interrupt acknowledge	Enables servicing of BIC-connected peripheral device controllers
IUCX	Interrupt clock	Provides timing for servicing BIC
IiiX	I register flip-flop	Stores initial and subsequent data address bits
LFRX	Load F register	Gates E bus address into F register
LFXX	Load F register permit	Stores command to load F register
LIRX	Load I register	Gates E bus address into I register
LIXX	Load I register permit	Stores command to load I register
PRMX	Priority input	Gives priority to BIC
PRNX	Priority output	Passes priority to next in line after BIC is serviced
OIRX	Output I register	Gates contents of I register onto E bus
RIXX	Read I register	Stores requirement of central processor to know contents of I register
SERX	Sense response	Indicates whether the BIC is busy
SYRT	System reset	Generates initialize signal when SYSTEM RESET switch is pressed
TAKX	Transfer acknowledge	Indicates that requirements for data transfer have been met
TAOX	Trap address out	Stores the placing of the data address on the E bus
TCOX	Trap command	Stores the need for a trap requested by the BIC
TPDX	Trap detect	Stores the peripheral device request for a trap when data is to be transferred
TPIX	Trap input	Indicates that the BIC is ready to transfer data to memory
TPOX	Trap output	Indicates that the BIC is ready to transfer data from memory
TROX	Transfer out	Indicates the direction (in or out) of data transfer
TRQX	Transfer request	Indicates that the peripheral device is ready for the data transfer

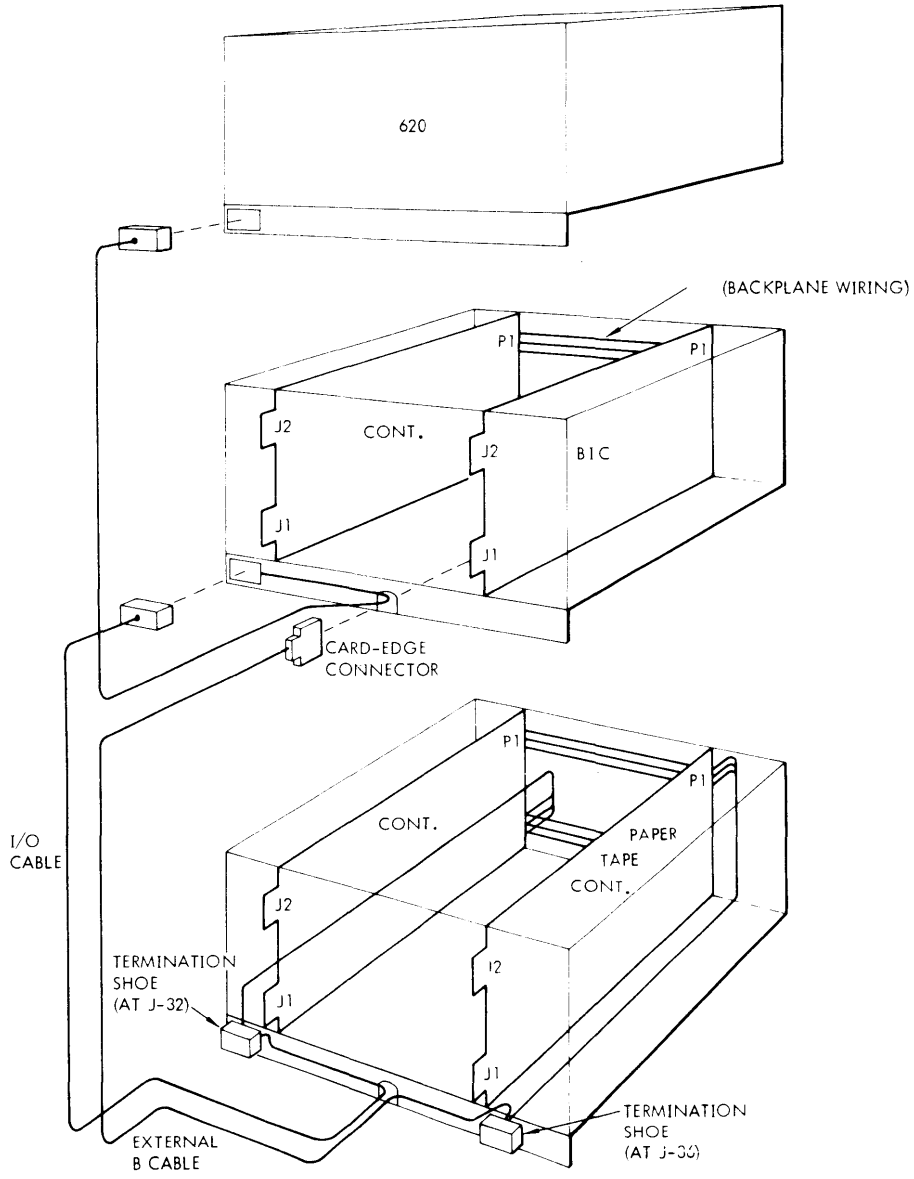
SECTION 3
INSTALLATION

3.1 GENERAL

It is recommended that installation of the BIC be performed by Varian Data Machines customer service engineers. Logic diagrams, assembly drawings, and wiring information are provided at the time of purchase.

3.2 REQUIREMENTS

A 620 memory expansion/peripheral controller chassis must be installed in close proximity to the computer and connected to the I/O cable by means of an extender cable. This cable is available in lengths up to 20 feet.



NOTE: B CABLE NOT REQUIRED WHEN BUFFER INTERLACE CONTROLLER IS NOT USED.

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Figure 3-1. Typical External B Cable Installation

3.3 CARD LOCATION AND INSTALLATION*

The BIC is a printed circuit card located in a card slot in the I/O section of the expansion chassis. The I/O section is located in the right half of both rows of the expansion chassis when viewed from the front panel.

Installation of the BIC into its designated card slot is accomplished by inserting the card into the mounting guides with the component side of the card on the installer's left at the rear of the expansion chassis.

Moderate pressure should be applied to seat the 122-pin card-edge connector firmly into the mating connector on the chassis backplane. To prevent damage to the backplane connector or to the nylon guides, care must be taken to ensure that even pressure is applied across the top of the card during insertion. A Titchener 1731 circuit-card puller or equivalent is recommended for circuit card removal.

3.4 INTERCONNECTION*

The BIC is hardwired through the expansion chassis backplane to the I/O cable and peripheral controllers installed in the same expansion chassis. Interconnection with peripherals installed in a different expansion chassis is through an external B cable. This cable is connected to the BIC by a card-edge connector and is hardwired to the second expansion chassis (figure 3-1).

The B cable is fabricated to meet the requirements of each installation. Eight twisted pairs are used in each B cable. To prevent noise generation from reflected signals, each active signal pair must be terminated (figure 3-2).

* Reference Varian 73 System Handbook

When two or more BIC controllers are instailed in the same chassis, the B cable signals are connected only to the controller or controllers with which each BIC communicates; there are no B cable signals between BICs.

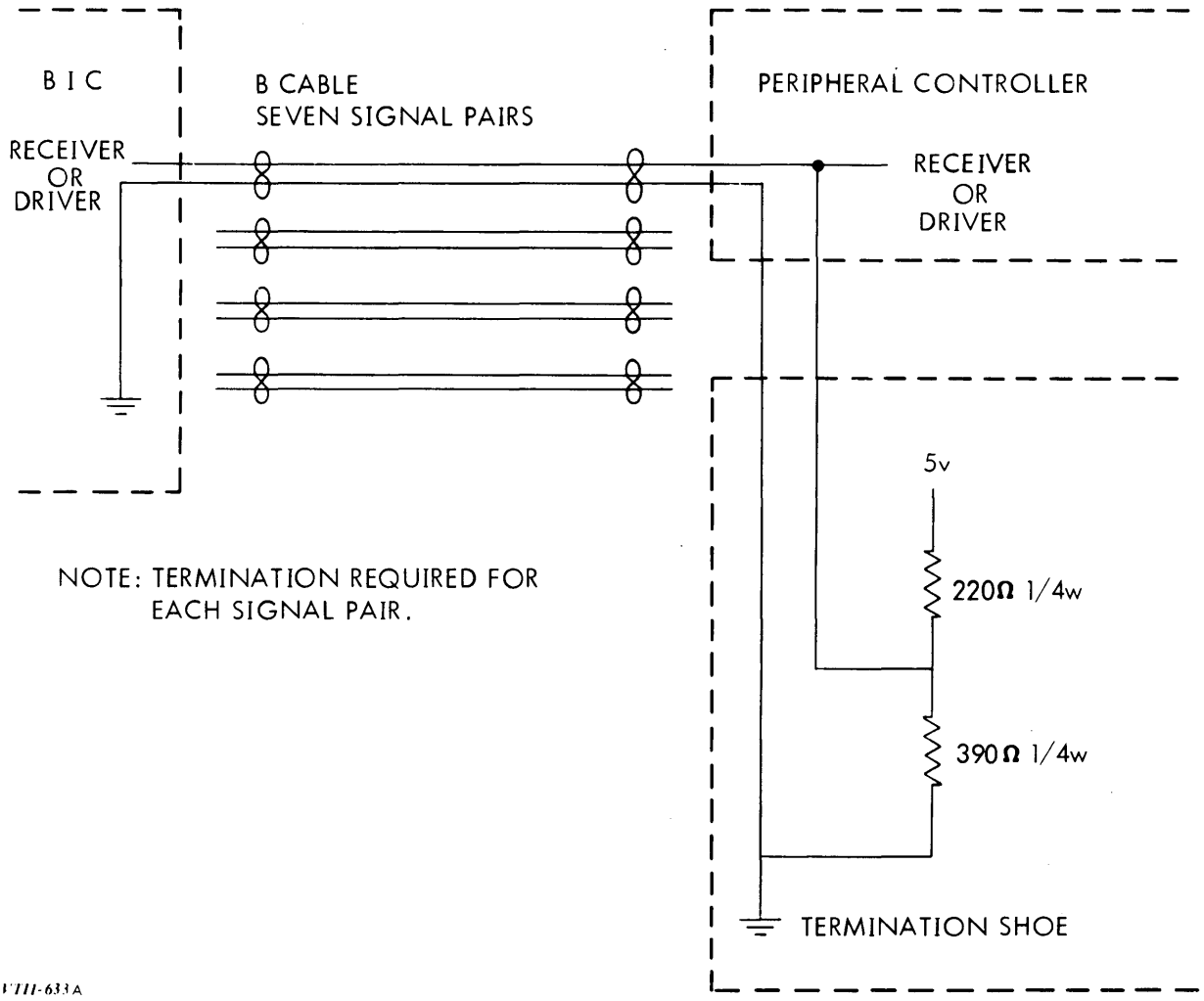


Figure 3-2. Typical Termination for B Cable Pair

SECTION 4
INTERFACE DATA

4.1 GENERAL

All BIC input/output signals utilize receiver/driver stages to buffer internal circuits and external lines. For detailed information concerning interface between the CPU and peripheral controllers connected to the I/O cable, refer to the 620 Interface Reference Manual or Varian 73 Processor Manual.

4.2 INTERFACE SIGNALS*

The BIC interfaces with the computer and peripheral controllers via the control lines listed in table 4-1. A circuit-card connector pin number follows each signal mnemonic (see logic diagram 95D0020, sheet 4). Refer to table 2-3 for definitions of the mnemonics.

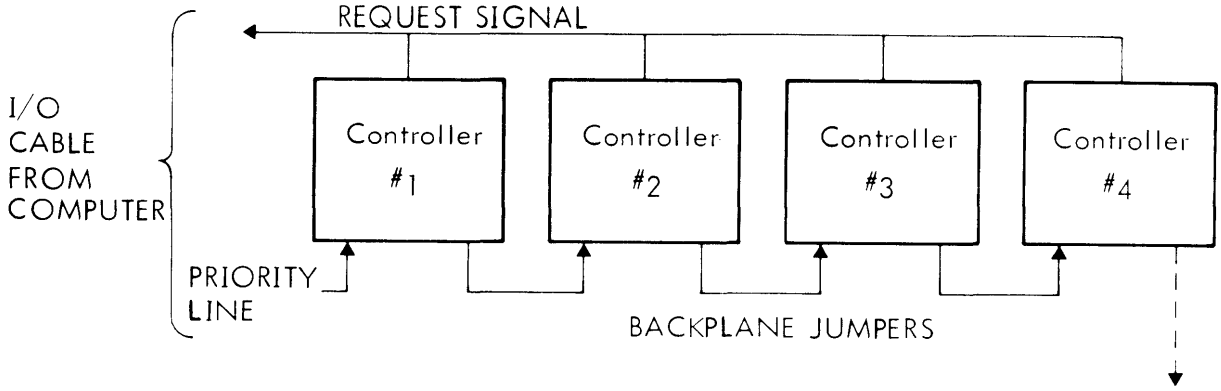
* Reference Varian 73 Handbook and Processor Manual

4.3 PRIORITY ASSIGNMENTS

Peripheral controllers are assigned priorities to ensure that automatic requests such as interrupts and traps will not conflict. Priorities are determined by controller electrical placement on the I/O bus (figures 4-1 and 4-2). Refer to the 620 Interface Reference Manual (document number 98 A 9902 015 or Varian 73 Processor Manual document number 98 A 9906 020) for detailed information.

Table 4-1. BIC Inputs and Outputs

Input		Output	
BCDX-52	EB11-17	DCEX-56	EB09-15
CDCX-54	EB12-18	DESX-60	EB10-16
DRYX-29	EB13-19	EB00-2	EB11-17
EB00-2	EB14-20	EB01-4	EB12-18
EB01-4,65	EB11-68,69	EB02-6	EB13-19
EB02-6,70	EB21-71,72	EB03-8	EB14-20
EB03-8	FRYX-27	EB04-10	PRNX-42
EB04-10	INTX-75	EB05-11	SERX-31
EB05-11	IUAX-44	EB06-12	TAKX-58
EB06-12	IUCX-45	EB07-13	TPIX-33
EB07-13	PRMX-37	EB08-14	TPOX-35
EB08-14	SYRT-43		
EB09-15	TROX-50		
EB10-16	TRQX-49		



NOTE: PR1X-I, PR2X-I, PR3X-I, and PR4X-I in the I/O cable are used to effect connection between the computer and expansion chassis, and are wired to meet system requirements.

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Figure 4-1. Controller Priority - One Expansion Chassis

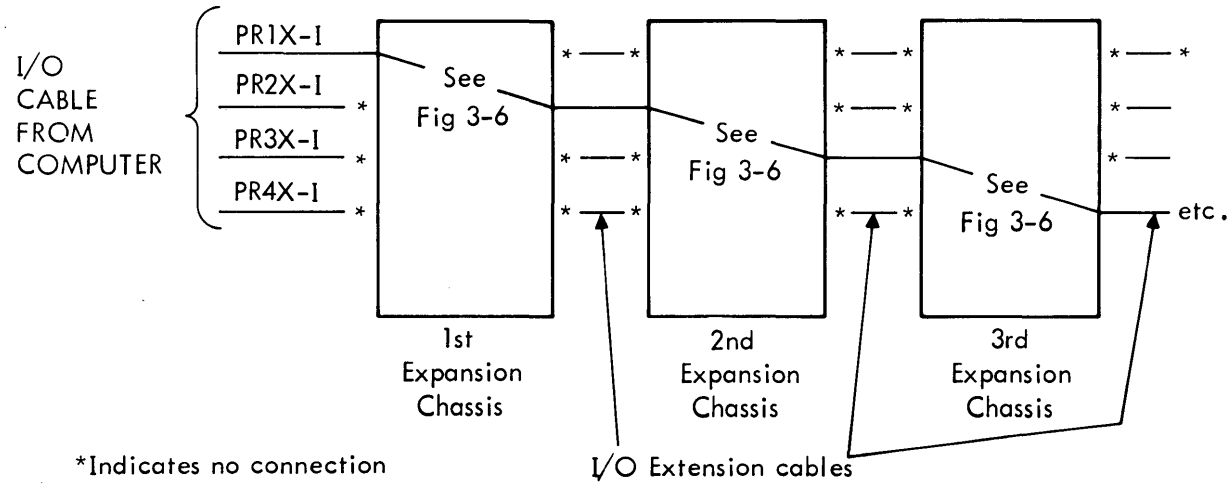

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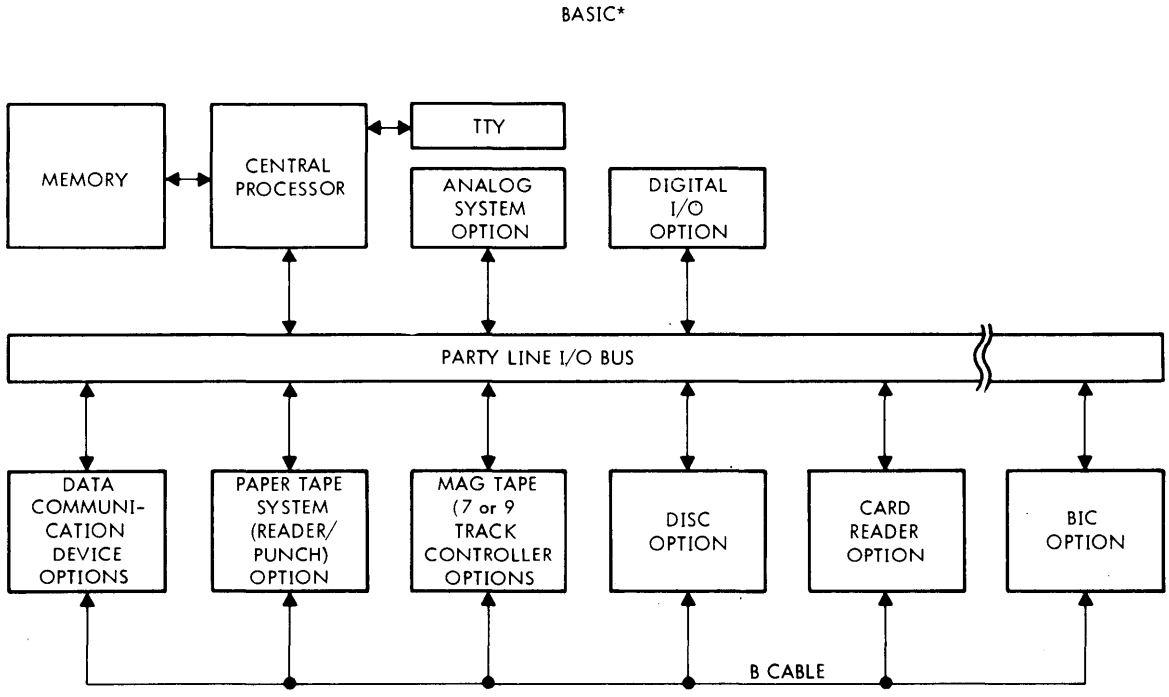
Figure 4-2. Priority Line Connection - Multiple Expansion Chassis

4.4 PERIPHERAL CONTROLLER INTERFACE

A peripheral controller can enable an I/O device to operate under control of either the CPU or the BIC. A device controller connected for BIC control can also function under control of the standard I/O instructions. Figure 4-3 shows a computer system with peripheral device controllers interfaced for operation with and without BIC. Figure 4-4 illustrates BIC/peripheral interconnection; figure 4-5 is typical interface logic.



*PARTY LINE I/O HAS 16/18 BI-DIRECTIONAL ADDRESS/DATA LINES PLUS FIVE CONTROL LINES.

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Figure 4-3. 620 Interface for Peripheral Devices with and without BIC

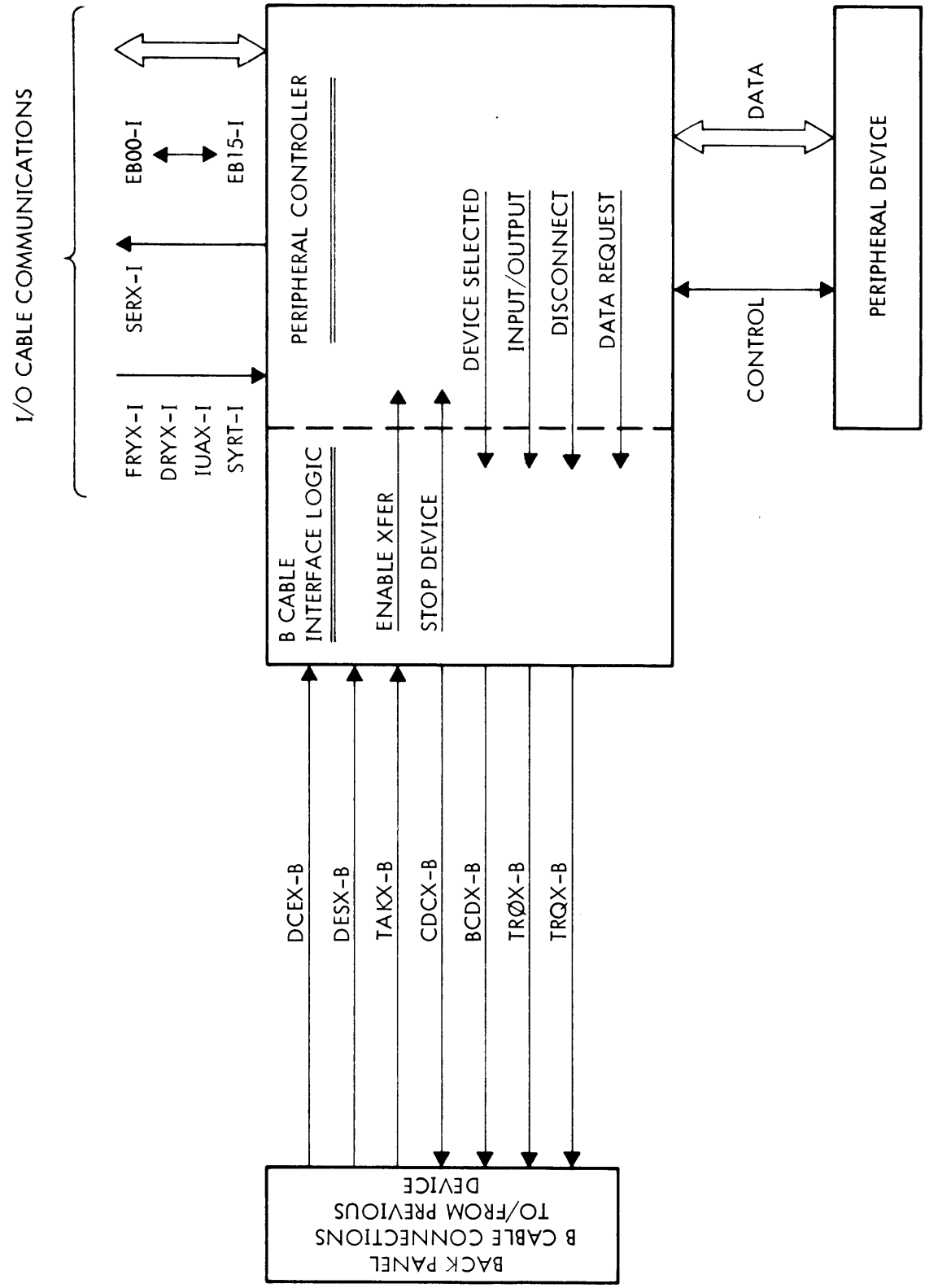

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Figure 4-4. BIC/Peripheral Controller Interface

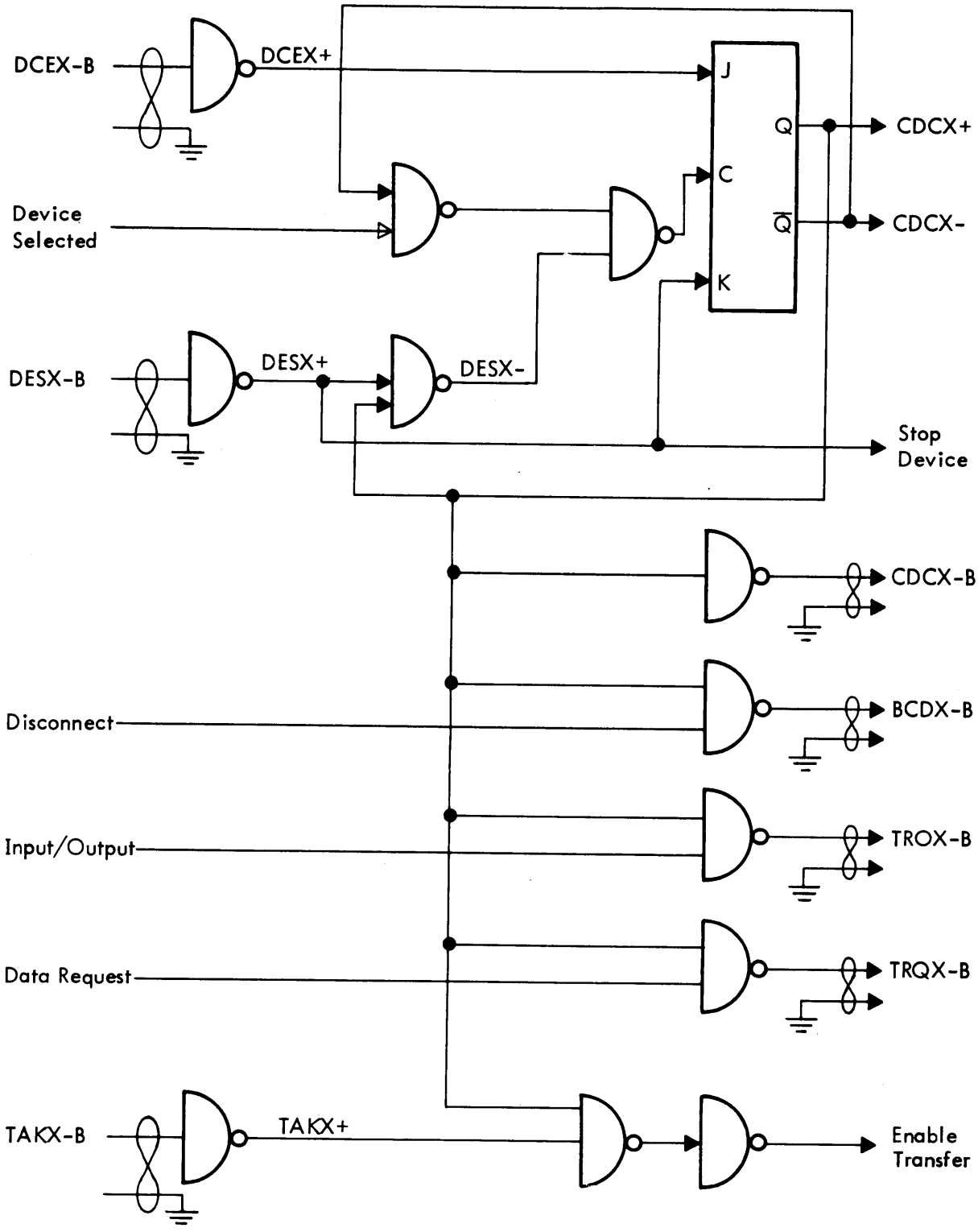

Figure 4-5. Typical B Cable Interface Logic

SECTION 5
MAINTENANCE

5.1 GENERAL

BIC maintenance consists of running test programs, troubleshooting, and making repairs if required. However, if repair is indicated, it is recommended that the entire circuit card be replaced. Troubleshooting is facilitated by familiarization with the operation of the BIC and use of the logic diagram.

5.2 REQUIRED EQUIPMENT

The following is a list of recommended test equipment and tools for the maintenance of the BIC.

a. Oscilloscope, Tektronix type 547

b. Multimeter, Triplett type 630

c. Extender Card, VDM 44D0540-000

5.3 REFERENCE DOCUMENTS

The documents listed below will be useful as aids to understanding and maintaining the BIC.

a. 620 System Reference Manual, 98 A 9902 003

b. 620 Interface Reference Manual, 98 A 9902 015

c. 620 Maintenance Manual, Volume 1, 98 A 9902 055

d. V73 System Handbook 98 A 9906 010

e. V73 Processor Manual Volume 1, 98 A 9906 020

f. Logic diagram, 95D0020

g. Assembly drawing, 44D0026

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CHAPTER/SECTIONS		MOST USEFUL			NEEDS MORE				NEEDS LESS		
		Field Reference	Training	Big Picture Description	Illustration	Detailed Description	Detailed Description	Detailed Description			

2. Please list any errors, omissions, or difficult areas noticed in the manual. _____

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