PERIPHERAL LOGIC

FOR LAST WEEK OF MAINTENANCE COURSES

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varian data machines / a varian subsidiary
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PRIORITY INTERRUPT MODULE

an option for the

Varian Data Machines

Computer Systems

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SECTION 1
GENERAL DESCRIPTION

The Priority Interrupt Module is an I/O option available with Varian 70 series and 620 computer systems. This manual is divided into six sections:

- Features and specifications
- Installation and interconnection
- Operation
- Theory of Operation
- Maintenance
- Mnemonics list

Documents such as logic diagrams, schematics, and parts lists are supplied in a System Maintenance Manual. This manual is assembled when the equipment is shipped, and reflects the configuration of a specific system.

The following list contains the part numbers of other manuals pertinent to the Varian 70 series computers (the x at the end of each document number is the revision number and can be any digit 0 through 9):

V72 System Handbook	98 A 9906 20x
V73 System Handbook	98 A 9906 01x
V74 System Handbook	98 A 9906 21x
V75 System Supplement	98 A 9906 22x
Processor Manual	98 A 9906 02x
8K Core Memory Manual	98 A 9906 03x
8K Semiconductor Memory Manual	98 A 9906 04x
16K Core Memory Manual (1200 ns)	98 A 9906 24x
16K Core Memory Manual (990 ns)	98 A 9906 25x
Option Board Manual	98 A 9906 05x
Power Supply (Universal) Manual	98 A 9906 06x
V72 Power Supply Manual	98 A 9906 12x
Microprogramming Guide	98 A 9906 07x
Writable Control Store Manual	98 A 9906 08x
Memory Map Manual	98 A 9906 10x
MAINTAIN III Manual	98 A 9952 07x

The priority interrupt module (PIM) provides for the orderly servicing of peripheral-initiated interrupts of a program in progress. It does so by:

a. Establishing up to eight levels of interrupt priority for selected peripheral controllers.

b. Storing interrupt requests originated by associated peripheral controllers and placing the requests on the I/O bus in the order of the established priority.

In effect, the PIM organizes a " priority-within-a-priority" system. Peripheral controllers that cannot normally initiate an interrupt because of their inability to generate memory addresses can do so when connected to the PIM. PIM-controlled priority assignments are prewired at the factory to user specifications.

Table 1-1 lists the PIM specifications.

Table 1-1. PIM Specifications

Parameter	Description
Organization	Contains line synchronization, and mask registers; an interrupt address generator; priority and control logic; and line drivers and receivers
Control Capability	Establishes and implements eight levels of interrupt priority (user-assigned) for system peripheral controllers.
I/O Capability	Five external control and three transfer instructions
Standard Device Address	040 through 043
Interrupt Addresses	First PIM: 0100 through 0117 Second and succeeding PIMs: 0120 through 0177

Table 1-1 PIM Specifications (continued)

System Priority Assignment	Determined by location in the system priority chain (user-selected)
Logic levels (internal)	High = +2.4 to +5.0V dc Low = 0 to +0.4V dc
Logic levels (I/O bus)	High = +2.8 to +3.6V dc Low = 0 to +0.5V dc
Size	Contained on one 7-3/4-by-12-inch (19.7 x 30.3 cm) printed circuit board.
Power	5V dc at 0.45A
Operating Environment	0 to 50 degrees C, 0 to 90 percent relative humidity without condensation.

SECTION 2
INSTALLATION

2.1 INSPECTION

The PIM has been packed and inspected to ensure its arrival in good working order. To prevent damage, take care during unpacking and handling. Check the shipping list to ensure that all equipment has been received. Immediately after unpacking, inspect the equipment for shipping damage. If damage exists:

a. Notify the transportation company.

b. Notify Varian Data Machines.

c. Save all packing material.

2.2 PHYSICAL DESCRIPTION

The PIM circuits are contained on a single printed-circuit (PC) board (p/n 44P0683). As illustrated in figure 2-1, the board contains three connectors P1, J1, and J2. Connectors J1 and J2 each contain eight interrupt lines (IL00– through IL07–) that can be connected to selected peripheral controllers. Connector P1 also contains the same eight interrupt lines as well as all I/O bus control signals for the PIM.

2.3 PIM INTERRUPT LINES

The PIM has eight interrupt lines that enable up to eight peripheral controllers to be connected in the desired order of priority. The interrupt lines are designated IL00– through IL07– , where IL00– has the highest priority and IL07– the lowest. For controllers that are installed in the same chassis as the PIM, the interrupt lines are connected at the computer backplane connector that mates with P1 of the PIM board. For controllers in a different chassis, the interrupt lines are contained in either an I/O expansion cable that connects to P1 of the PIM (via computer backplane) or in an interrupt cable that connects to J1 or J2 of the PIM. Pin assignments for the interrupt lines are listed in table 2-1.

Table 2-1. Pin Assignments for Interrupt Lines

Interrupt Lines	P1	J1	J2	Interrupt Lines	P1	J1	J2
IL00–	108	3	3	IL04–	102	11	11
IL01–	114	13	13	IL05–	88	5	5
IL02–	104	9	9	IL06–	112	1	1
IL03–	110	15	15	IL07–	86	7	7

2.4 DEVICE ADDRESS ASSIGNMENT

The device address for each PIM is implemented with jumper wires installed on the computer backplane connector that mates with P1 of the PIM board (figure 2-2). Device addresses 040 through 043 are reserved for PIM. Normally 040 is assigned to the first PIM, 041 to the second, 042 to the third, and 043 to the fourth. Address 044 affects all PIMs simultaneously and is used to enable or disable all PIMs.

2.5 INTERCONNECTION

In the V70 series systems, the PIM is installed in a designated slot of an I/O chassis. Refer to the appropriate Varian 70 Series System Handbook for further installation information.

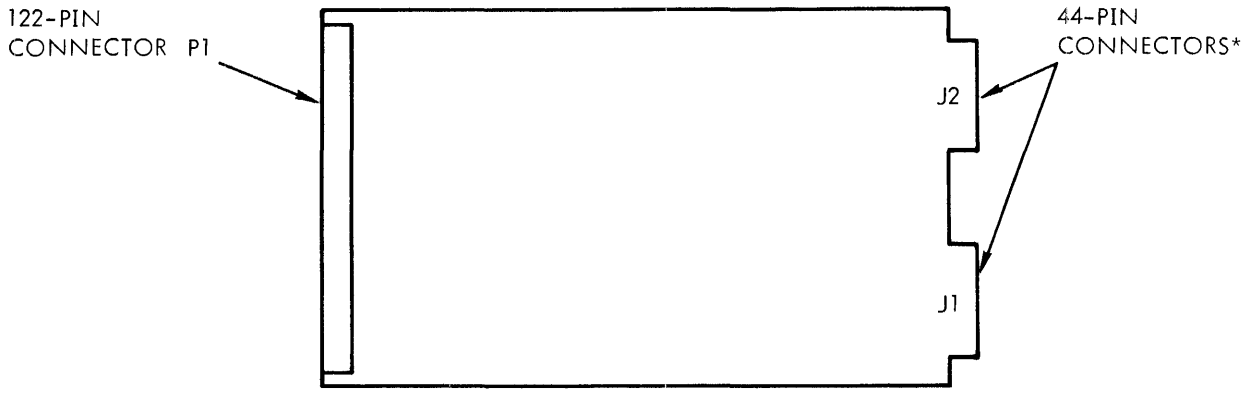

Figure 2-1. PIM Board (Component Side)

The PIM can be installed in designated slots of the mainframe and expansion chassis for 620/L systems, and in designated slots of the memory and I/O expansion chassis for 620/f-100 systems. Further installation information for these computer systems, can be found in the 620/L Maintenance Manual (document number 98 A 9905 15x) and the 620/f-100 Maintenance Manual (document number 98 A 9908 15x).

The pin assignments for the connectors on the PIM board are provided in logic diagram 91D0016.

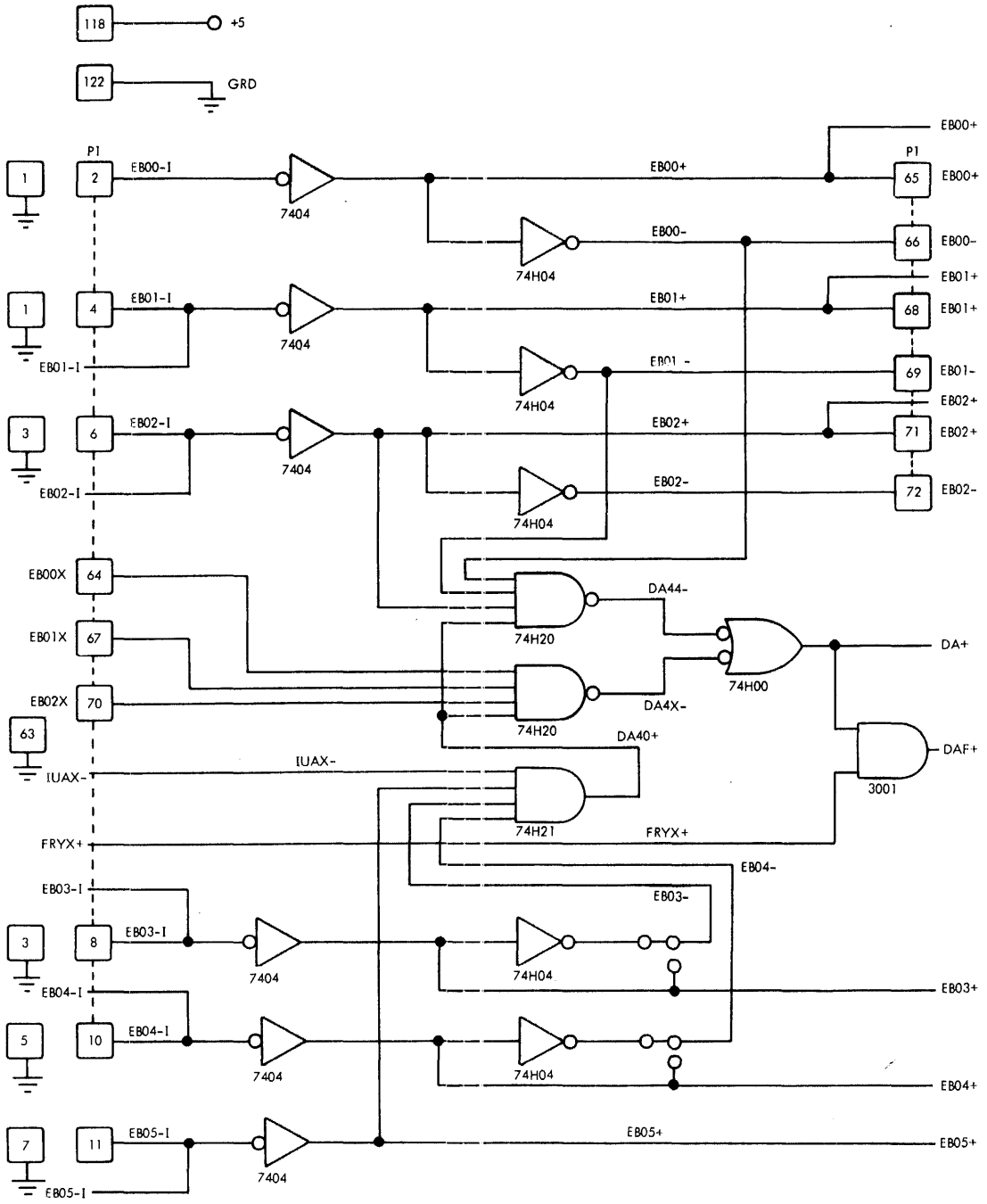

Figure 2-2. Device Address Connections

SECTION 3
OPERATION

The PIM has no operating controls or indicators. It operates under program control.

3.1 I/O INSTRUCTIONS

The PIM responds to the five external control and three data transfer instructions listed in table 3-1.

loops. Two NOP instructions are required after an external control (EXC) instruction.

For computer systems containing the memory protection (MP) option in addition to the PIM, the MP is disabled everytime an interrupt is serviced. Therefore at the end of the PIM service program, the MP must be enabled again.

Table 3-1. I/O Instructions

Mnemonic	Program Code	Functional Description
External Control		
EXC 014*	10014*	Clear interrupt registers.
EXC 024	10024	Enable PIM.
EXC 0244	100244	Enable all PIMs in system.
EXC 034	10034	Clear interrupt registers and enable PIM.
EXC 044	10044	Disable PIM.
EXC 0444	100444	Disable all PIMs in system.
EXC 054	10054	Clear interrupt registers and disable PIM.
Data Transfer		
OME 04	10304	Transfer contents of memory to mask register.
OAR 04	10314	Transfer contents of A register to mask register.
OBR 04	10324	Transfer contents of B register to mask register.

*** represents the last octal digit of the device address.**

3.2 PROGRAMMING CONSIDERATIONS

When preparing a PIM program, clear the interrupt registers to establish initial conditions. To mask peripheral controllers, write a mask word in the program. The eight least significant bits of the mask word correspond to the eight priority interrupt lines. Setting bit 0 inhibits the highest priority line, setting bit 1 inhibits the second-highest priority line, etc. The mask register must be loaded by the program after any power-up sequence, including the power-up cycle of the power failure/restart (PF/R) feature. System reset does not clear the PIM mask register.

When program loops contain only uninterruptable instructions, interrupts cannot occur. Thus, when recognition of an interrupt is imperative (such as with the PF/R), at least one no-operation (NOP) instruction must be added to such

3.3 UNINTERRUPTABLE INSTRUCTIONS AND CONDITIONS

An interrupt can only be detected during the last cycle of an instruction execution. In V70 and 620/f-100 systems using the memory protection feature, interrupts can be detected immediately following all instructions except:

a. Halt (HLT) instructions

b. Any external control (EXC) I/O instruction

c. Any execution instruction. If the condition is met, interrupts are inhibited between executions of an execution instruction and the instruction at the execution address. If the condition is not met,

interrupts are inhibited between executions of an execution instruction and the instruction following in sequence.

d. Any instruction executed in the step mode.

In Varian 70 series and 620/f-100 systems without the memory protection feature, detection of an interrupt is inhibited during the following types of instructions:

a. Halt (HLT) instructions

b. All shift instructions

c. All I/O instructions

d. All double-word instructions

e. All multiplication or division instructions

f. Any instruction executed in the step mode

In all 620/L systems, detection of an interrupt is inhibited during the following types of instructions and conditions:

a. Halt (HLT) instructions

b. All jump, jump and mark, or execution instructions when the jump condition is met. (When the jump condition is not met these instructions are interruptable).

c. All I/O instructions

d. All shift or rotation instructions

e. All multiplication or division instructions

f. During the processor cycle immediately following an external control (EXC) I/O instruction.

g. During the processor cycle immediately following a shift, rotation, multiplication, or division instruction during which a trap occurred (DMA operation).

h. During the first instruction executed after entering run mode if that instruction is a single-word instruction.

i. During a manual step operation

j. During a halt condition

3.4 PROGRAM EXAMPLE

Table 3-2 shows a typical program using the PIM. In this program, 256 descending binary frames are transferred to the high-speed paper tape punch. Memory locations 01000 to 01023 are used in the program as are computer mnemonic codes with corresponding machine language codes.

Table 3-2. Program Example

Machine Code		Source Code			
Location	**Instruction**	**Label**	**Mnemonic**	**Operand**	**Description**
001000		STRT	.ORG	.01000	
001000	011011		.LDA	.MASK	FETCH INTERRUPT MASK
001001	103140		.OAR	.040	AND STORE IN REGISTER
001002	006010		.LDAI	.0377	INITIALIZE OUTPUT DATA
001003	000377				
001004	103137		.OAR	.037	PRIME INTERRUPT MODULE
001005	100240		.EXC	.0240	ENABLE PIM
001006	005000		.NOP	.	
001007	001000		.JMP	.*-1	DELAY FOR INTERRUPTS
001010	001006				
001011	000376	MASK	.DATA	.0376	
*		INTERRUPT	PROCESSING	SUBR	
001012	000000	INTR	.ENTR	.	
001013	005311		.DAR	.	DECR OUTPUT DATA
001014	103137		.OAR	.037	OUTPUT DATA TO PUNCH
001015	100240		.EXC	.0240	RE-ENABLE PIM
001016	001010		.IAZ	.*+4	
001017	001022				
001020	001000		.JMP*	.INTR	EXIT
001021	101012				
001022	100440		.EXC	.0440	CLEAR PIM
001023	000000		.HLT	.	END OF PROGRAM
		INTERRUPT	ADDRESS		
000100			.ORG	.0100	
000100	002000		.JMPM	.INTR	
000101	001012				
	000000		.END	.	

SECTION 4
THEORY OF OPERATION

4.1 GENERAL

Communication between the PIM and the processor is similar to that of any peripheral controller except that the PIM can request a program interrupt. When the computer acknowledges the interrupt, the PIM specifies the memory location of the instruction to be executed.

The PIM scans the interrupt lines with every cycle of the interrupt clock (IUCX-I). If signals are detected on more than one line, the highest-priority signal is acknowledged. The remaining interrupt requests are stored in the PIM interrupt-line register until acknowledged. The PIM has an eight-bit mask register that selectively inhibits interrupt requests from the interrupt-line register. When a given flip-flop of the mask register is set, corresponding interrupt requests from the interrupt-line register are inhibited. When the mask register flip-flop is reset, the interrupt request is not inhibited. The mask register is unaffected by system reset and must be loaded under program control using data-transfer instructions.

Acknowledgment of an interrupt by the processor causes execution of the instruction located at the memory address specified by the PIM. Any instruction can be executed except an I/O type. An interrupt is thus serviced in one instruction period.

4.2 FUNCTIONAL DESCRIPTION

The following subsections describe the five functional circuits of the PIM (figure 4-1). Refer to the timing waveforms of figure 4-2 and the PIM logic diagram.

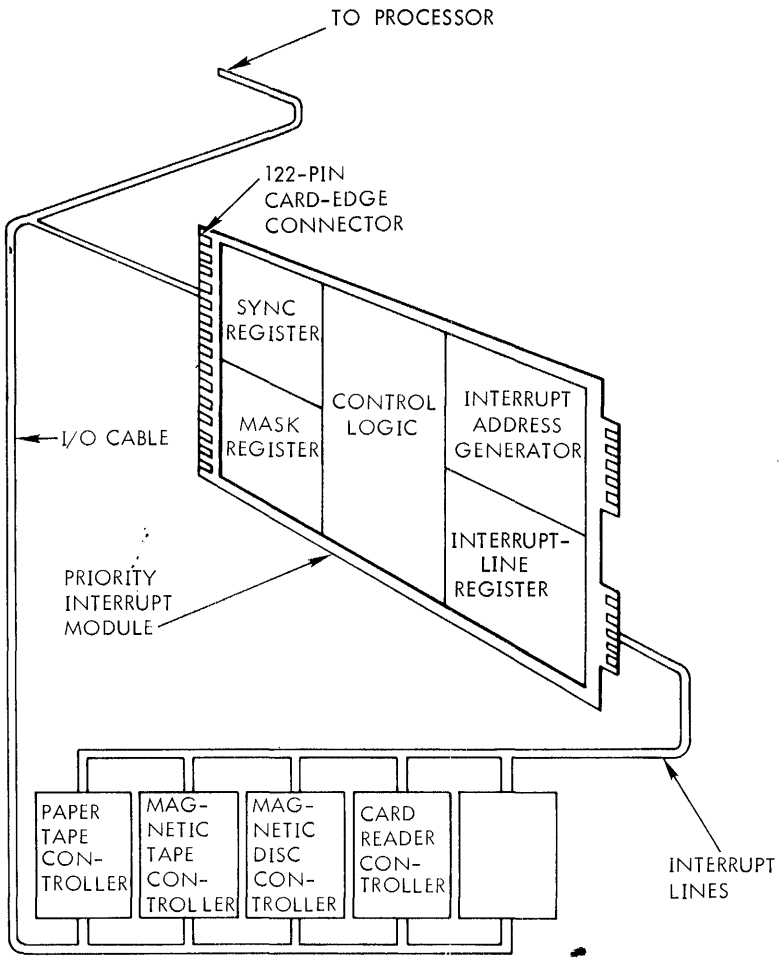

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Figure 4-1. PIM Functional Block Diagram

4.2.1 Control Logic

The control logic circuit directs and sequences the response of the PIM to external control, data transfer, and interrupt operations. When a computer program interrupt is requested, the processor requests the PIM to place the interrupt address on the I/O bus. If the PIM has system priority, the address line drivers are enabled. The PIM interrupt-request signal will remain active until all interrupts stored (but not inhibited) by the PIM have been acknowledged, or until PIM priority is lost.

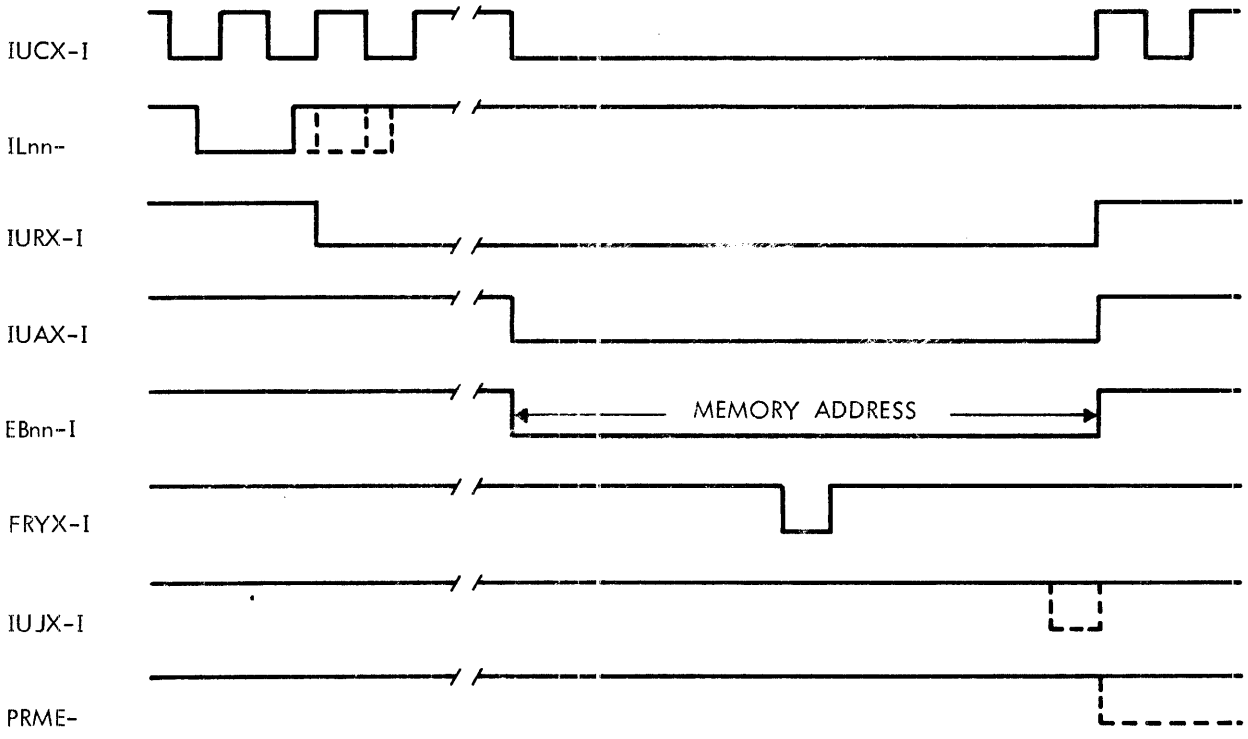
The control logic circuit consists of flip-flops PRME, DTOX, IURM and associated gates. During the execution of an output data transfer command, signals FRYX and DA set DTOX. DTOX+ high and DRYX+ generate SMR1- low, which transfers the mask word from the I/O bus to the mask register. At the end of the transfer, DRYX+ resets flip-flop DTOX. DA, in conjunction with FRYX+, indicates that the central processor is communicating with the PIM.

External control commands for the PIM are indicated by EXCX+ low. EB06+, EB07+, and EB08+ are combined with EXCX+ to actuate the five external control commands.

Flip-flop PRME provides master enable/disable for the entire PIM. When PRME is reset, computer program interrupts cannot be requested by the PIM; however, the PIM continues to receive and store interrupts from external devices. When PRME+ is high, flip-flop IURM is set by INR1+ high, one IUCX-I clock period after an interrupt is clocked into the sync register. IURM+ and PRME+ high plus PRMX-I low generate IURX-I low, requesting an interrupt.

When a computer program interrupt is requested by the PIM, the processor responds with signal IUAX-I low. This signal requests that PIM place the interrupt instruction address on the I/O bus.

If the PIM has system priority, the address line drivers are enabled as long as IUAX-I is low. When IUAX-I goes low, IUCX-I is held low. Interrupt conditions are therefore held static during the time that IUAX-I is low. Flip-flop IURM is cleared when all interrupts received by the PIM have been acknowledged by the central processor.



VTII-347B

Figure 4-2. Timing for Reception and Servicing of a Single Interrupt

4.2.2 Interrupt Address Generator

The interrupt address generator consists of coding logic that generates the binary number of the interrupt line requesting the interrupt. A pair of memory locations is reserved for each interrupt line. The interrupt addresses are normally in memory locations 0100 through 0117. However, the 16 interrupt addresses can be placed anywhere within the first 128 memory locations except 040 through 047, and may be placed at other addresses by special request.

The interrupt address generator consists of three gates that use line priority signals to generate signals A0XX+, A1XX+, and A2XX+. These signals consititute three bits of the address code for the interrupt line to be serviced. They are placed on the I/O bus by IAEX+ low. The least-significant bit of the address code is always low, resulting in an even address. This bit is supplied by the processor when the second word of a double-word interrupt instruction is accessed.

Signal IAEX+ low is generated by signals PRMX-I and IUAX-I low and FF set signal PRME+ and IURM+ high. These four signals indicate, respectively, that: the PIM has priority; the PIM interrupt has been acknowledged; the PIM is activated; and interrupt awaits on one of the interrupt lines.

4.2.3 Interrupt-Line Register

The interrupt-line register consists of eight flip-flops that asynchronously accept interrupt inputs. An interrupt is stored in the register until the interrupt is serviced or until the entire register is cleared by command.

The interrupt-line register consists of flip-flops LR00 through LR07. An interrupt is generated when an interrupt line signal, ILnn−, goes low. IL00− through IL07− are each connected to the clock input of an interrupt-line register flip-flop. ILnn− may remain low for any period of time greater than 0.2 microseconds; a constant low does not produce repetitive interrupts. If the interrupt is serviced, the flip-flop is reset by IUCP+ and a line priority signal, LPnn+. Although IUCP+ is sent to all register flip-flops, only the flip-flop that was serviced is reset.

4.2.4 Sync Register and Line Priority

The sync register consists of eight flip-flops. At each interrupt clock period, the outputs of the interrupt-line register are clocked into the sync register. The sync register, therefore, samples the status of the eight interrupt lines synchronously with the computer interrupt clock. The sync register outputs activate the priority logic used to generate the interrupt address.

If two or more interrupts occur simultaneously, the line with the highest priority is given precedence and all other lines are temporarily inhibited. An interrupt line can request a computer program interrupt only if the line has not been inhibited and a higher-priority line is not active.

The sync register consists of flip-flops IR00 through IR07. IUC1− clocks the contents of the interrupt-line register into the sync register. The outputs of the sync register are fed into a network of gates that determine the priority of each interrupt line signal. The line priority circuit generates signal INR1+, which enables the generation of signal IURX−I. In addition, LP00+ through LP07+ determine the interrupt address and the interrupt-line register flip-flop to be reset after servicing its interrupt. IL00− has the highest priority, and signal IL07− has the lowest.

4.2.5 Mask Register

The mask register inhibits interrupt requests from selected interrupt lines to be disarmed while other lines are permitted to cause a program interrupt. The eight flip-flops of the mask register inhibit corresponding interrupt requests from the interrupt-line register. The mask register must be loaded under program control to establish which interrupts are to be inhibits.
EB00+ through EB07+ are loaded into the mask register when a particular interrupt is to be masked (inhibited). SMR1+ clocks this mask word into the register. The register outputs are fed into the line priority circuit. If one or more interrupts are inhibited by the mask register, the highest-priority unmasked interrupt is serviced.

SECTION 5
MAINTENANCE

Maintenance personnel should be familiar with the contents of this manual before attempting PIM troubleshooting. The Varian MAINTAIN III test program system (Test Programs Manual, 98 A 9952 07x) contains a PIM test program used to test various phases of PIM operation. Further diagnosis can then be made by referring to this manual.

5.1 TEST EQUIPMENT

The following test equipment and tools are recommeded for maintenance:

a. Oscilloscope, Tektronix type 547 with dual-trace plug-in unit, or equivalent.

b. Multimeter, Triplett type 630 or equivalent.

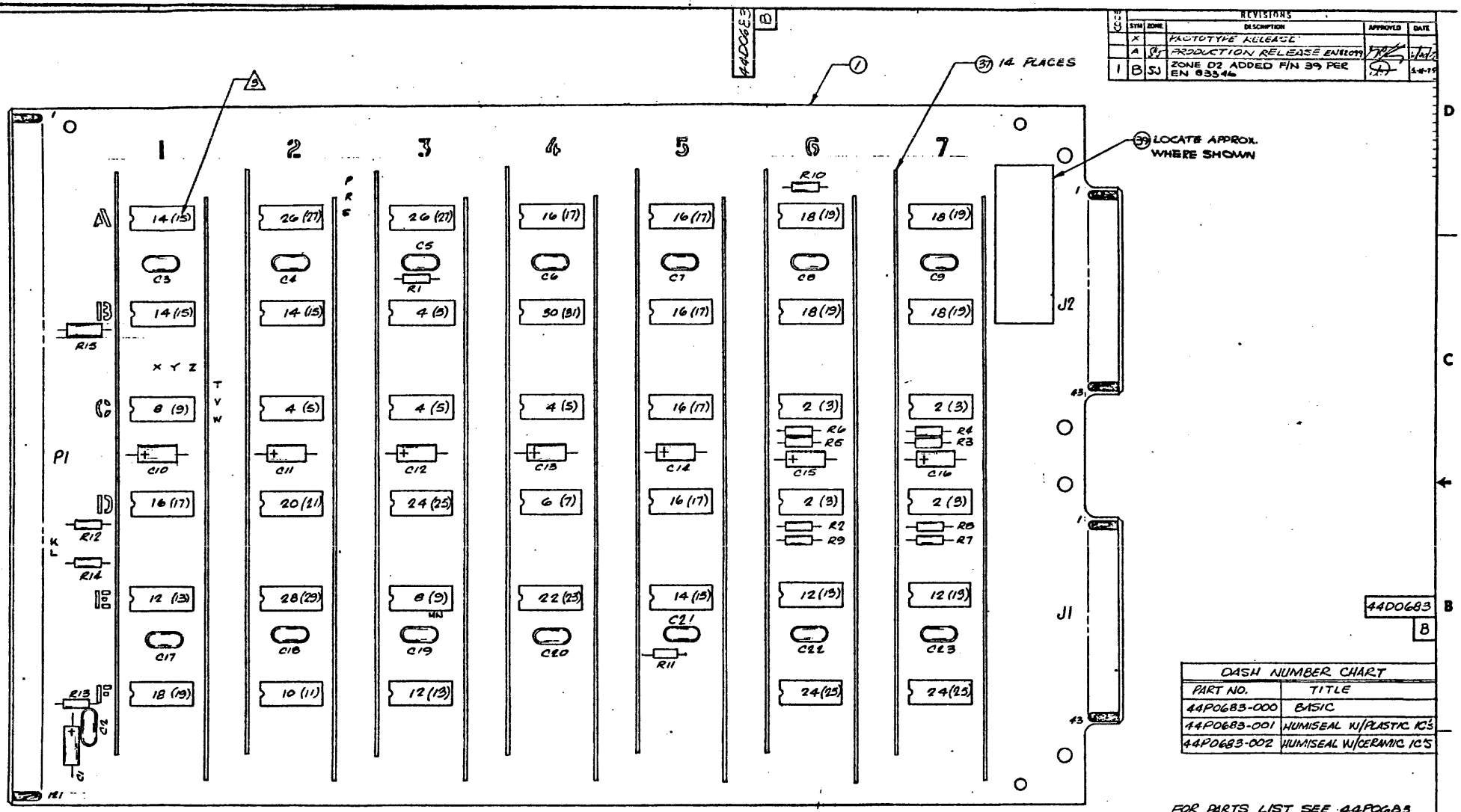
c. Soldering iron, 39-watt pencil type.

5.2 CIRCUIT-BOARD REPAIR

If it has been determined that circuit-board repair is required, it is recommended that the Varian Data Machines customer service department be contacted so that a new circuit board can be installed in the user's system and the faulty one returned to the factory for repairs. However, if the user decides to perform his own repairs, caution should be used so that the circuit board is not permanently damaged. Approved repair procedures should be followed such as the ones described in document IPC-R-700A prepared by the Institute of Printed Circuits.

SECTION 6
MNEMONICS

Mnemonics	Description
AnXX	Address code of device with priority interrupt.
CACR	Clear ac register. Generates signal CILR on receipt of signal EXCX.
CILR	Clear line register. Clears the line and sync registers.
DA	Decoded device address.
DRYX	Data ready pulse that resets flip-flop DTOX; enables signal SMR1.
DTOX	Data transfer out flip-flop. Stores the occurrence of an output command from the processor.
EBnn-I	Address or function code bit from I/O bus.
EXCX	Enables initialization of PIM upon external control command.
FRYX	Function ready pulse that sets flip-flop DTOX.
IAEX	Interrupt address enable. Gates address of interrupt line onto I/O bus.
ILnn	Interrupt line from peripheral controller.
INRn	Interrupt request. Indicates a request from one or more interrupt lines.
IRnn	Sync register outputs. Stores the status of the line register in synchronism with the interrupt clock signal.
IUAX	Interrupt acknowledgment. Enables servicing of PIM interrupts.
IUCP	Interrupt completion resets line register flip-flop after interrupt is serviced.
IUCX	Interrupt clock. Provides timing for servicing of PIM interrupt request.
IUCI	Interrupt clock inverted. Clocks contents of line register into sync register.
IUDX	Interrupt detection. Sets flip-flop IURM.
IUJX	Interrupt jump. Inhibits the PIM after a jump and mark command.
IURM	Interrupt request memory flip-flop. Stores a request for an interrupt from an interrupt line.
IURX-I	Interrupt request. Sent to the processor to request signal IUAX-I.
KPRME	K-input to PRME
LPii	Line priority signals. Indicates the eight PIM priorities.
LRnn	Line register flip-flop outputs. Stores request for an interrupt from a device connected to an interrupt line.
PRME	PIM enabling flip-flop. Stores the activation of the PIM.
PRMX	Priority input. Gives priority to PIM.
PRNX	Priority output. Passes priority to next in line after interrupts are serviced.
SMR1	Clocks mask word into mask register.
SYRT	System reset. Clears flip-flops DTOX and PRME and generates signal CILR when control-panel reset switch is pressed.


44D0683 B
REVISIONS
SYM | ZONE | DESCRIPTION | APPROVED | DATE
X | | PROTOTYPE RELEASE
A | SJ | PRODUCTION RELEASE EN11099
B | SJ | ZONE D2 ADDED F/N 39 PER EN 03346
(1)
(3) 14 PLACES
(5)
(39) LOCATE APPROX. WHERE SHOWN
1 2 3 4 5 6 7
A B C D
P1
J1
J2
R10
R15
R12
R14
R13
C4
C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23
R1 R11 R2 R3 R4 R5 R6 R7 R8 R9
X Y Z
T V W
K L
14 (15) 26 (27) 26 (27) 16 (17) 16 (17) 18 (19) 18 (19)
14 (15) 14 (15) 4 (5) 50 (51) 16 (17) 18 (19) 18 (19)
8 (9) 4 (5) 4 (5) 4 (5) 16 (17) 2 (3) 2 (3)
16 (17) 20 (21) 24 (25) 6 (7) 16 (17) 2 (3) 2 (3)
12 (13) 28 (29) 8 (9) 22 (23) 14 (15) 12 (13) 12 (13)
18 (19) 10 (11) 12 (13) 24 (25) 24 (25)
44D0683 B
DASH NUMBER CHART
PART NO. | TITLE
44P0683-000 | BASIC
44P0683-001 | HUMISEAL W/PLASTIC IC'S
44P0683-002 | HUMISEAL W/CERAMIC IC'S
FOR PARTS LIST SEE 44P0683
5. NUMBERS IN PARENTHESIS ( ) ARE FOR THE -002 ONLY. -000 & -001 VERSIONS SHOWN
4 AFTER FINAL TEST AND PRIOR TO ACCEPTANCE TEST (-001, -002 ONLY) MASK OFF CONNECTOR CONTACT AREA ON BOTH SIDES OF F/N 1 AND TOTALLY COAT BOTH SIDES OF ASSEMBLY WITH F/N 38.
1 MARK WITH APPROPRIATE DASH NO. AND THE REVISION LETTER OF THE PARTS LIST TO WHICH THE PART WAS MANUFACTURED AND THE SERIAL NO. APPROX WHERE SHOWN. IDENTIFICATION TO BE .12 HIGH CHARACTERS PERMANENT AND LEGIBLE.
NOTE: UNLESS OTHERWISE SPECIFIED
MODEL NO. 620/VT3
NEXT ASSY 01P0094
MATERIAL
FINISH
DIMENSIONS ARE IN INCHES AND AFTER FINISHING
TOLERANCES (UNLESS OTHERWISE SPECIFIED)
X ± .1
.XX ± .03
.XXX ± .005
ANGLES ± 0.5°
BREAK ALL SHARP EDGES .005 R APPROX
DO NOT SCALE DRAWING
DR K.Williams 3/21/73
CHK (J.) Brown 4/9/73
DSGN D.Wing 4/9/73
ENGR E.F.Neuman 4/11/73
APPD [illegible] 4/11/73
APPD
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2722 michelson drive / irvine / california / 92665
TITLE
PRIORITY INTERRUPT ASSY DM 398
CODE IDENT NO. 21101
SIZE D
DWG NO 44D0683
REV B
SCALE 2/1
SHEET 1 OF 1

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE 1/4 W, 5%

2. THIS DRAWING CONSISTS OF THE FOLLOWING SHEETS: 1.0, 2.0, 3.0, 4.0, 5.0, 6.0, 7.0, 8.0, 9.0, 10.0

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C23	
R15	
P2,	
J2	

REFERENCE DRAWINGS	
40D0617	BOARD DETAIL
44D0683	ASSEMBLY
44P0683	PARTS LIST
97E0863	ARTWORK
97E0864	SILKSCREEN
97E0865	SOLDER MASK

DR C. WARNER	5-17-73	varian data machines /a varian subsidiary 2722 michelson drive / irvine / california / 92664
CHK W. Brown	5-29-73	
DSGN		TITLE: LOGIC DIAGRAM - PRIORITY INTERRUPT MODULE, DM 398
ENGR T. E. Hanson	6/15/73	
APPD [signature]	6/15/73	
APPD		

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CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0454	A
SCALE			SHEET 1.0 OF

REVISIONS					
CODE	SYM	ZONE	DESCRIPTION	APPROVED	DATE
—	A		PRODUCTION RELEASE PER EN 82099		
—	—		ADDED WIRING TABLE & NOTES 1 & 2 TO SHT 5 PER EN 83034		

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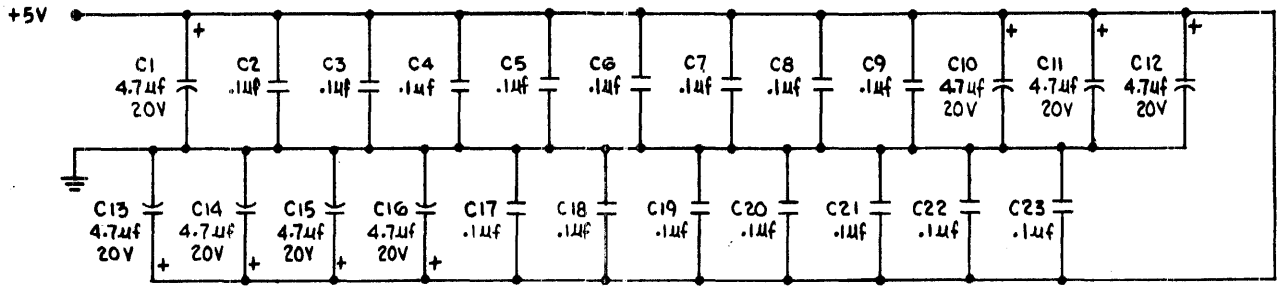

DECOUPLING, TABLE OF CONTENTS, & REVISIONS

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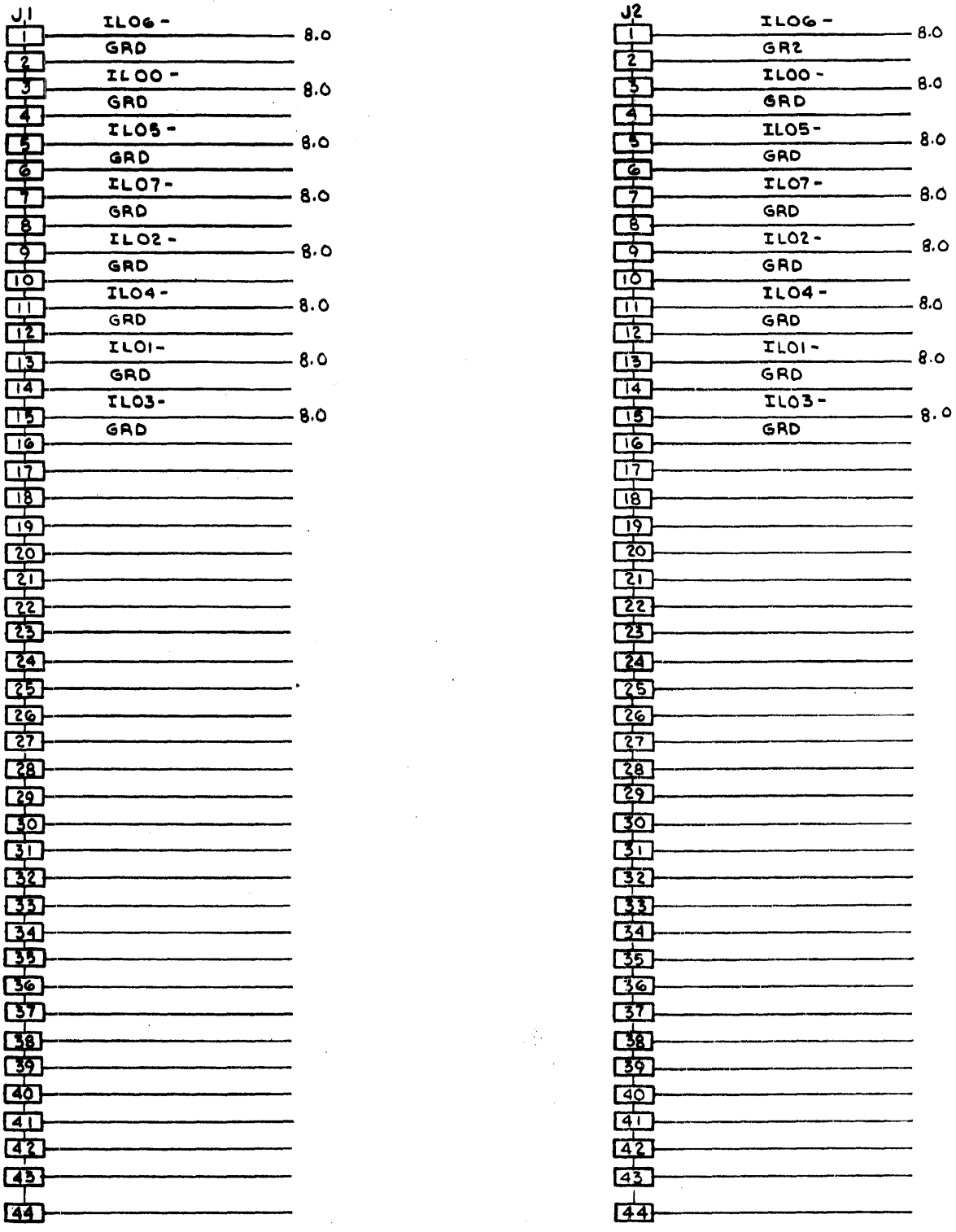

CONNECTOR FUNCTIONS

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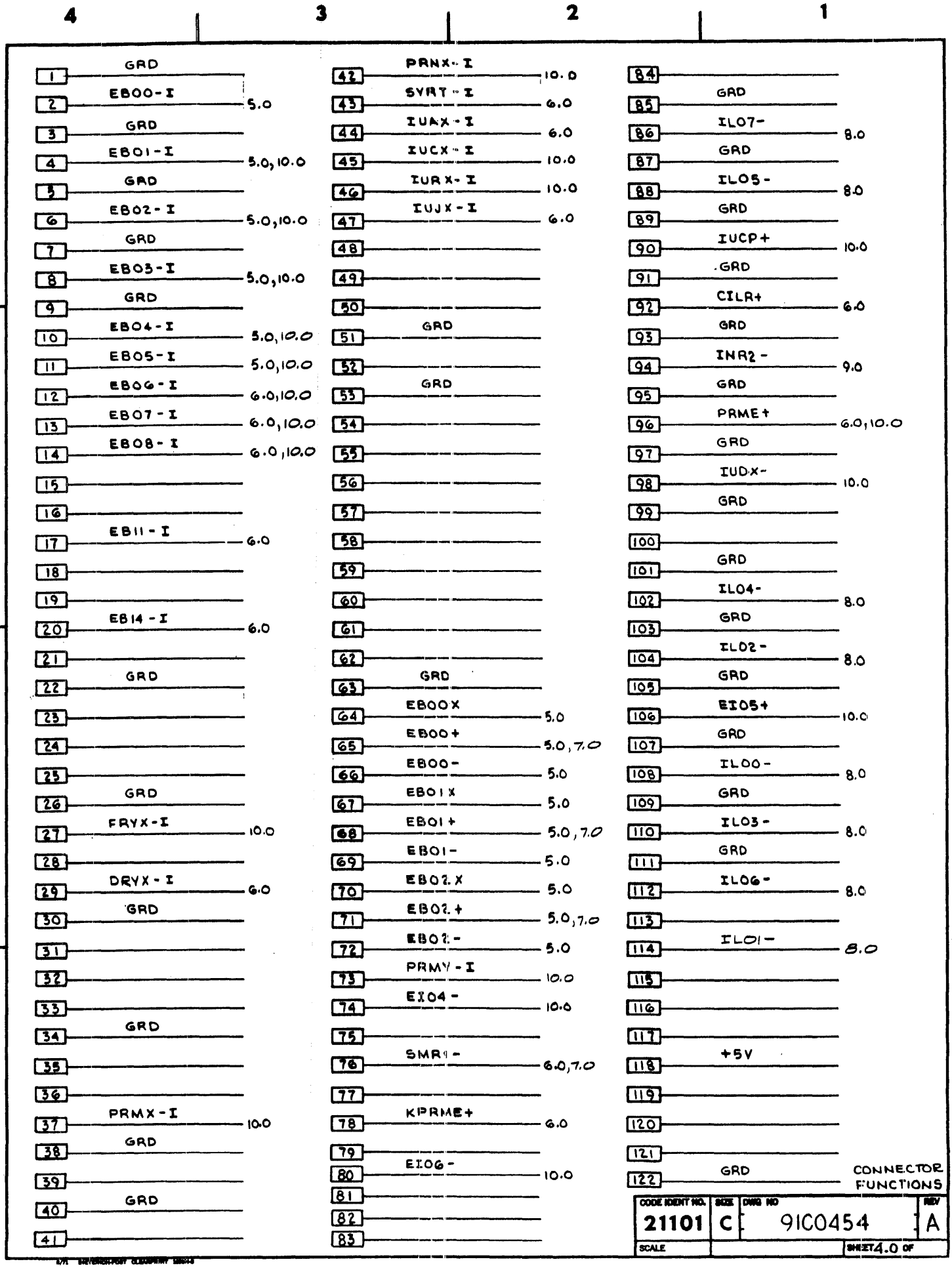
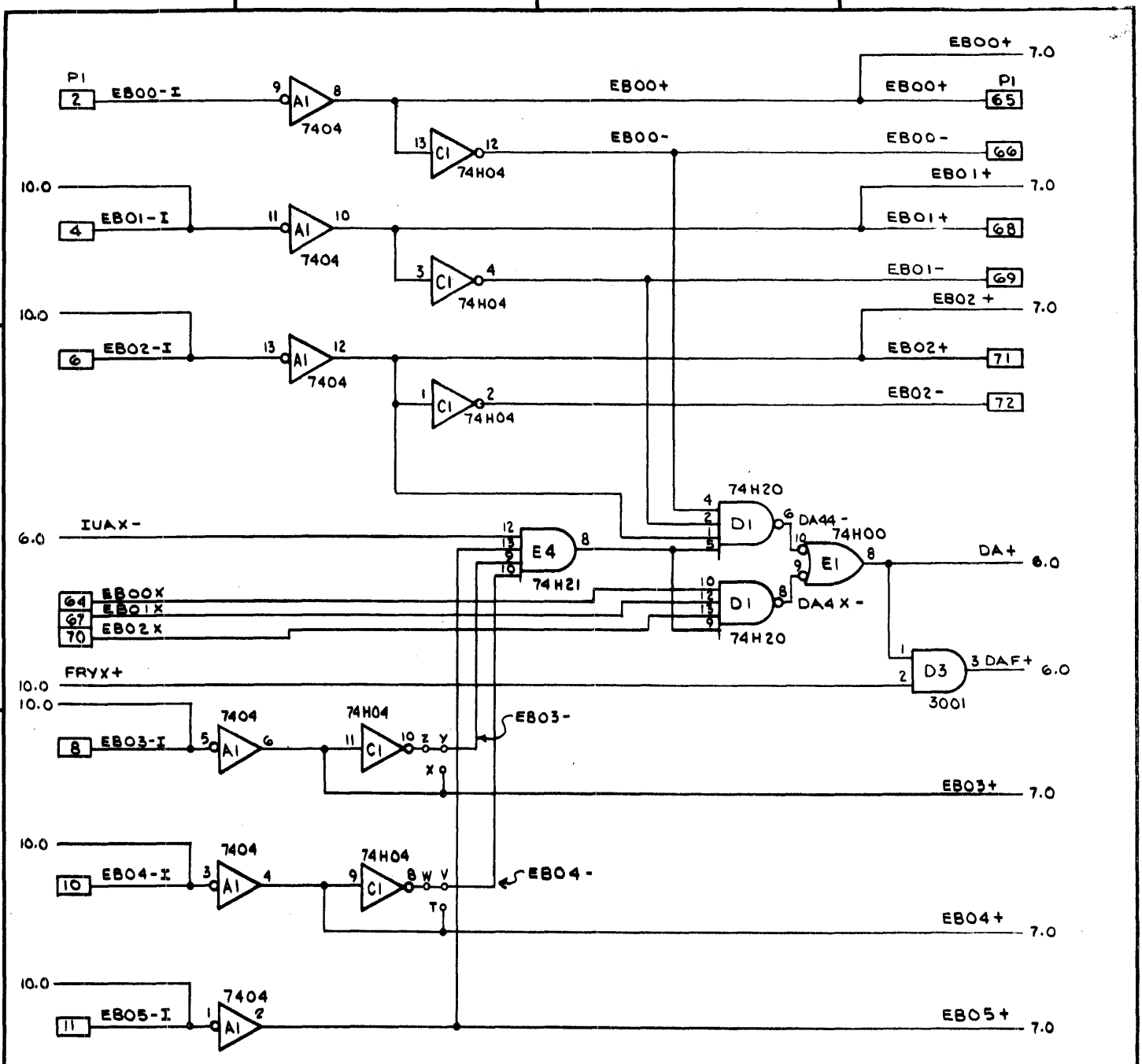
SCALE		SHEET 3.0 OF	


4
3
2
1
D
C
B
A
1 GRD
2 EB00-I 5.0
3 GRD
4 EB01-I 5.0,10.0
5 GRD
6 EB02-I 5.0,10.0
7 GRD
8 EB03-I 5.0,10.0
9 GRD
10 EB04-I 5.0,10.0
11 EB05-I 5.0,10.0
12 EB06-I 6.0,10.0
13 EB07-I 6.0,10.0
14 EB08-I 6.0,10.0
15
16
17 EB11-I 6.0
18
19
20 EB14-I 6.0
21
22 GRD
23
24
25
26 GRD
27 FRYX-I 10.0
28
29 DRYX-I 6.0
30 GRD
31
32
33
34 GRD
35
36
37 PRMX-I 10.0
38 GRD
39
40 GRD
41
42 PRNX-I 10.0
43 SYRT-I 6.0
44 IUAX-I 6.0
45 IUCX-I 10.0
46 IURX-I 10.0
47 IUJX-I 6.0
48
49
50
51 GRD
52
53 GRD
54
55
56
57
58
59
60
61
62
63 GRD
64 EB00X 5.0
65 EB00+ 5.0,7.0
66 EB00- 5.0
67 EB01X 5.0
68 EB01+ 5.0,7.0
69 EB01- 5.0
70 EB02X 5.0
71 EB02+ 5.0,7.0
72 EB02- 5.0
73 PRMY-I 10.0
74 EI04- 10.0
75
76 SMR1- 6.0,7.0
77
78 KPRME+ 6.0
79
80 EI06- 10.0
81
82
83
84
85 GRD
86 IL07- 8.0
87 GRD
88 IL05- 8.0
89 GRD
90 IUCP+ 10.0
91 GRD
92 CILR+ 6.0
93 GRD
94 INR2- 9.0
95 GRD
96 PRME+ 6.0,10.0
97 GRD
98 IUDX- 10.0
99 GRD
100
101 GRD
102 IL04- 8.0
103 GRD
104 IL02- 8.0
105 GRD
106 EI05+ 10.0
107 GRD
108 IL00- 8.0
109 GRD
110 IL03- 8.0
111 GRD
112 IL06- 8.0
113
114 IL01- 8.0
115
116
117
118 +5V
119
120
121
122 GRD
CONNECTOR FUNCTIONS
CODE IDENT NO. 21101
SIZE C
DWG NO 9100454
REV A
SCALE
SHEET 4.0 OF



DEVICE ADDRESS WIRING TABLE

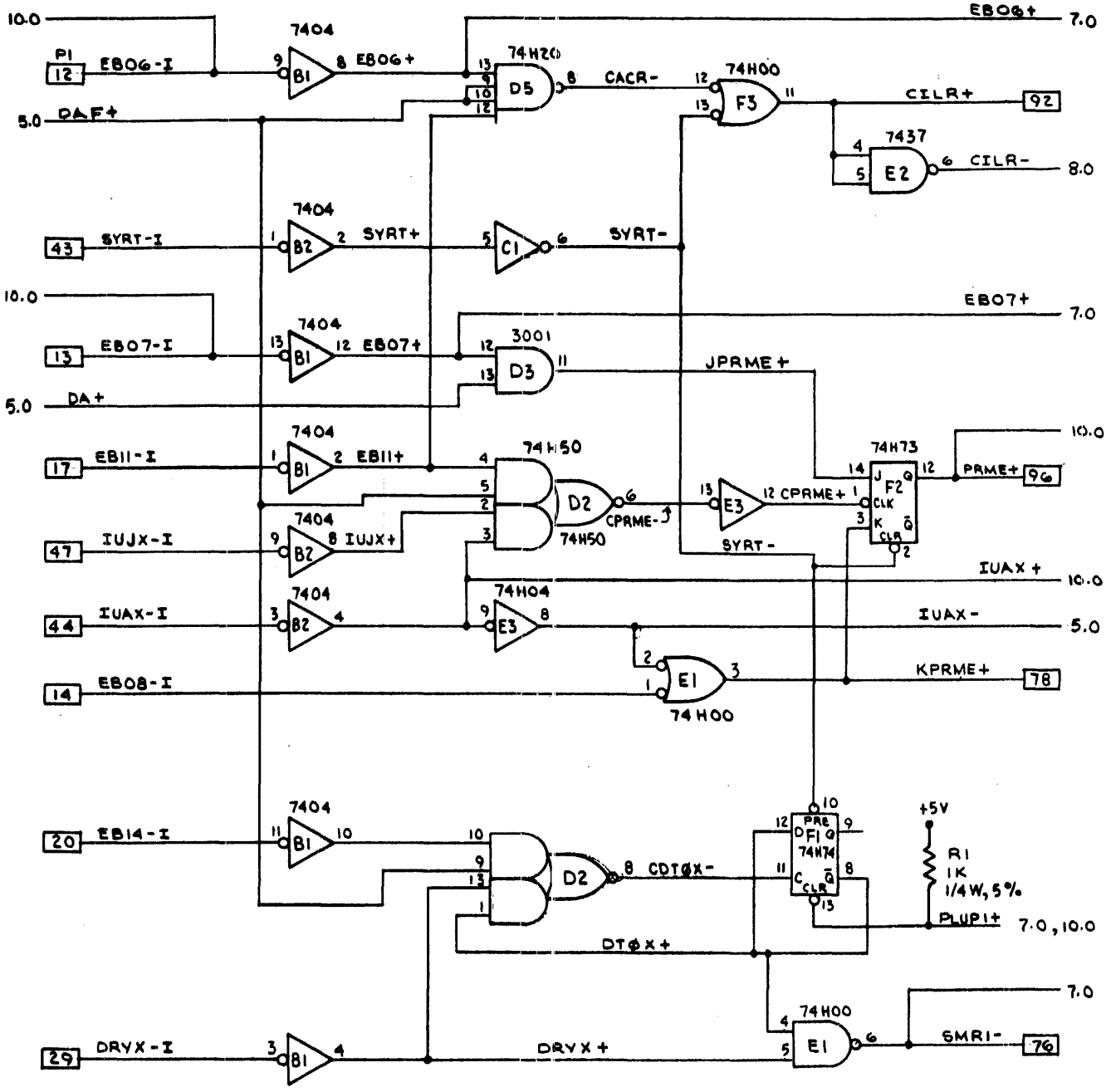
TO SELECT DEVICE ADDRESS	ADD W/W JUMPER FROM P1		
	PIN 64 TO PIN	PIN 67 TO PIN	PIN 70 TO PIN
40	66	69	72
41	68	69	72
42	66	68	72
43	68	68	72
44	66	69	71
45	65	69	71
46	66	68	71
47	65	68	71

2. TO INSTALL A NEW PIM(44P0688) IN PLACE OF AN OLD STYLE PIM(44P0172), REMOVE ENTIRE WIRE WRAP STRING(IF ANY) BETWEEN PIN 68 AND ANY OF THE FOLLOWING PINS: 66, 69 AND 72.

1. MAKE NO CONNECTION TO PIN 68 FOR DEVICE ADDRESSING

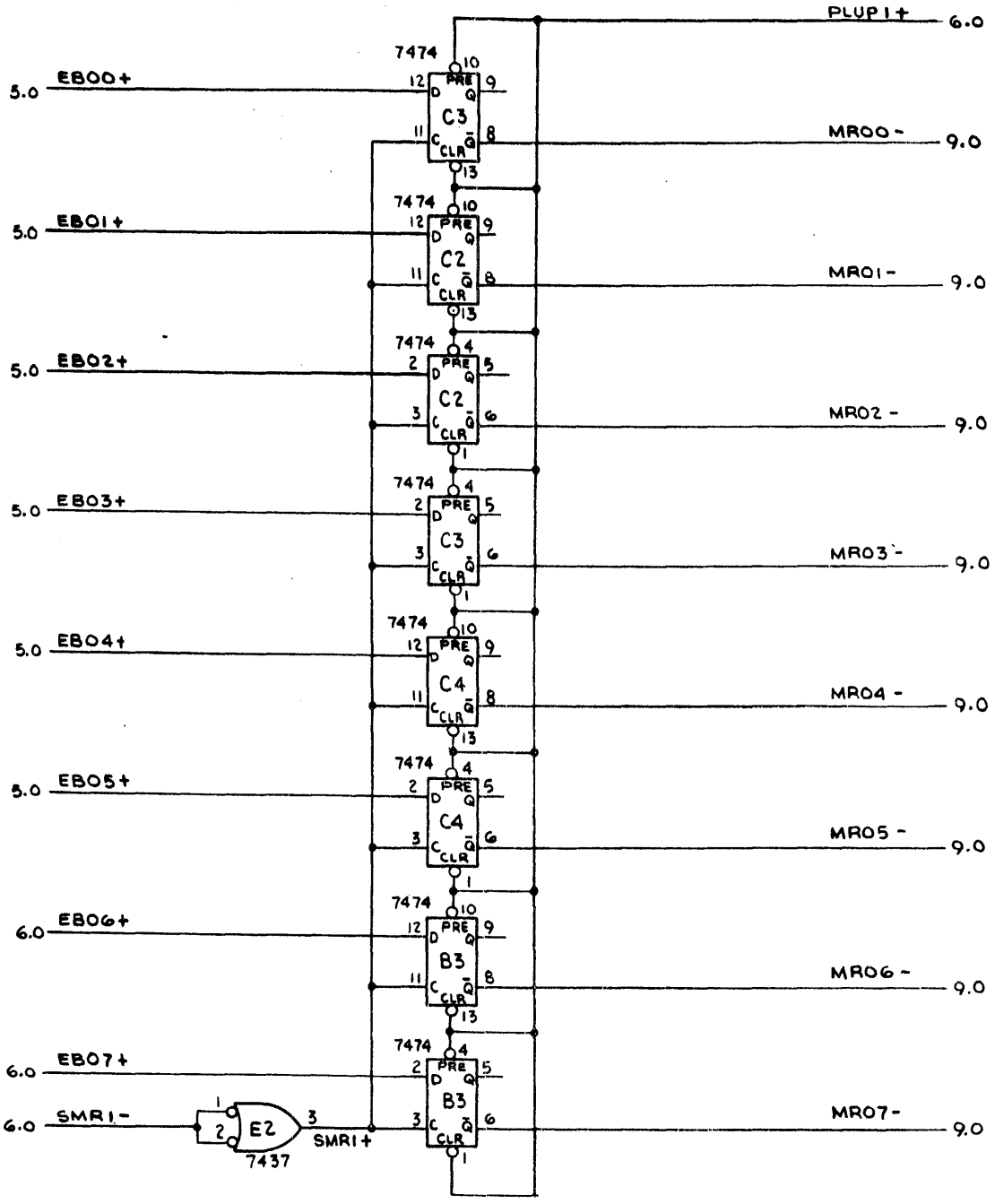
E-BUS RECEIVERS & DEVICE ADDRESS DECODE

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0454	A
SCALE		SHEET 5.0 OF	



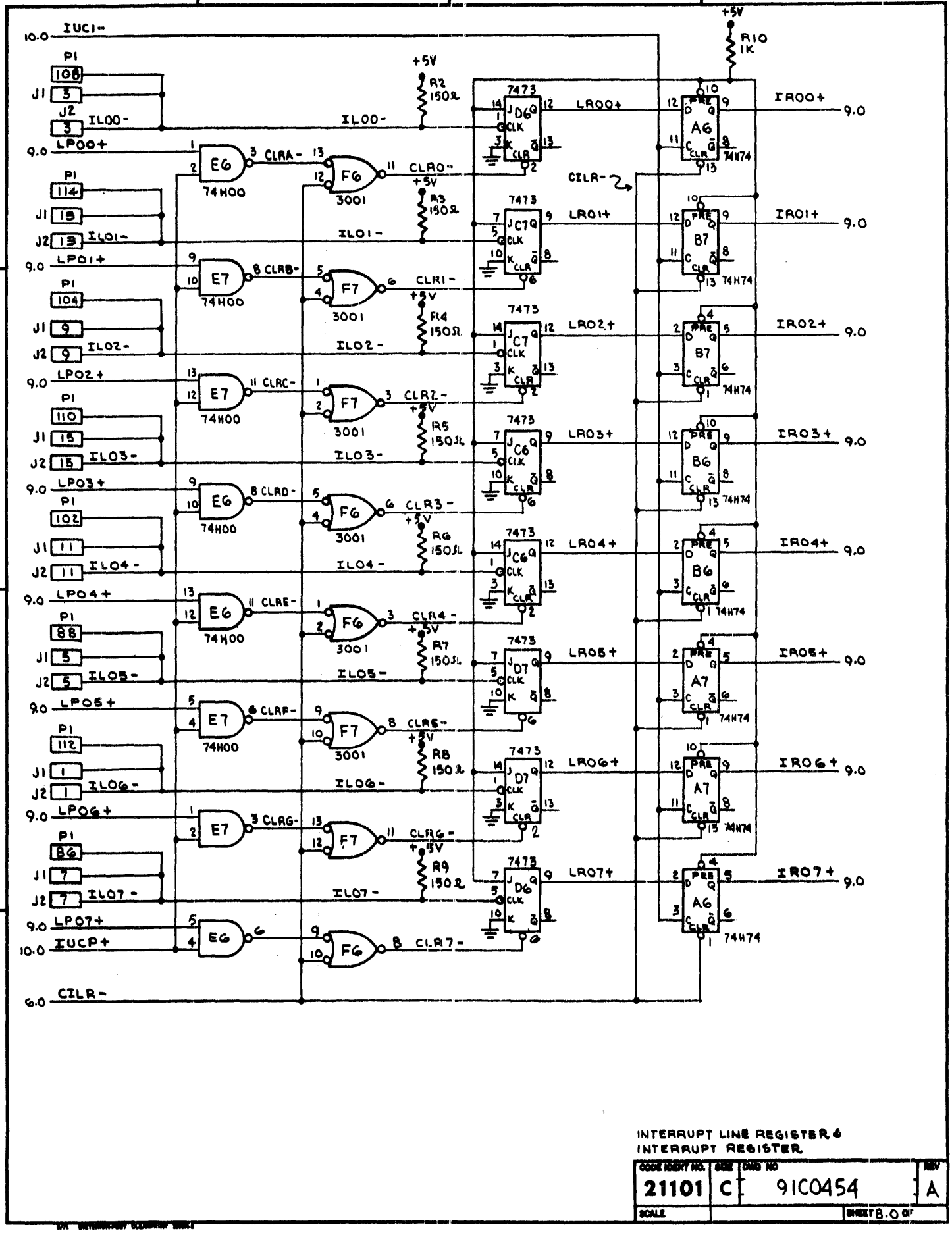
E-BUS RECEIVERS & CONTROL LOGIC

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9IC0454	A
SCALE			SHEET 6.0 OF



INTERRUPT MASK REGISTER

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9IC0454	A
SCALE			SHEET 7.0 OF



INTERRUPT LINE REGISTER &
INTERRUPT REGISTER

CODE IDENT NO.	SIZE	DWG NO	REV
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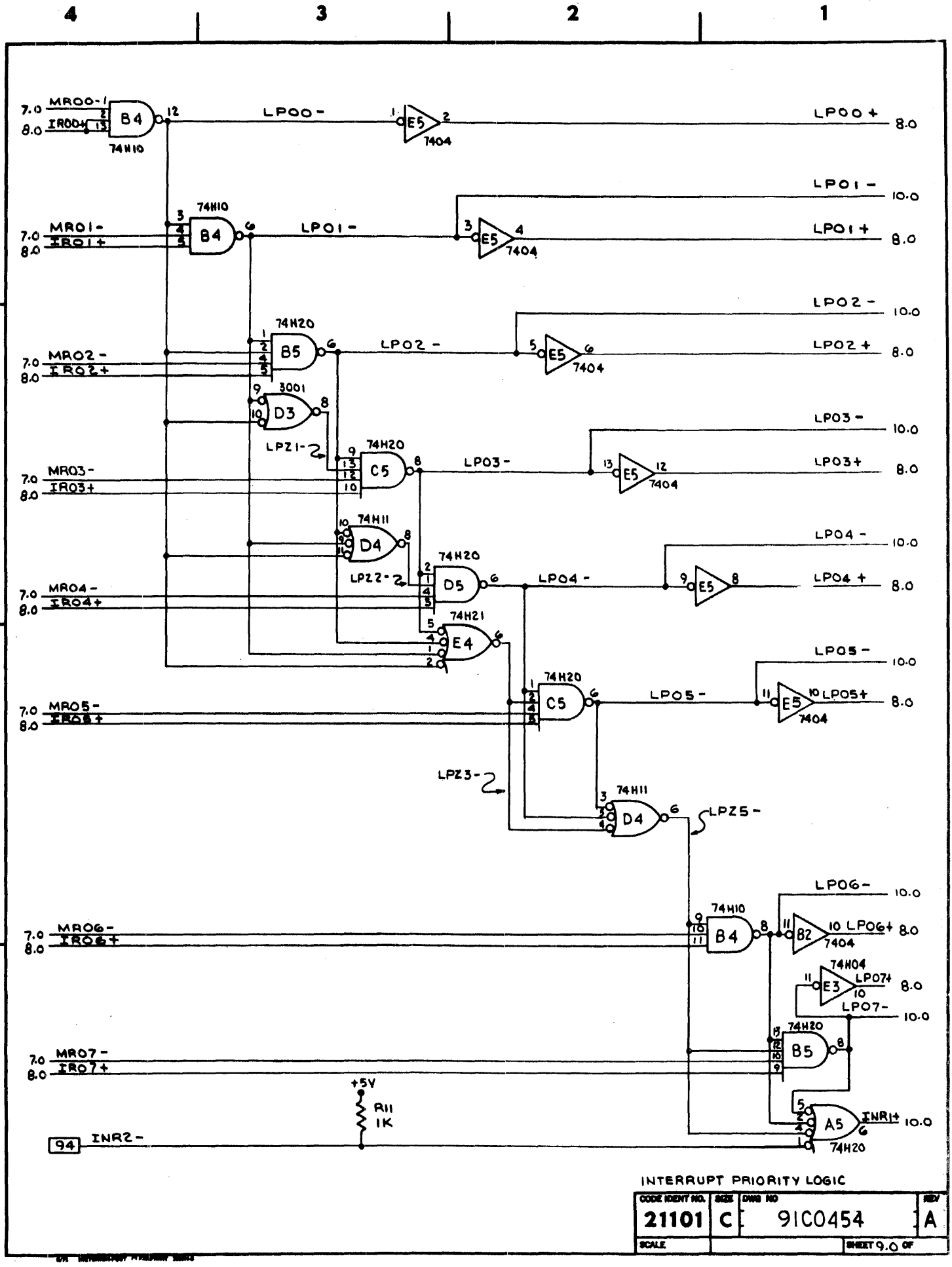
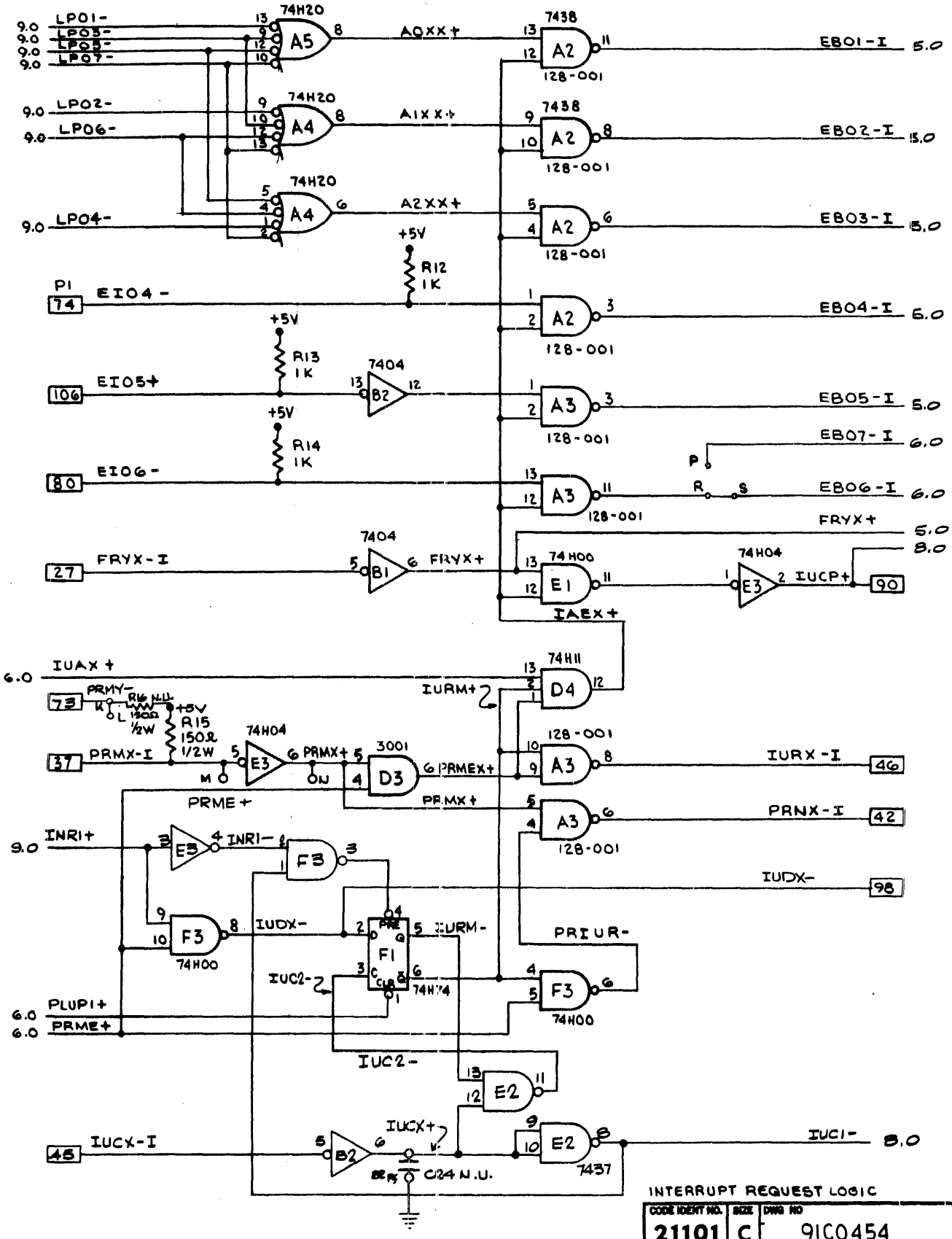
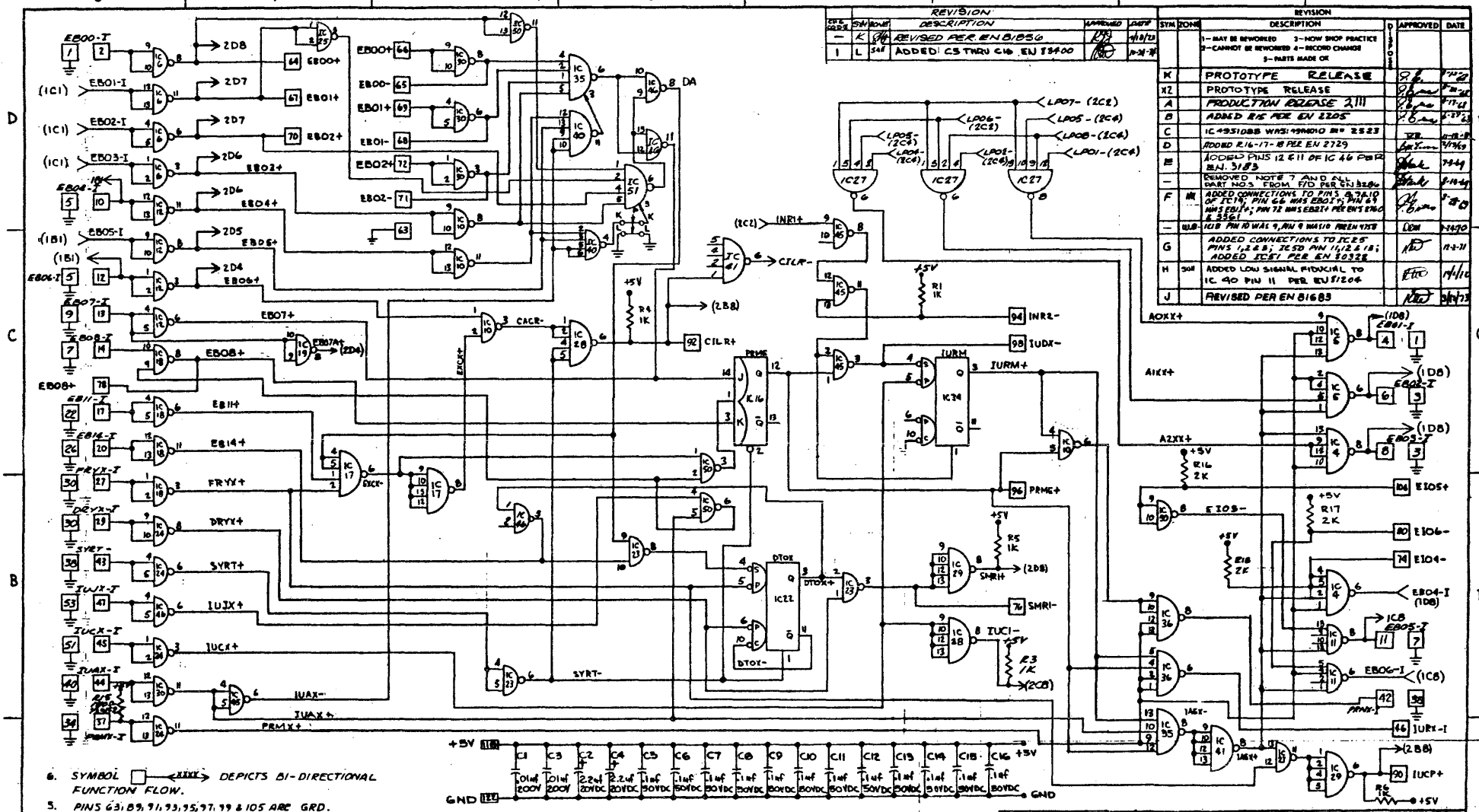
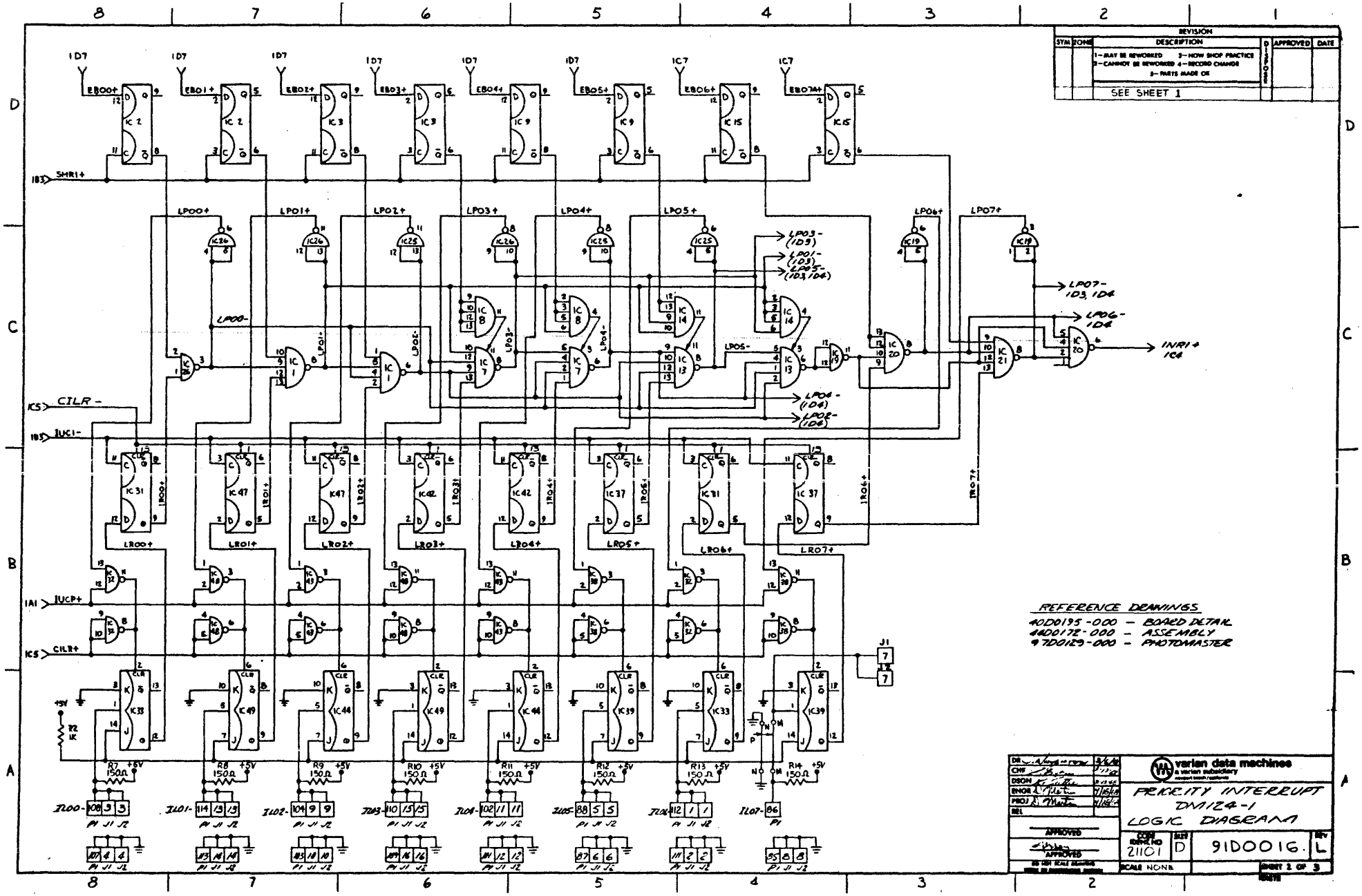
SCALE			SHEET 8.0 OF

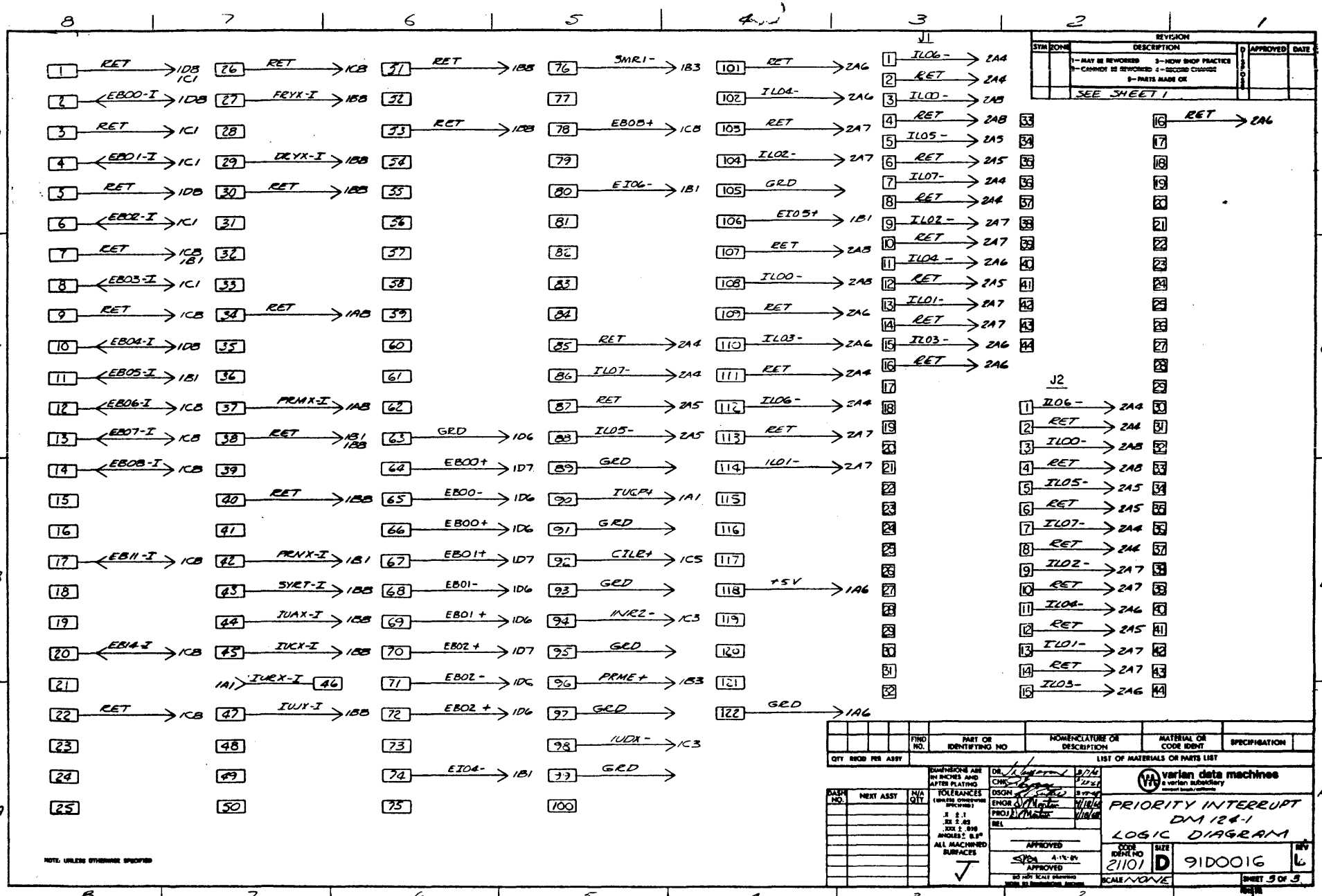

4
3
2
1
D
C
B
A
7.0 MR00-1
8.0 IR00+
B4
74H10
LP00-
E5
7404
LP00+
8.0
LP01-
10.0
MR01-
IR01+
LP01-
LP01+
LP02-
MR02-
IR02+
B5
74H20
LP02-
LP02+
3001
D3
LPZ1-2
MR03-
IR03+
C5
LP03-
LP03+
D4
74H11
LP04-
LPZ2-2
MR04-
IR04+
D5
LP04-
LP04+
E4
74H21
LP05-
MR05-
IR05+
LP05-
LP05+
LPZ3-2
LPZ5-
LP06-
MR06-
IR06+
LP06+
74H04
E3
LP07+
LP07-
MR07-
IR07+
+5V
R11
1K
94
INR2-
A5
INR1+
INTERRUPT PRIORITY LOGIC
CODE IDENT NO. 21101
SIZE C
DWG NO 91C0454
REV A
SCALE
SHEET 9.0 OF


LPO1-
LPO3-
LPO5-
LPO7-
LPO2-
LPO6-
LPO4-
74H20
A5
A4
A4
AOXX+
A1XX+
A2XX+
7438
A2
128-001
EBO1-I
EBO2-I
EBO3-I
+5V
R12
1K
P1
74
EIO4-
EBO4-I
R13
1K
7404
B2
106
EIO5+
EBO5-I
R14
1K
80
EIO6-
EBO7-I
EBO6-I
P
R
S
FRYX+
27
FRYX-I
B1
74H00
E1
74H04
E3
IUCP+
90
IAEX+
IUAX+
6.0
74H11
D4
IURM+
PRMY-
R16 1KΩ
1/2W
R15
150Ω
1/2W
37
PRMX-I
3001
D3
PRMEX+
PRMX+
IURX-I
46
PRME+
PRNX-I
42
INRI+
9.0
E3
INRI-
F3
IUDX-
98
F1
74H74
IUDX-
IURM-
PRIUR-
IUC2-
PLUP1+
6.0
PRME+
6.0
E2
IUC2-
IUCX+
45
IUCX-I
B2
C24 N.U.
7437
IUC1-
8.0
INTERRUPT REQUEST LOGIC
CODE IDENT NO.
21101
SIZE
C
DWG NO
9IC0454
REV
A
SCALE
SHEET 10.0 OF



6. SYMBOL □ <XXXX> DEPICTS BI-DIRECTIONAL FUNCTION FLOW.
5. PINS 63, 89, 91, 93, 95, 97, 99 & 105 ARE GRD.
4. POWER DISTRIBUTION TO IC 16, 33, 39, 44 & 49 PIN 4 = +5V, PIN 11 = GND.
3. POWER DISTRIBUTION TO IC'S: PIN 14 = +5V, PIN 7 = GND, (EXCEPTIONS NOTE 4).
2. ALL RESISTORS ARE 1/4W ±5%.
1. THE SYMBOLS XXY ——→ AND ←—— INDICATE A SIGNAL SOURCE AND FLOW LOCATION CODE. THE FIRST DIGIT INDICATES SHEET NO., THE LETTER A HORIZONTAL AND THE SECOND DIGIT A VERTICAL ZONE.


REVISION
SEE SHEET 1
REFERENCE DRAWINGS
40D0195-000 - BOARD DETAIL
44D0172-000 - ASSEMBLY
97D0129-000 - PHOTOMASTER
varian data machines
PRIORITY INTERRUPT
DMI24-1
LOGIC DIAGRAM
91D0016.
SCALE NONE
SHEET 2 OF 3


1 RET → 1D8 1C1
2 EB00-I → 1D8
3 RET → 1C1
4 EB01-I → 1C1
5 RET → 1D8
6 EB02-I → 1C1
7 RET → 1C8 1B1
8 EB03-I → 1C1
9 RET → 1C8
10 EB04-I → 1D8
11 EB05-I → 1B1
12 EB06-I → 1C8
13 EB07-I → 1C8
14 EB08-I → 1C8
15
16
17 EB11-I → 1C8
18
19
20 EB14-I → 1C8
21
22 RET → 1C8
23
24
25
26 RET → 1C8
27 FRYX-I → 1B8
28
29 DRYX-I → 1B8
30 RET → 1B8
31
32
33
34 RET → 1A8
35
36
37 PRMX-I → 1A8
38 RET → 1B1 1B8
39
40 RET → 1B8
41
42 PRNX-I → 1B1
43 SYET-I → 1B8
44 IUAX-I → 1B8
45 IUCX-I → 1B8
1A1 IUAX-I 46
47 IUJX-I → 1B8
48
49
50
51 RET → 1B8
52
53 RET → 1D8
54
55
56
57
58
59
60
61
62
63 GRD → 1D6
64 EB00+ → 1D7
65 EB00- → 1D6
66 EB00+ → 1D6
67 EB01+ → 1D7
68 EB01- → 1D6
69 EB01+ → 1D6
70 EB02+ → 1D7
71 EB02- → 1D6
72 EB02+ → 1D6
73
74 EI04- → 1B1
75
76 SMR1- → 1B3
77
78 EB08+ → 1C8
79
80 EI06- → 1B1
81
82
83
84
85 RET → 2A4
86 IL07- → 2A4
87 RET → 2A5
88 IL05- → 2A5
89 GRD →
90 IUCP4 → 1A1
91 GRD →
92 CILR+ → 1C5
93 GRD →
94 INR2- → 1C3
95 GRD →
96 PRME+ → 1B3
97 GRD →
98 IUDX- → 1C3
99 GRD →
100
101 RET → 2A6
102 IL04- → 2A6
103 RET → 2A7
104 IL02- → 2A7
105 GRD →
106 EI05+ → 1B1
107 RET → 2A8
108 IL00- → 2A8
109 RET → 2A6
110 IL03- → 2A6
111 RET → 2A4
112 IL06- → 2A4
113 RET → 2A7
114 IL01- → 2A7
115
116
117
118 +5V → 1A6
119
120
121
122 GRD → 1A6
J1
1 IL06- → 2A4
2 RET → 2A4
3 IL00- → 2A8
4 RET → 2A8
5 IL05- → 2A5
6 RET → 2A5
7 IL07- → 2A4
8 RET → 2A4
9 IL02- → 2A7
10 RET → 2A7
11 IL04- → 2A6
12 RET → 2A5
13 IL01- → 2A7
14 RET → 2A7
15 IL03- → 2A6
16 RET → 2A6
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
J2
1 IL06- → 2A4
2 RET → 2A4
3 IL00- → 2A8
4 RET → 2A8
5 IL05- → 2A5
6 RET → 2A5
7 IL07- → 2A4
8 RET → 2A4
9 IL02- → 2A7
10 RET → 2A7
11 IL04- → 2A6
12 RET → 2A5
13 IL01- → 2A7
14 RET → 2A7
15 IL03- → 2A6
16 RET → 2A6
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
SEE SHEET 1
REVISION
SYM ZONE DESCRIPTION APPROVED DATE
1-MAY BE REWORKED 3-NEW SHOP PRACTICE
2-CANNOT BE REWORKED 4-RECORD CHANGE
5-PARTS MADE OK
NOTE: UNLESS OTHERWISE SPECIFIED
FIND NO. PART OR IDENTIFYING NO NOMENCLATURE OR DESCRIPTION MATERIAL OR CODE IDENT SPECIFICATION
QTY REQD PER ASSY LIST OF MATERIALS OR PARTS LIST
DASH NO. NEXT ASSY N/A QTY
DIMENSIONS ARE IN INCHES AND AFTER PLATING
TOLERANCES
ALL MACHINED SURFACES
DR
CHK
DSGN
ENGR
PROJ
REL
APPROVED
APPROVED
DO NOT SCALE DRAWING
varian data machines a varian subsidiary
PRIORITY INTERRUPT DM 124-1 LOGIC DIAGRAM
CODE IDENT NO 21101
SIZE D
91D0016
REV L
SCALE NONE
SHEET 5 OF 5

BUFFER INTERLACE CONTROLLER

an option for the

Varian Data Machines

Computer Systems

Specifications are subject to change without notice. Address comments regarding this document to Varian Data Machines, Publications Department, 2722 Michelson Drive, Irvine, California, 92664.

varian data machines / a varian subsidiary
2722 michelson drive / p.o. box e / irvine / california / 92664

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98 A 9902 116

April 1975

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MAINTENANCE

SECTION 6
MNEMONICS

LIST OF ILLUSTRATIONS

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SECTION 1
GENERAL DESCRIPTION

The Buffer Interlace Controller (BIC) is a special-purpose hardware option for use with Varian computer systems. This manual is divided into six sections:

- Features and specifications
- Installation and interconnection
- Operation
- Theory of operation
- Maintenance
- Mnemonics list

Volume 2 of this manual is assembled when the hardware is shipped and contains engineering documents such as logic diagrams, parts list, and installation drawings.

There are two versions of the BIC available. One version (without key bits) is for systems that do not have the memory map option and the other version (with key bits) is for systems that do have the memory map option.

The function of the BIC is to free the processor to perform other program functions during block word transfers between memory and peripheral controllers. Cycle-stealing trap requests inhibit the processing of a stored program for only the memory cycle required to transfer one word of data between memory and a peripheral controller. Operation register contents are not changed by the transfer, thus freeing the processor to execute an instruction from the stored program between successive data word transfers.

The BIC will perform DMA transfers at the peripheral device rate up to a maximum rate defined as follows:

$$R_{max} = \frac{1}{\frac{1}{R_{CPU\ max}} + T_{IUCX}}$$

where: R_{max} is the maximum rate through a BIC (words/second)
R_{CPU} is the maximum DMA rate for the processor (words/second)
T_{IUCX} is the period of interrupt clock (seconds)

As an example, the maximum DMA rate for a Varian 70 series computer with core memory and a 990 nanosecond interrupt clock period is 361,800 words/second. The maximum rate through the BIC is then:

$$R_{max} = \frac{1}{\frac{1}{361{,}800} + (990 \times 10^{-9})} = 266{,}383 \text{ words/second}$$

The BIC monitors trap requests initiated by the peripheral controllers.

Up to ten peripheral controllers can be connected to one BIC. Using standard I/O device addressing, a computer system can include up to four BICs.

The BIC is considered to be an I/O controller. Priorities for optional controllers having trap or interrupt capabilities are established by the order of their placement in the priority chain. The BIC is a system priority device; however the peripheral devices connected to it have no priority of their own.

Table 1-1 lists the BIC specifications.

Table 1-1. BIC Specifications

Parameter	Description
Organization	Contains input receivers and output drivers, two 16-bit address registers, a 4-bit key register, and a sequence control circuit
Control capability	Up to ten peripheral controllers
I/O transfer rate	Synchronized to peripheral device rate
I/O signal limits (rise/fall)	Minimum 10 nanoseconds; maximum 100 nanoseconds
Logic levels (internal)	High = +2.4 to +5.0V dc Low = 0 to +0.4V dc
Logic levels (I/O bus)	High = +2.8 to +3.6V dc Low = 0 to +0.5V dc
Size	Contained on one 7-3/4-by 12-inch (19.7 x 30.3 cm) printed-circuit board

(continued)

Table 1-1. BIC Specifications *(continued)*

Parameter	Description
Interconnection	Interfaces with I/O cable through backplane connector; connects to peripheral controllers through the backplane connector or through a cable
Connectors	One 122-terminal card-edge connector (mates with female connector at backplane) and two 44-terminal card-edge connectors (each mates with a 44-terminal connector on B cable for special configurations)
Power	+5V dc at 0.6A
Operating environment	0 to 50 degrees C; 10 to 90 percent relative humidity without condensation

SECTION 2
INSTALLATION

The BIC has been packed and inspected to ensure its arrival in good working order. To prevent damage, take care during unpacking and handling. Check the shipping list to ensure that all equipment has been received. Immediately after unpacking, inspect the equipment for shipping damage. If damage exists:

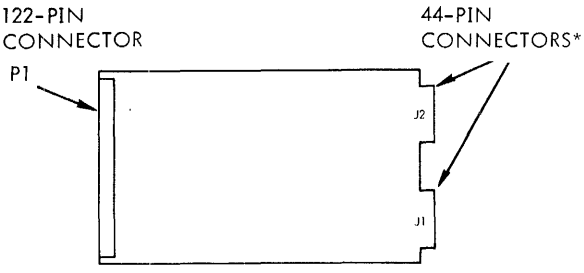
- Notify the transportation company
- Notify Varian Data Machines
- Save all packing material

2.1 PHYSICAL DESCRIPTION

The BIC circuits are contained on a single printed-circuit (PC) board (p/n 44P0689). As illustrated in figure 2-1, the board contains three connectors P1, J1, and J2. Connectors J1 and J2 are wired in parallel and contain the peripheral control lines. Connector P1 also contains the same peripheral control lines as well as all I/O bus control signals for the BIC. Connectors J1 and J2 are used for special configurations.

2.2 INTERCONNECTION

When two or more BIC controllers are installed in the same chassis, the B cable signals are connected only to the controller or controllers with which each BIC communicates. There are no B cable signals between BICs. If the BIC and the peripheral controllers are installed in different chassis, the interconnection is made through the J1 and J2 connectors. Figure 2-2 illustrates BIC/peripheral interconnections.



* CONNECTORS J1 AND J2 ARE PARALLEL WIRED

VTII-1792

Figure 2-1. BIC Board (Component Side)

2.3 INTERFACE DATA

All BIC input/output signals utilize receiver/driver stages to buffer internal circuits and external lines. The BIC interfaces with the computer via the "—I" signal lines and with peripheral controllers via the "—B" signal lines listed in table 2-1. The corresponding pin number of circuit card edge connector P1 follows each signal mnemonic (see logic diagram 91C0459). Refer to section 6 for definitions of the mnemonics.

Table 2-1. BIC Inputs and Outputs

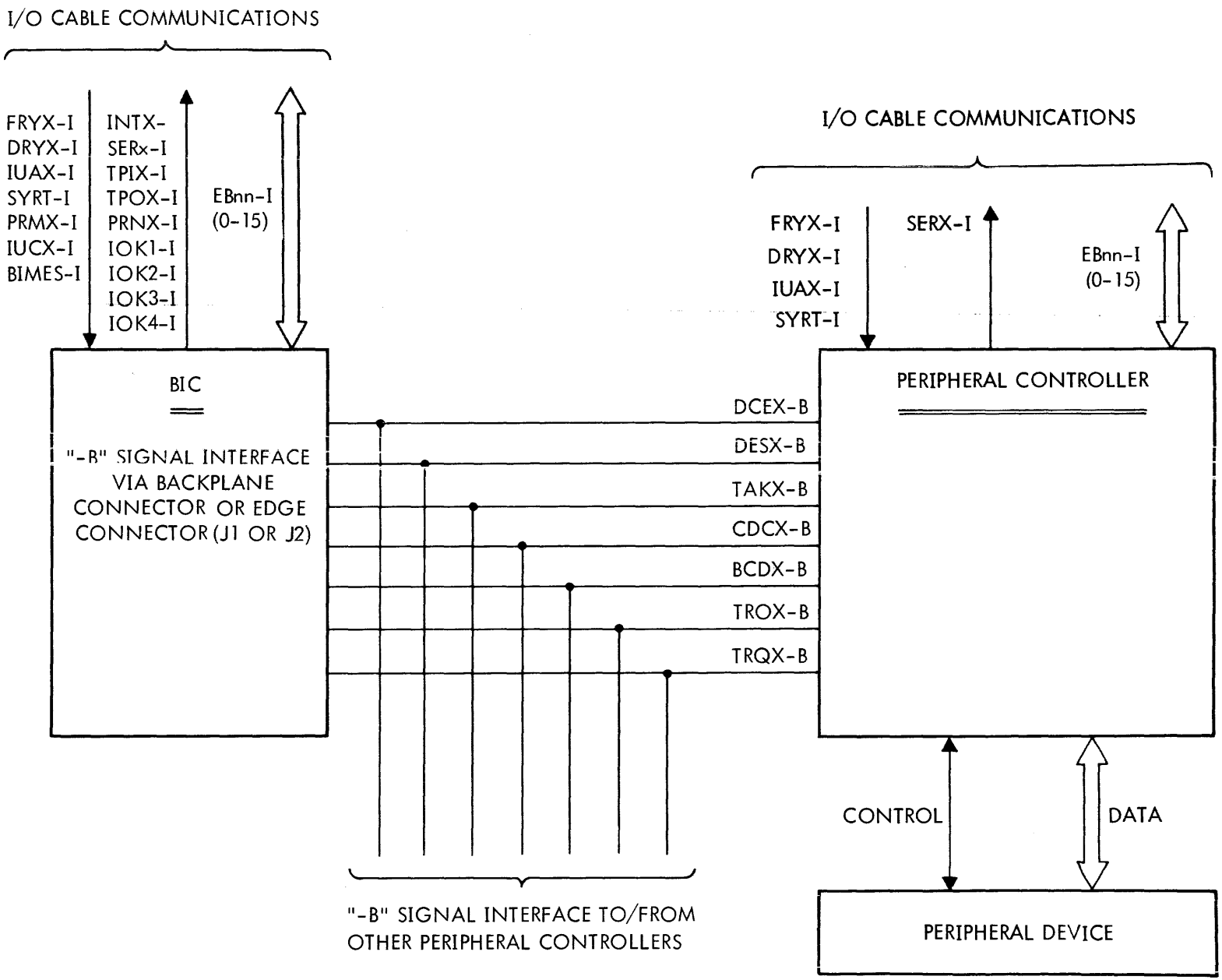
INPUTS				OUTPUTS			
BCDX-B	52	EB10-I	16	DCEX-B	56	EB12-I	18
BIMES-I	93	EB11-I	17	DESX-B	60	EB13-I	19
CDCX-B	54	EB12-I	18	EB00-I	2	EB14-I	20
DRYX-I	29	EB13-I	19	EB01-I	4,68,69	EB15-I	21
EB00-I	2	EB14-I	20	EB02-I	6,71,72	INTX-	75
EB01-I	4,65	EB15-I	21	EB03-I	8	IOK1-I	109
EB02-I	6,70	FRYX-I	27	EB04-I	10	IOK2-I	110
EB03-I	8	IUAX-I	44	EB05-I	11	IOK3-I	112
EB04-I	10	IUCX-I	45	EB06-I	12	IOK4-I	113
EB05-I	11	PRMX-I	37	EB07-I	13	PRNX-I	42
EB06-I	12	SYRT-I	43	EB08-I	14	SERX-I	31
EB07-I	13	TROX-B	50	EB09-I	15	TAKX-B	58
EB08-I	14	TRQX-B	49	EB10-I	16	TPIX-I	33
EB09-I	15			EB11-I	17	TPOX-I	35

NOTE: On systems with memory map, the BIMES-I and BTMES-I signals are floating and must be pulled up to +5 volts by adding the following jumpers:

a. On each backplane slot, pin 93 (BIMES-I) is connected to pin 73 (PRMY-I).

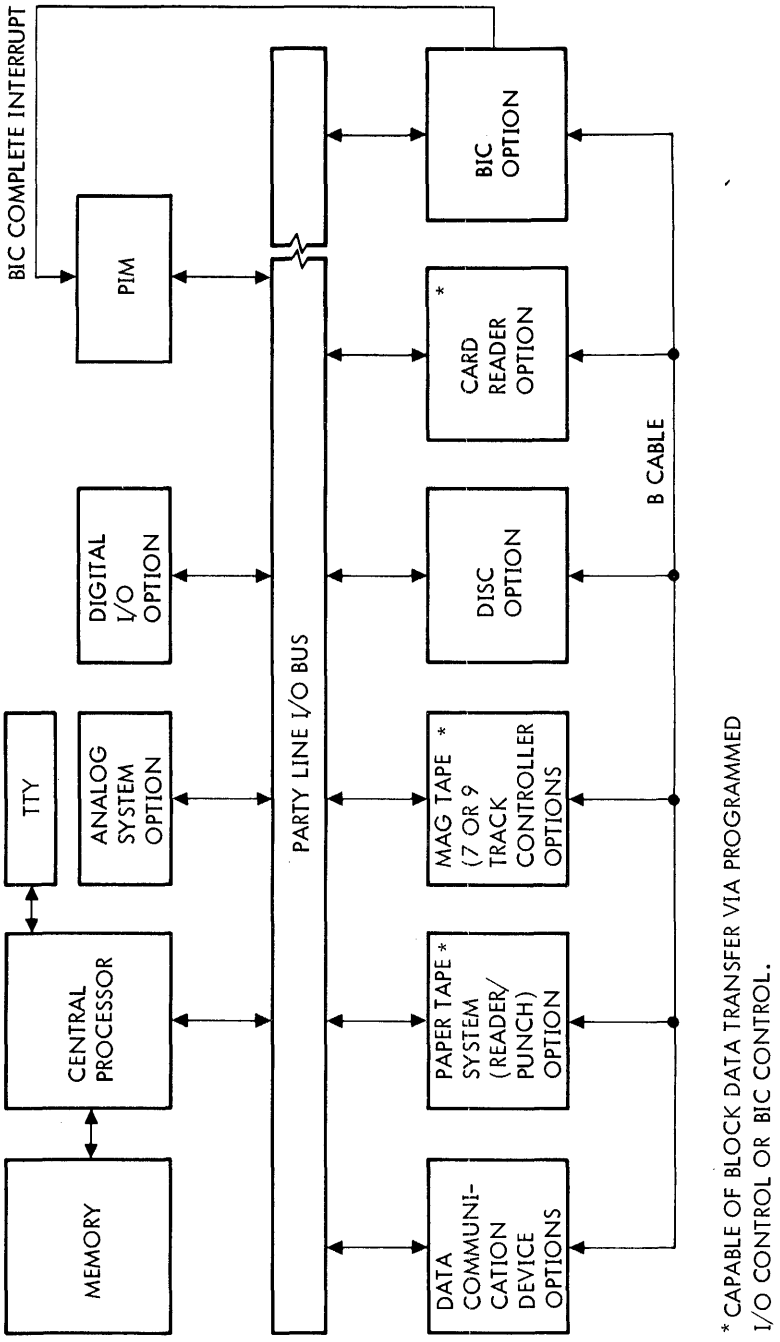
b. On each PMA/BTC backplane slot, pin 96 (BTMES-I) is connected to pin 73 (EXPU+).

Many peripheral controllers, under software control, can transfer data either by programmed I/O or via BIC control. Controllers for peripherals such as discs and drums usually are not able to transfer data via programmed I/O due to their high transfer rates. Figure 2-3 shows a computer system with peripheral controllers that operate with and without BIC. Figure 2-4 is typical interface logic.



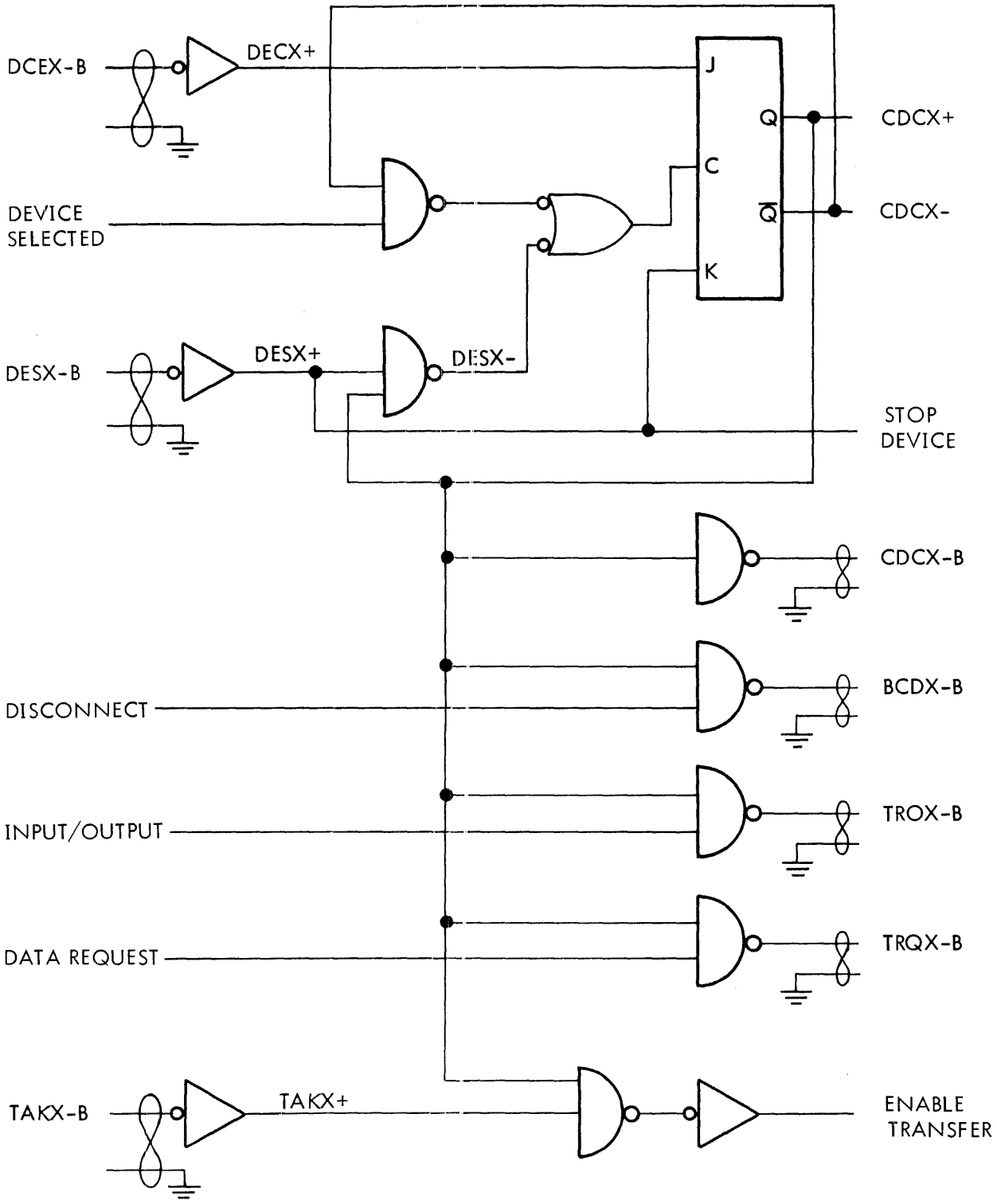
VTII-2314

Figure 2-2. BIC/Peripheral Controller Interface



VTII-340B

Figure 2-3. Interface for Peripheral Devices with and



VTII-232A

Figure 2-4. Typical B Cable Interface Logic

SECTION 3
OPERATION

The BIC has no operating controls or indicators. It operates under program control.

3.1 I/O INSTRUCTIONS

The BIC responds to the instructions listed in table 3-1. Two device addresses are assigned to each BIC to differentiate functions directed by the I/O instruction. Addresses 020 through 027 are reserved for BICs. Address/instruction codes in table 3-1 are for the first BIC in a system. If additional BICs are installed, the addresses shown should be incremented by two for each additional BIC (i.e., second BIC addresses should be 022 and 023).

Table 3-1. I/O Instructions

Mnemonics	Octal Code	Description
		External Control
EXC 020	100020	Activate BIC
EXC 021	100021	Initialize
EXC 0321	100321	Enable loading of key bits
		Transfer
OAR 020	103120	Load initial register from A
OBR 020	103220	Load initial register from B
OME 020	103020	Load initial register from memory
OAR 021	103121	Load final register from A
OBR 021	103221	Load final register from B
OME 021	103021	Load final register from memory
INA 020	102120	Read initial register into A
INB 020	102220	Read initial register into B
IME 020	102020	Read initial register into memory
CIA 020	102520	Read initial register into cleared A
CIB 020	102620	Read initial register into cleared B
		Sense
SEN 020	101020	Sense BIC not busy
SEN 021	101021	Sense abnormal device stop
SEN 0121	101121	Senses if BIC has been stopped due to a memory-map error

3.2 PROGRAMMING CONSIDERATIONS

The user writes the programs that use the BIC. When preparing a program for use with the BIC, the programmer first initializes then senses the status of the BIC and the selected peripheral controller. After a not-busy response is received from both the BIC and the peripheral controller, the BIC address registers are loaded with the initial and final memory addresses of the block of data to be transferred, a BIC activate enable instruction is placed on the I/O cable, and the transfer is started. Although the program requires loops for use with sense instructions and to handle abnormal conditions, transfer of the data block is accomplished by the BIC without further program instructions.

The key bit register (for memory map option) is loaded by first issuing the "Enable (loading of) Key Bit Register" instruction (0100321) followed by one of the "Load Final Register" instructions (0103021, 0103121, 0103221).

3.3 SAMPLE PROGRAM

Table 3-2 shows a typical service routine for the BIC, a Teletype paper tape punch operation under BIC control. Using DAS symbols with corresponding machine language

Table 3-2. Typical Service Routine

Memory Location	Octal Code	Label	Operation	Variable Field	Comments
001000			,ORG	,01000	
001000	101020	BIC0	,SEN	,020,BIC1	CK BIC NOT BUSY
001001	001007 R				
001002	100401		,EXC	,0401	INIT TTY
001003	100021		,EXC	,021	INIT BIC
001004	005000		,NOP	,	
001005	001000		,JMP	,*-3	

(continued)

Table 3-2. Typical Service Routine *(continued)*

Memory Location	Octal Code	Label	Operation	Variable Field	Comments
001006	001002 R				
001007	101101	BIC1	,SEN	,0101,BIC2	CK TTY WRITE READY
001010	001014 R				
001011	005000		,NOP	,	
001012	001000		,JMP	,*-3	
001013	001007 R				
001014	103120	BIC2	,OAR	,020	SET BIC I REG
001015	103221		,OBR	,021	SET BIC F REG
001016	100020		,EXC	,020	ACTIVATE BIC
001017	100101		,EXC	,0101	CONNECT WRITE REG
001020	101020		,SEN	,020,BIC3	CK BIC NOT BUSY
001021	001025 R				
001022	005000		,NOP	,	
001023	001000		,JMP	,*-3	
001024	001020 R				
001025	101021	BIC3	,SEN	,021,BIC5	CK ABN STOP
001026	001032 R				
001027	007400		,ROF	,	
001030	102520	BIC4	,CIA	,020	INPUT BIC I REG
001031	000000		,HLT	,	
001032	007401	BIC5	,SOF	,	SET ABN FLAG
001033	001000		,JMP	,BIC4	
001034	001030 R				
	000000		,END	,	

octal codes, the program covers memory locations 01000 through 01034.

Once the program is loaded, the operator must insert the initial punch buffer address into the A register and the final address into the B register for each run. When started, the program will:

a. initialize the BIC and Teletype punch

b. initiate the data transfer

c. read the contents of the BIC initial register into the A register at the completion of the transfer

d. set the overflow indicator if the termination was abnormal

e. halt

The punch buffer must contain only ASCII characters. The first character is 0222 (punch on) and the last is 0224 (punch off).

SECTION 4
THEORY OF OPERATION

The BIC is functionally divided into address registers and a sequence control circuit (figure 4-1). A functional description of these circuits is provided in the following paragraphs.

4.1 ADDRESS REGISTERS

The two address registers contain the memory locations of output or input data, depending on the I/O instruction. The initial register stores the address of the first input or output word, and is incremented during each data-word transfer. When the block transfer is complete, the initial register contains the address + 1 of the last data word to be transferred.

The final register stores the address of the last word to be transferred. Unless the peripheral device is abnormally stopped, the address in the final register will be one less than the address in the initial register when the block transfer is complete. When the initial and final registers reach comparison, the block word transfer is complete.

The key-bit register stores the four key bits that are used with the memory map. The key-bit register is not used on systems without the memory map. The enable instruction sets a flip-flop which directs the data being transferred by a load (of final register) instruction, into the key-bit register. The flip-flop is reset when the transfer is complete.

4.2 SEQUENCE CONTROL

The sequence control circuit generates the control signals which coordinate address and data transfer between the processor, BIC, and the peripheral controllers. The data are not routed through the BIC but are directly transferred between the peripheral controller and memory.

Under program control, the processor senses that the BIC is not busy and prepares the BIC to receive the initial and final data addresses. The processor then senses that the selected peripheral controller is not busy and loads the initial and final registers and the key register. The BIC is then activated and the peripheral controller is started. The BIC then assumes control of the data transmission, allowing the processor operational registers to be used by the program for other functions.

Data transfer is accomplished between memory and the peripheral controller via the I/O bus. The BIC counts the words transferred and when the data block transfer is complete, disconnects the peripheral controller and assumes a not-busy state. Data transfer may also be terminated upon request from the peripheral controller.

4.3 OPERATING SEQUENCE

The following paragraphs describe the sequence of operations of the BIC. Refer to the block diagram (figure 4-1), the timing diagram (figure 4-2), and the logic diagram 91C0459 in volume 2.

4.3.1 Initial Conditions

The processor senses the BIC for a not-busy condition. The sense instruction places the BIC device address and a function code on the I/O bus. The BIC responds with a low SERX-I if it is not busy (CDCX-B low). The processor then executes the initialize instruction which generates a low INIT- which prepares BIC for receiving the initial and final addresses of the block data to be transferred.

The initial register is loaded from the I/O bus when data ready DRYX—I returns high and LIxx— is low.

The final register is loaded from the I/O bus when DRYX—I returns high, and LFRX + is high.

4.3.2 Device Selection

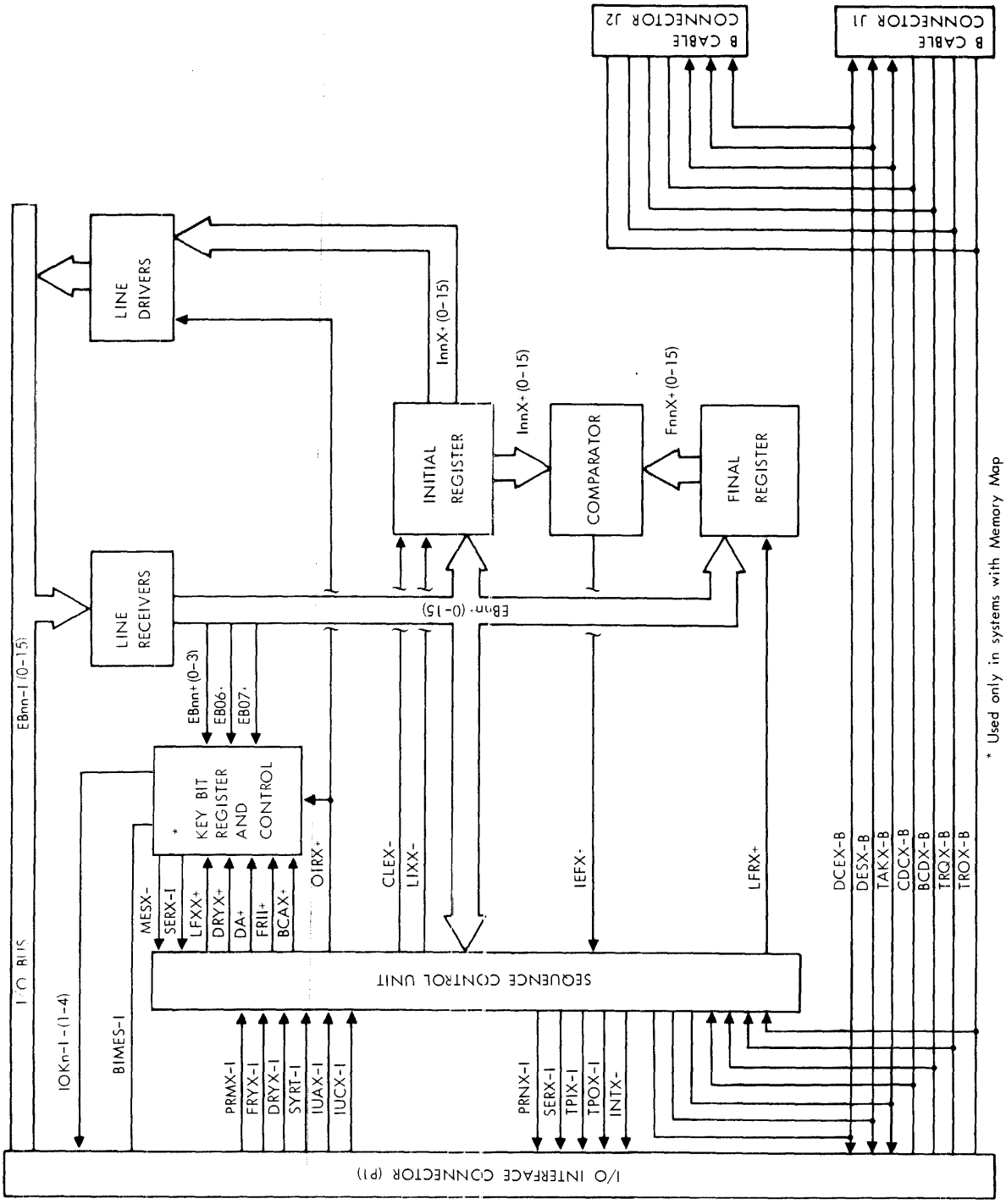
The processor executes the activate BIC instruction which causes DCEX-B to go low. This signal is sent to all peripheral controllers connected to the BIC. The processor then executes an instruction to select a peripheral device. This instruction with DCEX-B low, connects the selected device to the BIC and starts the device.

The connected peripheral controller sends a low CDCX-B to the BIC causing DCEX-B to go high, thus disabling the selection of any other peripheral controllers. When CDCX-B goes low, the connected peripheral controller also selects the state of TROX-B. When data is to be transferred to memory, a high TROX-B is sent. If data is to be transferred to memory, a low TROX-B is sent.

4.3.3 Data Address

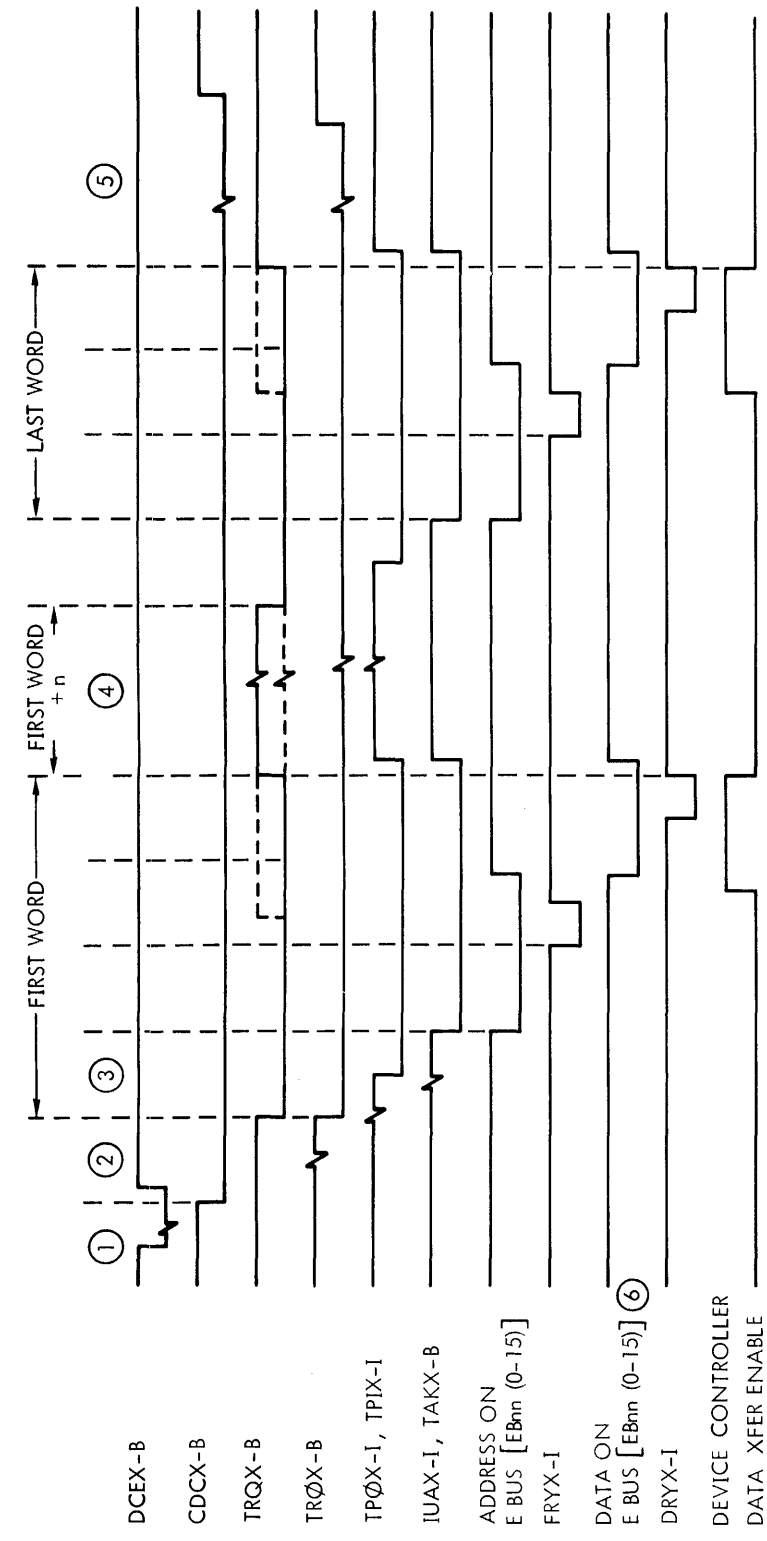
When the connected peripheral controller is ready for the data transfer, it sends a low TRQX-B to the BIC. The BIC then sends a TPIX-I or low TPOX-I to the processor, depending on the state of TROX-B.

When the processor is ready for the data transfer, it sends a low IUAX—I to the BIC. IUAX—I going low generates a low TAKX—B which is sent to the peripheral controller to initiate the transfer. The BIC then causes OIRX + to go high which gates the memory address, that is in the initial register plus the key bits onto the I/O bus. The connected peripheral controller is thus enabled. FRYX—I, from the processor, going high terminates the address phase of the BIC. FRYX—I going high causes CLEX— to go high, which



VTII-2046A

Figure 4-1. BIC Block Diagram



NOTES:

1. TIMING REQUIRED TO ISSUE THE COMMAND TO CONNECT THE DEVICE.
2. TIME REQUIRED FOR DEVICE TO REQUEST FIRST DATA TRANSFER AFTER STARTING.
3. TIME REQUIRED TO SERVICE CURRENT AND/OR HIGHER PRIORITY REQUESTS FOR I/O ACCESSES.
4. SIGNAL TRQX-B MAY BE BROUGHT LOW (TRUE) AGAIN, AS EARLY AS THE TRAILING EDGE OF DRYX-I. HOWEVER, SIGNAL TRQX-B MUST HAVE BEEN HIGH FOR AT LEAST 50 NANOSECONDS BEFORE GOING LOW.
5. END OF DATA BLOCK. SIGNAL CDCX MAY REMAIN HIGH BETWEEN BLOCKS.
6. INCLUDES KEY BITS IF PRESENT [IOKn-I (0-3)].
7. FOR DMA TIMING REFER TO THE APPLICABLE SYSTEM HANDBOOK.

Figure 4-2. BIC Trap Sequence Timing

causes the initial register to be incremented to the next memory address.

4.3.4 Data Transfer

The data transfer may be an output from or an input to the processor. For output, the processor places the data on the I/O bus, and the data is strobed into the peripheral controller by DRYX-I going high. For input, the peripheral controller places the data on the I/O bus when FRYX-I goes high and removes the data when DRYX-I goes high. BIC keeps TAKX-B low until the end of the transfer when IUAX-I goes high.

4.3.5 Transfer Termination

When the contents of the initial and final registers become equal, the comparator circuit generates a high IEFX—. This creates a low DESX—B which is sent to the peripheral controller. The peripheral controller then causes CDCX--B to go high. This causes the BIC to assume a not busy state. The transfer of data is thus terminated.

When an abnormal device stop occurs, the peripheral controller terminates the transfer without regard to the contents of the initial and final registers. The peripheral controller generates a low BCDX—B. This causes a low DESX—B to be sent to the peripheral controller. The peripheral controller responds with a high CDCX—B. This causes the BIC to assume a not busy state. The transfer of data is thus terminated. After an abnormal device stop, the processor can read the contents of the initial register to determine the number of words that were transferred. The number in the initial register will be the address of the last word transferred plus one.

An abnormal device stop can occur as a result of any of the following situations: the length of the data block is unknown, and the device has detected the end of the data; the peripheral controller has detected an invalid operation of the device; the processor has issued an instruction to stop the operation of the peripheral device.

Another abnormal stop is created when an error is detected by the memory map during a BIC operation. The error causes BIMES—I to go low. This causes a low DESX--B to be sent to the peripheral controller. The peripheral controller responds with a high CDCX—B. This causes the BIC to assume a not busy state. The transfer of data is then terminated.

SECTION 5
MAINTENANCE

Maintenance personnel should be familiar with the contents of this manual before attempting to troubleshoot the BIC. The Varian MAINTAIN II test program system (Test Programs Manual, 98 A 9952 06x)* contains a BIC test program used to test various phases of the BIC operation. Further diagnosis can then be made by referring to this manual.

5.1 TEST EQUIPMENT

The following test equipment and tools are recommended for maintenance:

a. Oscilloscope, Tektronix type 547 with dual-trace plug-in unit, or equivalent.

b. Multimeter, Triplett type 630 or equivalent.

c. Soldering iron, 39-watt pencil type.

d. Card extender VDM p/n 44P0540.

*The x at the end of the document number is the revision number and can be any digit 0 through 9.

5.2 CIRCUIT-COMPONENT IDENTIFICATION

All reference designations used in the logic diagram appear on the BIC board adjacent to each component. Component part numbers can be found in the parts list in volume 2.

5.3 CIRCUIT-BOARD REPAIR

If it has been determined that circuit-board repair is required, it is recommended that the Varian Data Machines customer service department be contacted so that a new circuit board can be installed in the user's system and the faulty one returned to the factory for repairs. However, if the user decides to perform his own repairs, caution should be used so that the circuit board is not permanently damaged. Approved repair procedures should be followed such as the ones described in document IPC-R-700A prepared by the Institute of Printed Circuits.

SECTION 6
MNEMONICS

Table 6-1 provides an alphabetized list of the signal mnemonics used in the BIC.

Table 6-1. Mnemonics

Mnemonic	Description
ACEX	Activate enable. Stores activation of BIC.
ADSX	Abnormal device stop. Stores end of data from peripheral controller.
BCAX	Buffer controller activate. Stores the activation of the BIC and the peripheral controller.
BCDX	Buffer controller deactivate. Initiates termination of data transfer by the peripheral controller.
BIMES	BIC map error stop. Stores the map error indication during a BIC operation.
CARx	Carry out. Increments the next higher position of the initial register on overflow.
CDCX	Controller device connected. Indicates that the peripheral controller to be connected is connected.
CLEX	Clock enabled. Enables the initial register to be incremented.
DA	Device address decode. Gates the device address from the I/O bus.
DCEX	Device connect enable. Enables the selection of a peripheral device.
DESX	Device stop. Stores the requirement to stop the peripheral device.
DRYX	Data ready. Indicates the I/O bus contains a word of data.
DSTX	Device stop enable. Stores the end of the data transfer.
EBii	E-bus bit. Address or function code bits from the I/O bus.
EKBR	Enable loading of key bit register. Gates the key bits into the key-bit register.
FRYX	Function ready. Indicates the I/O bus contains an address.
FiiX	Final register bit. Stores bit ii of the final address.
IEFX	Initial equals final. Indicates that the contents of the initial register is equal to the contents of the final register.
IFMX	Initial equals final memory. Clears the BIC active flip-flop when the contents of the initial register is equal to the contents of the final register.
INIT	Initialize. Resets BIC flip-flops to their initial condition.
INTX	Interrupt request. Used to request an interrupt when the block transfer is complete.
IOKi	Key-bit register output i to I/O bus.
IUAX	Interrupt acknowledge. Indicates that the processor is ready to send or receive data.
IUCX	Interrupt clock. Provides timing for servicing BIC.
IiiX	Initial register data bit. Stores bit ii of the initial address.
LFRX	Load final register. Loads data on I/O bus into final register.
LFXX	Load final. Gates the I/O bus contents into the key-bit register when EKBR is set.
LIXX	Load initial register. Loads data on I/O bus into initial register.
MESX	Map error stop. Indicates that there was a memory map error during a BIC operation.

(continued)

Table 6-1. Mnemonics *(continued)*

Mnemonic	Description
OIRX	Output initial register. Gates contents of initial register and key-bit register onto the I/O bus.
PLUP	Pullup voltage.
PRMX	Priority in. Gives priority to BIC.
PRNX	Priority out. Passes priority to next in line after BIC is serviced.
RIXX	Read initial register. Stores requirement of processor to read contents of initial register.
RTPD	Reset trap detect. Resets the trap request detection flip-flop.
SERX	Sense response. Indicates whether the BIC is busy.
SYRT	System reset. Generates initialize signal when SYSTEM RESET is pressed.
TAKX	Trap acknowledge. Indicates that the requirements for data transfer have been met.
TCOX	Trap command. Synchronizes trap request with interrupt clock.
TPDX	Trap request detect. Detects the peripheral controller request for a trap.
TPIX	Trap in. Indicates that the BIC is ready to transfer data to the processor.
TPOX	Trap out. Indicates that the BIC is ready to transfer data from the processor.
TROX	Trap out (from peripheral). Indicates the direction (in or out) of the data transfer.
TRQX	Trap request. Indicates that the peripheral controller is ready for a data transfer.

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE 1/4 W, 5%
2. THIS DRAWING CONSISTS OF THE FOLLOWING SHEETS: 1.0, 2.0, 3.0, 4.0, 5.0, 6.0, 7.0, 8.0, 9.0, 10.0, 11.0, 12.0, 13.0

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
R 16	
C 27	
E13	

REFERENCE DRAWINGS	
BOARD DETAIL	4000560
ARTWORK	97E0869
SOLDERMASK	97E0870
SILKSCREEN	97E0871
ASSEMBLY	4400689

DR	C. WARNER	5-29-73
CHK	[illegible]	6-7-73
DSGN	J. ZOLL	5-29-73
ENGR	[illegible]	6-21-73
APPD	[illegible]	6-21-73
APPD		

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varian data machines a varian subsidiary
2722 michelson drive, irvine, california, 92664

TITLE
LOGIC DIAGRAM-DM402
BUFFER INTERFACE CONTROLLER

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0459	H

SCALE | SHEET 1.0 OF

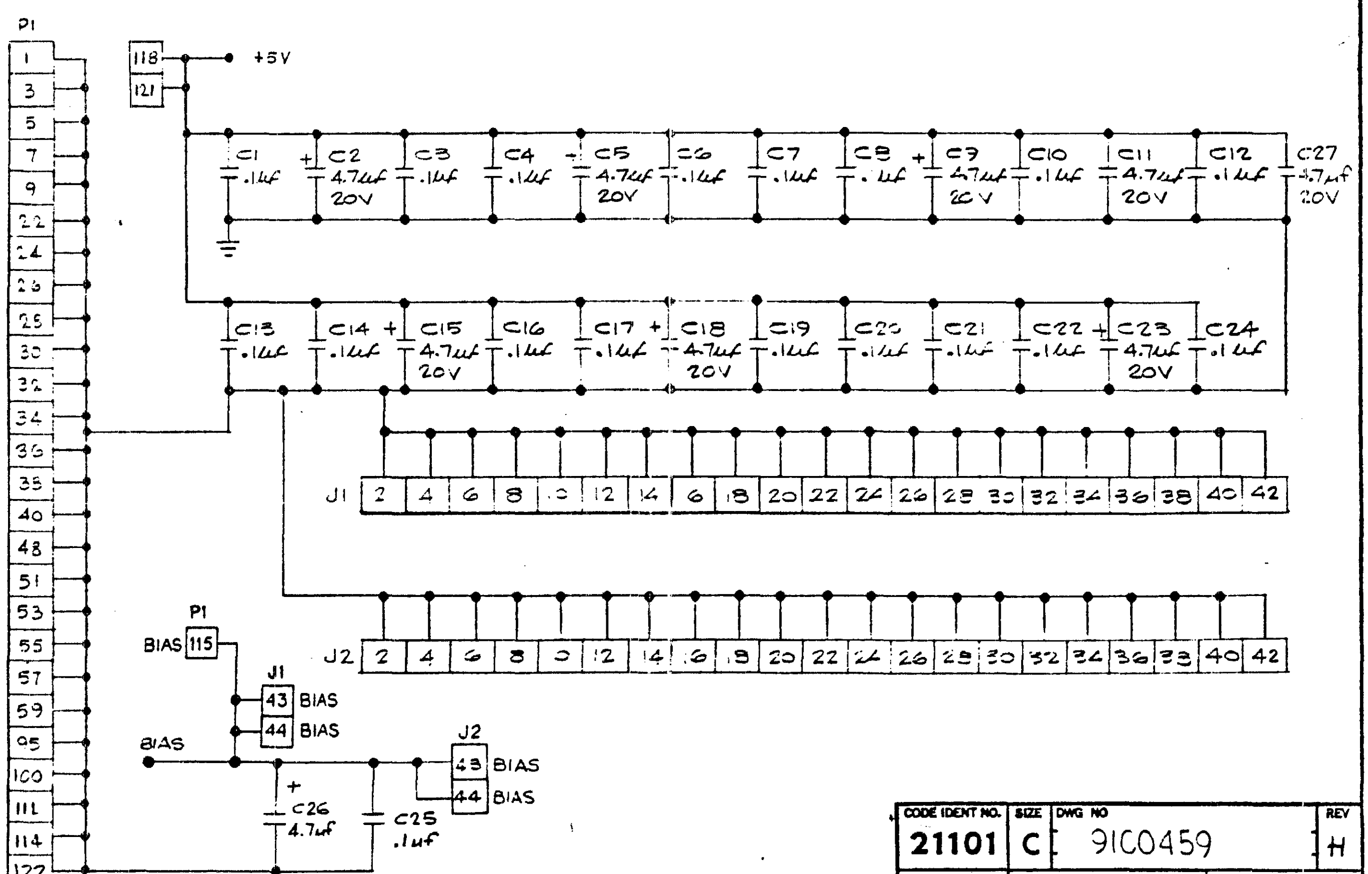
1-70 DIETZGEN-POST CLEARPRINT 100M-8

CHANGE CODE	SYM	EN	DESCRIPTION	APPROVED	DATE
	A		PRODUCTION RELEASE PER EN 82123	[signature]	6/21/73
	B	[initials]	REVISE PER EN 82554	[signature]	7/20/73
/	C	[initials]	ADDED C25 & C26 PER EN 82603	[signature]	3/26/74
/	D	[initials]	ADDED R16 - WAS N/U PER EN 82580	[signature]	5-15-74
	—	83154	ADDED DEVICE ADDRESS BLOCK AND NOTE'S 1,2 & 3 TO SHT 5.	B.B.	8/15/74
/	E	83164	F2 & 6 WAS TO SIGNAL TCEX+, THE IC AT C4 WAS 74-[illegible]	B.B.	9/15/74
	F	83218	ADDED GND TO PINS P1-43, 100, 111 & 114 SHT 2 & 4. ADDED POWER AND GND DIST. FOR ICs TO SHT 2	B.B.	8/15/74
	—	83335	SHT 2 ZONE C-3 IS WAS: 7404 IS; 74H04	B.B.	10/2/74
	G	83345	ADDED C27 AND E13	B.B.	10/2/74
/	—	83346	REVISED NOTES, PAGE 5 ZONE B3 & 4	[signature]	2-11-75
	H	83760	SH 3.0 F2-6 TO H3-12 WAS F2-6 TO F3-10	B.B.	4/21/75
—	—	83910	REVISED NOTE 1 AND 2 SH 5 AND DEVICE ADDRESS TABLE.	PSH / [signature]	9/11/75

TABLE OF CONTENTS

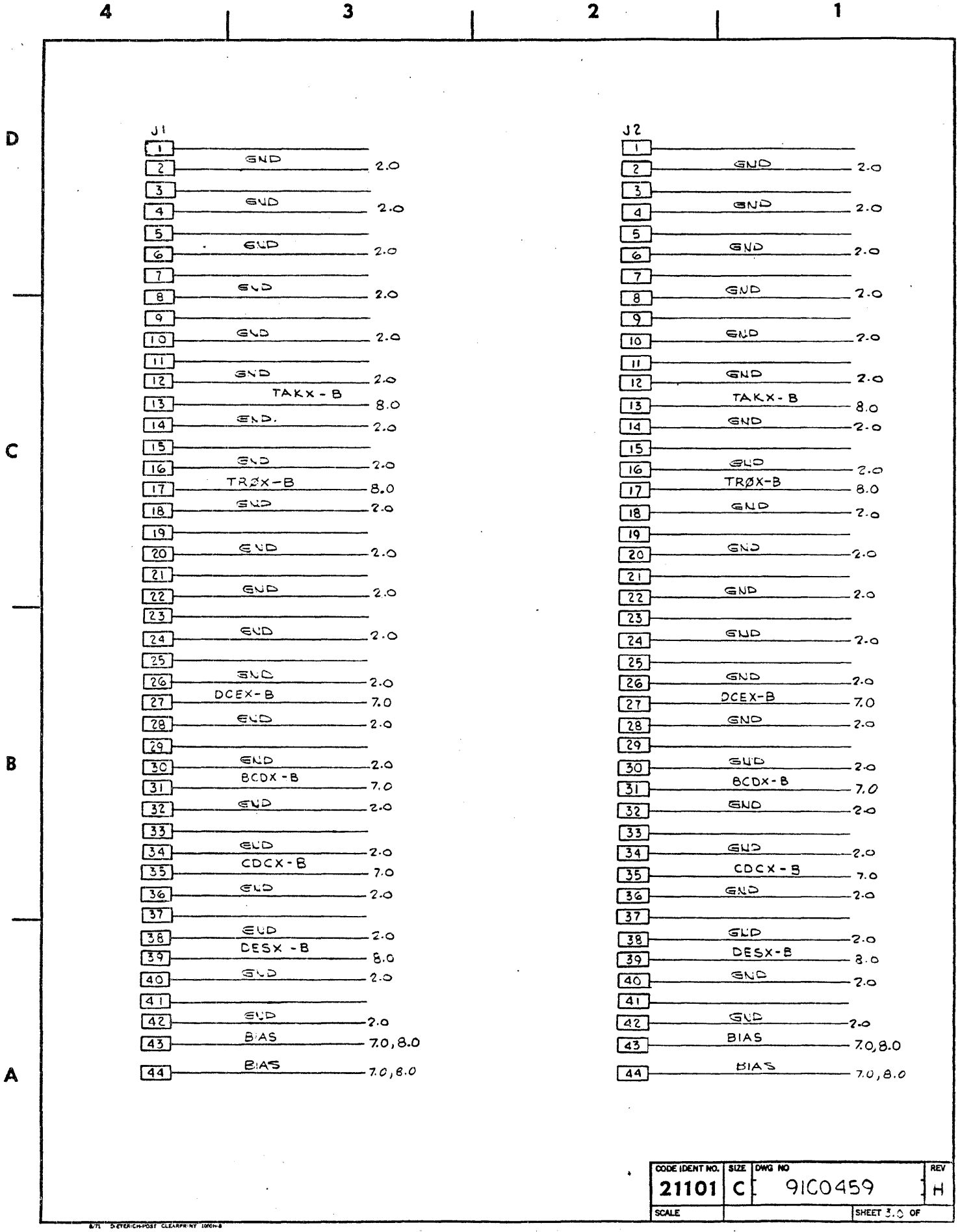
NOTE: POWER AND GROUND DISTRIBUTION

FOR 16 PIN IC PIN 16 = +5V PIN 8 = GND EXCEPT AS LISTED BELOW
FOR 14 PIN IC PIN 14 = +5V PIN 7 = GND EXCEPT AS LISTED BELOW
EXCEPTIONS:
I.C. AT F2, K4 AND E6 PIN 4 = +5 PIN 11 = GND
I.C. AT A7, B7, C7 AND D7 PIN 5 = +5 PIN 12 = GND



CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0459	H
SCALE		SHEET 2.0 OF	

DIETERICH-POST CLEARPRINT

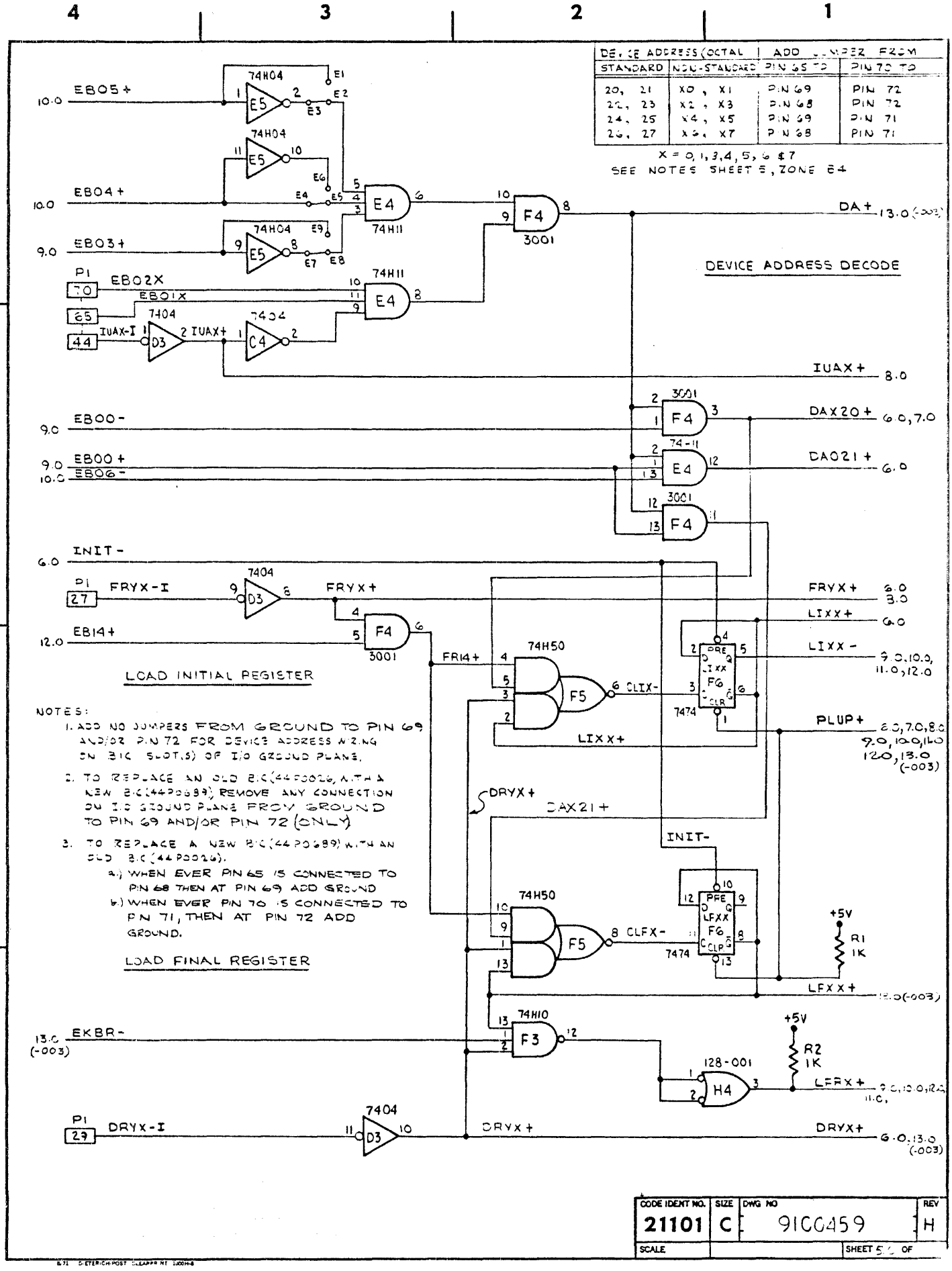


CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100459	H
SCALE		SHEET 3.0 OF	

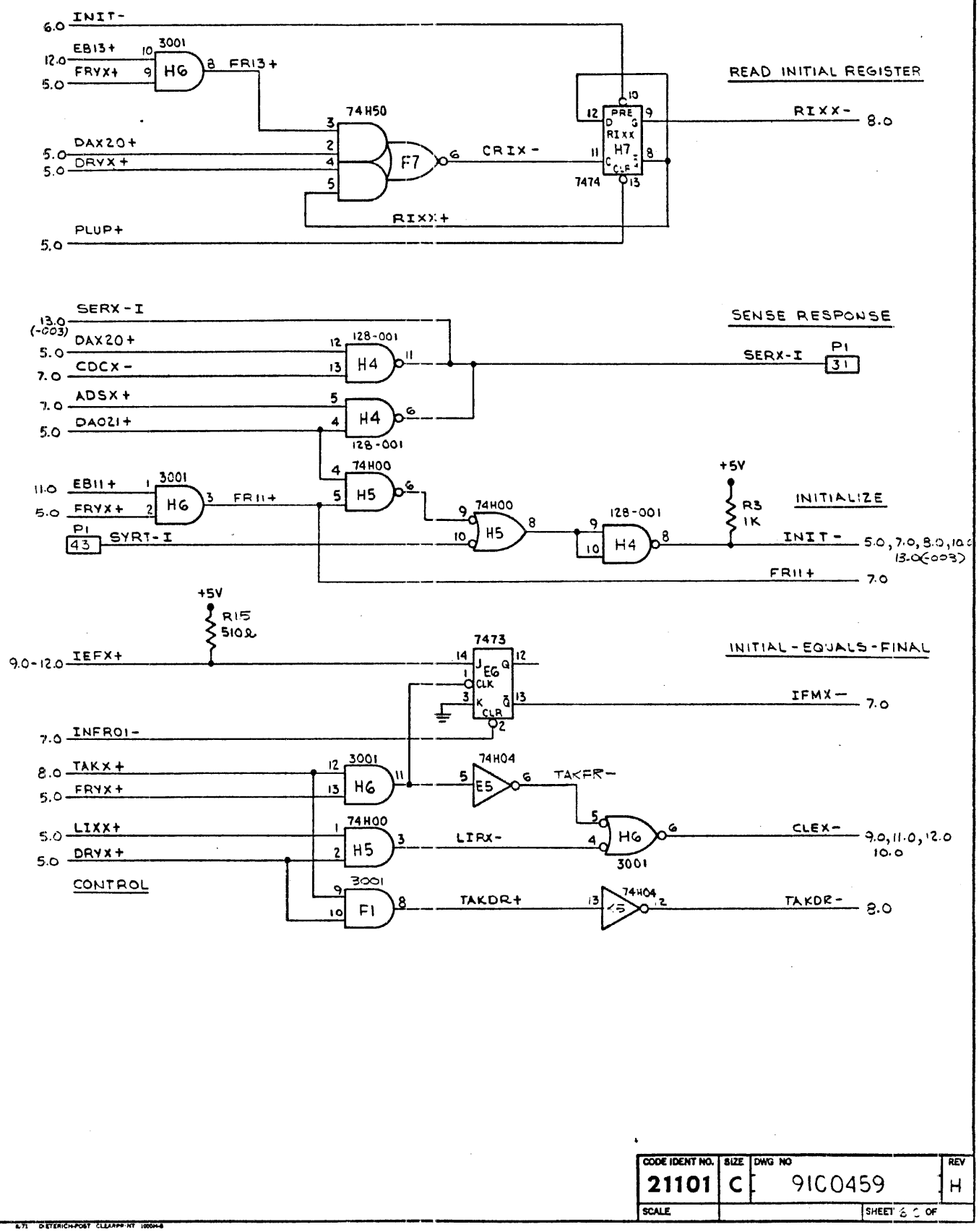
8/71 DIETERICH-POST CLEARPRINT 1000H-B

P1								
1	GND	2.0	42	PRNX-I	8.0	84		
2	EB00-I	9.0	43	SYRT-I	6.0	85		
3	GND	2.0	44	IUAX-I	5.0	86		
4	EB01-I	9.0	45	IUCX-I	7.0	87		
5	GND	2.0	46			88		
6	EB02-I	9.0	47			89		
7	GND	2.0	48	GND	2.0	90		
8	EB03-I	9.0	49	TRQX-B	8.0	91		
9	GND	2.0	50	TRØX-B	8.0	92		
10	EB04-I	10.0	51	GND	2.0	93	BIVES-I	13.0
11	EB05-I	10.0	52	BCDX-B	7.0	94		
12	EB06-I	10.0	53	GND	2.0	95	GND	2.0
13	EB07-I	10.0	54	CDCX-B	7.0	96		
14	EB08-I	11.0	55	GND	2.0	97		
15	EB09-I	11.0	56	DCEX-B	7.0	98		
16	EB10-I	11.0	57	GND	2.0	99		
17	EB11-I	11.0	58	TAKX-B	8.0	100	GND	2.0
18	EB12-I	12.0	59	GND	2.0	101		
19	EB13-I	12.0	60	DESX-B	8.0	102		
20	EB14-I	12.0	61			103		
21	EB15-I	12.0	62			104		
22	GND	2.0	63			105		
23			64			106		
24	GND	2.0	65	EB01X	5.0	107		
25			66			108		
26	GND	2.0	67			109	IØK1-I	13.0
27	FRYX-I	5.0	68	EB01+	9.0	110	IØK2-I	13.0
28	GND	2.0	69	EB01-	9.0	111	GND	2.0
29	DRYX-I	5.0	70	EB02X	5.0	112	IØK3-I	13.0
30	GND	2.0	71	EB02+	9.0	113	IØK4-I	13.0
31	SERX-I	6.0	72	EB02-	9.0	114	GND	2.0
32	GND	2.0	73	PRMY-I	8.0	115	BIAS	7.0, 80
33	TPIX-I	8.0	74			116		
34	GND	2.0	75	INTX-	8.0	117		
35	TPOX-I	8.0	76			118	+5V	2.0
36	GND	2.0	77			119		
37	PRMX-I	8.0	78			120		
38	GND	2.0	79			121	+5V	2.0
39			80			122	GND	2.0
40	GND	2.0	81					
41			82					
			83					

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0459	H
SCALE			SHEET 4 OF

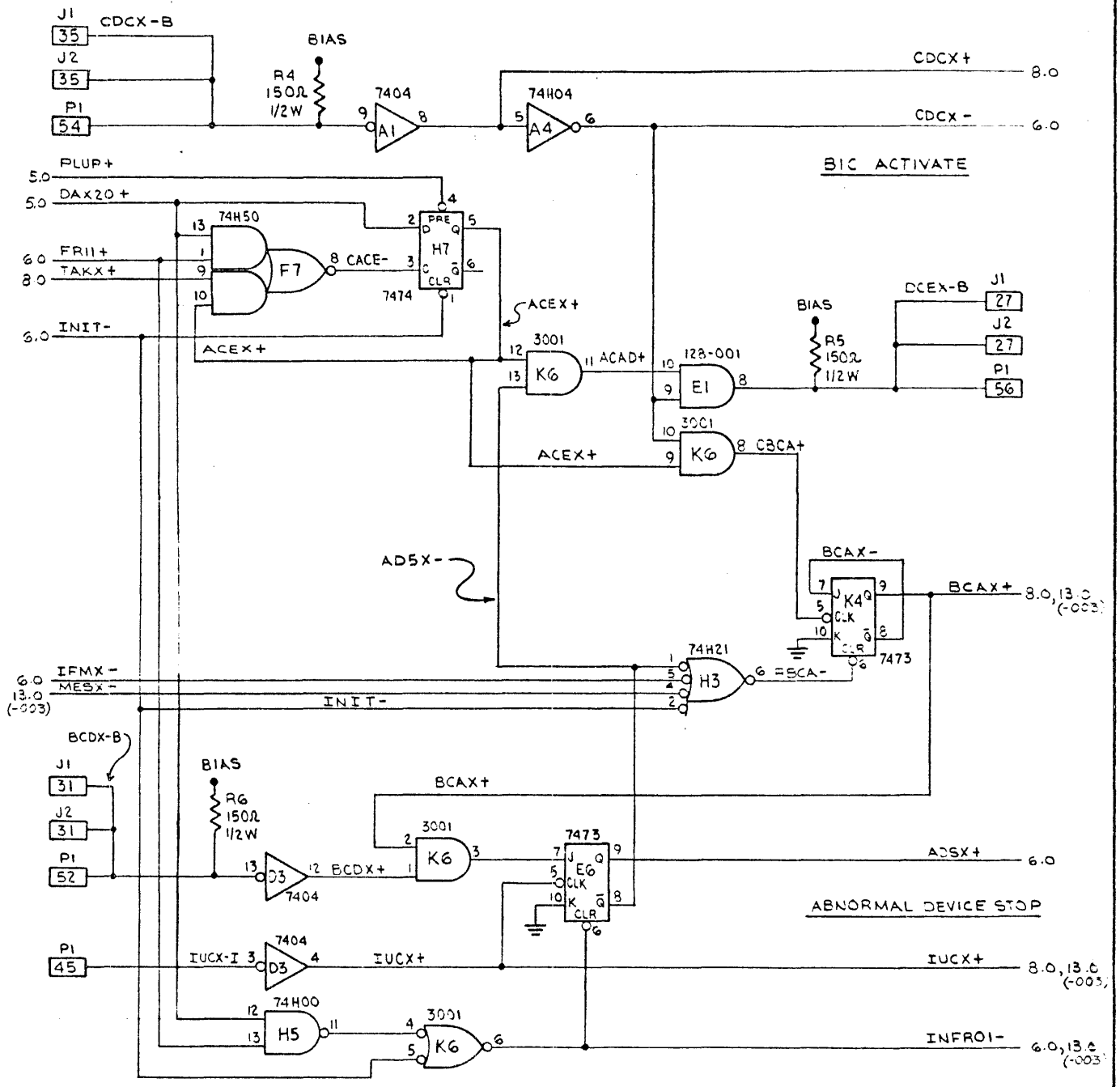


CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100459	H
SCALE			SHEET 5 OF

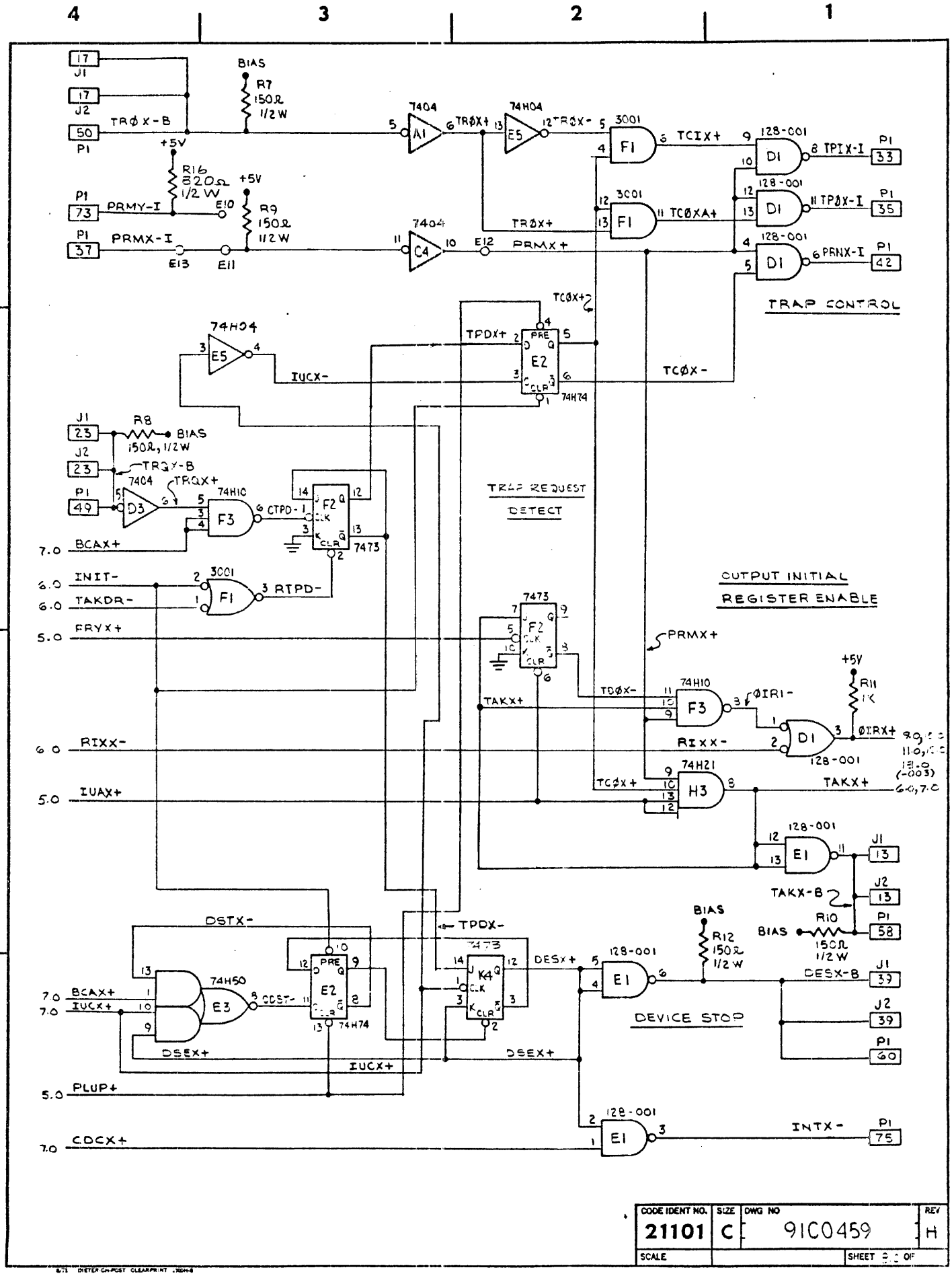


CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0459	H
SCALE		SHEET 6 OF	

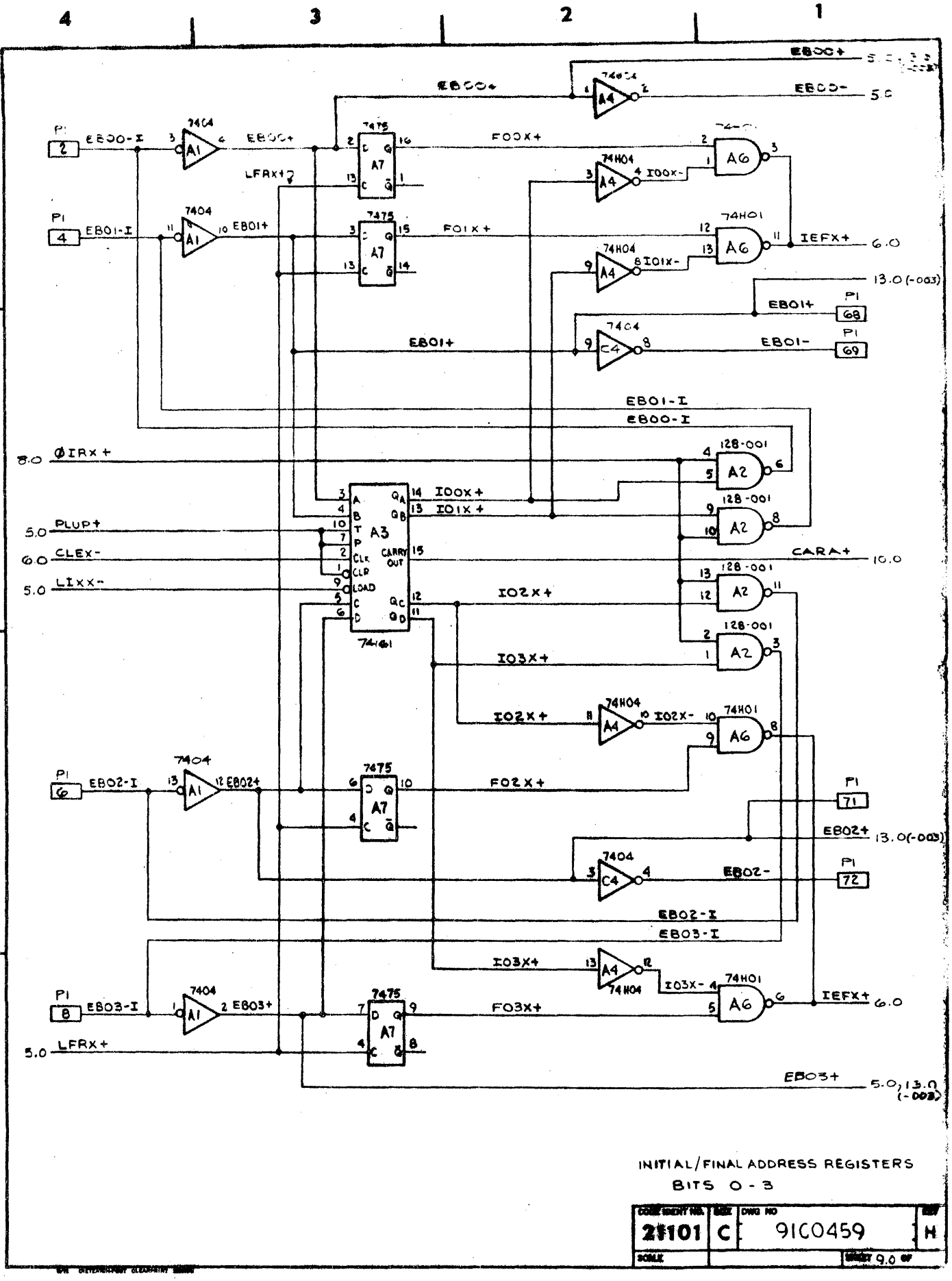
8-71 DIETERICH-POST CLEARPRINT 1000H-8

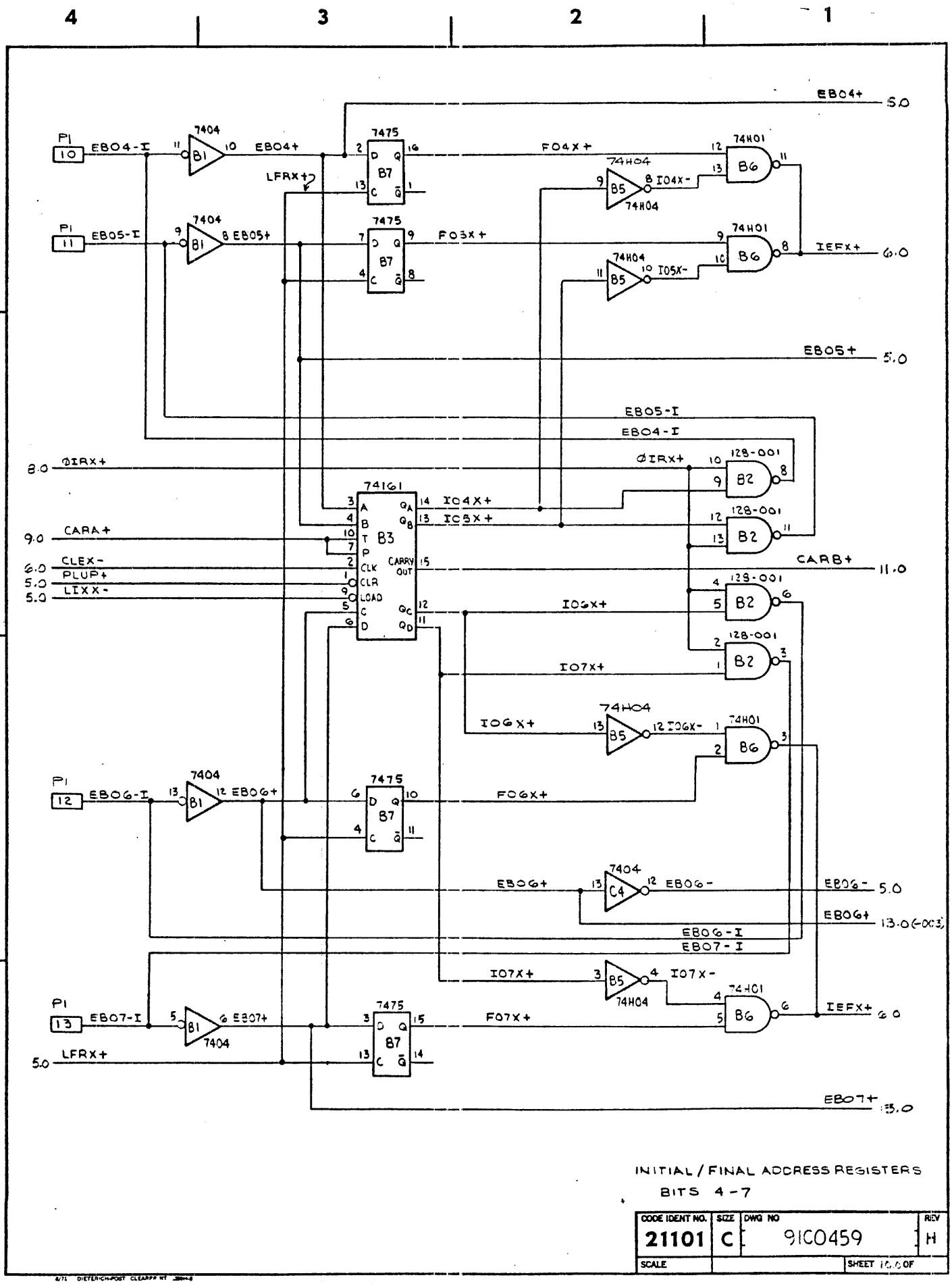


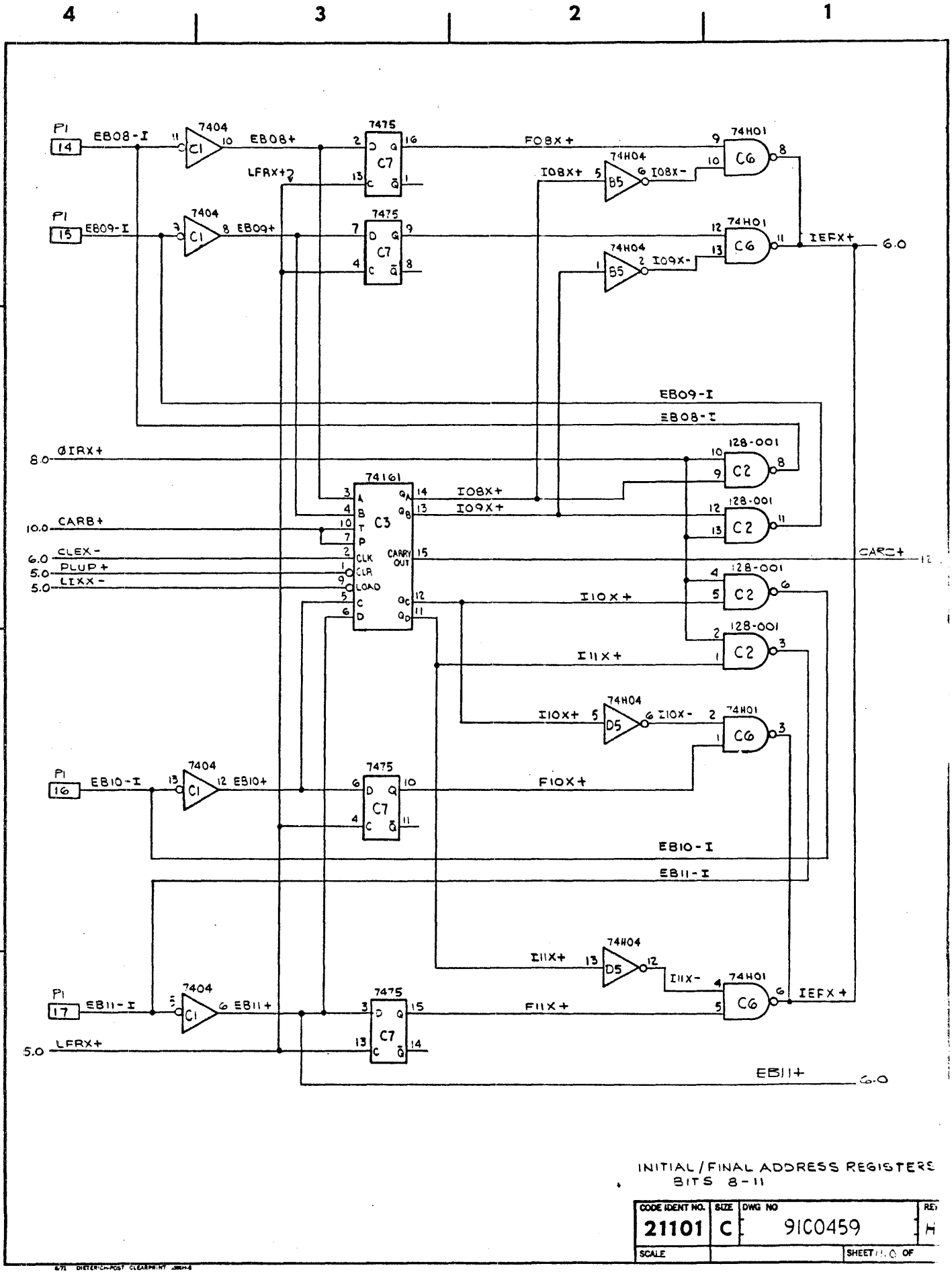
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100459	
SCALE		SHEET 7.0 OF	



CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0459	H
SCALE			SHEET OF


4
3
2
1
D
C
B
A
EB00+
EB00-
5.0
EB00-I
EB00+
FOOX+
LFRX+
IOOX-
IEFX+
6.0
13.0 (-003)
EB01-I
EB01+
FO1X+
IO1X-
EB01+
EB01-
EB01-I
EB00-I
8.0 ØIRX+
IOOX+
IO1X+
5.0 PLUP+
6.0 CLEX-
5.0 LIXX-
CARA+
10.0
IO2X+
IO3X+
IO2X-
FO2X+
EB02-I
EB02+
EB02-
EB03-I
IO3X+
IO3X-
FO3X+
EB03-I
EB03+
5.0, 13.0 (-003)
7404
7475
74H04
74H01
128-001
A1
A2
A3
A4
A6
A7
C4
P1
2
4
6
8
68
69
71
72
INITIAL/FINAL ADDRESS REGISTERS
BITS 0-3
21101
C
9100459
H
9.0

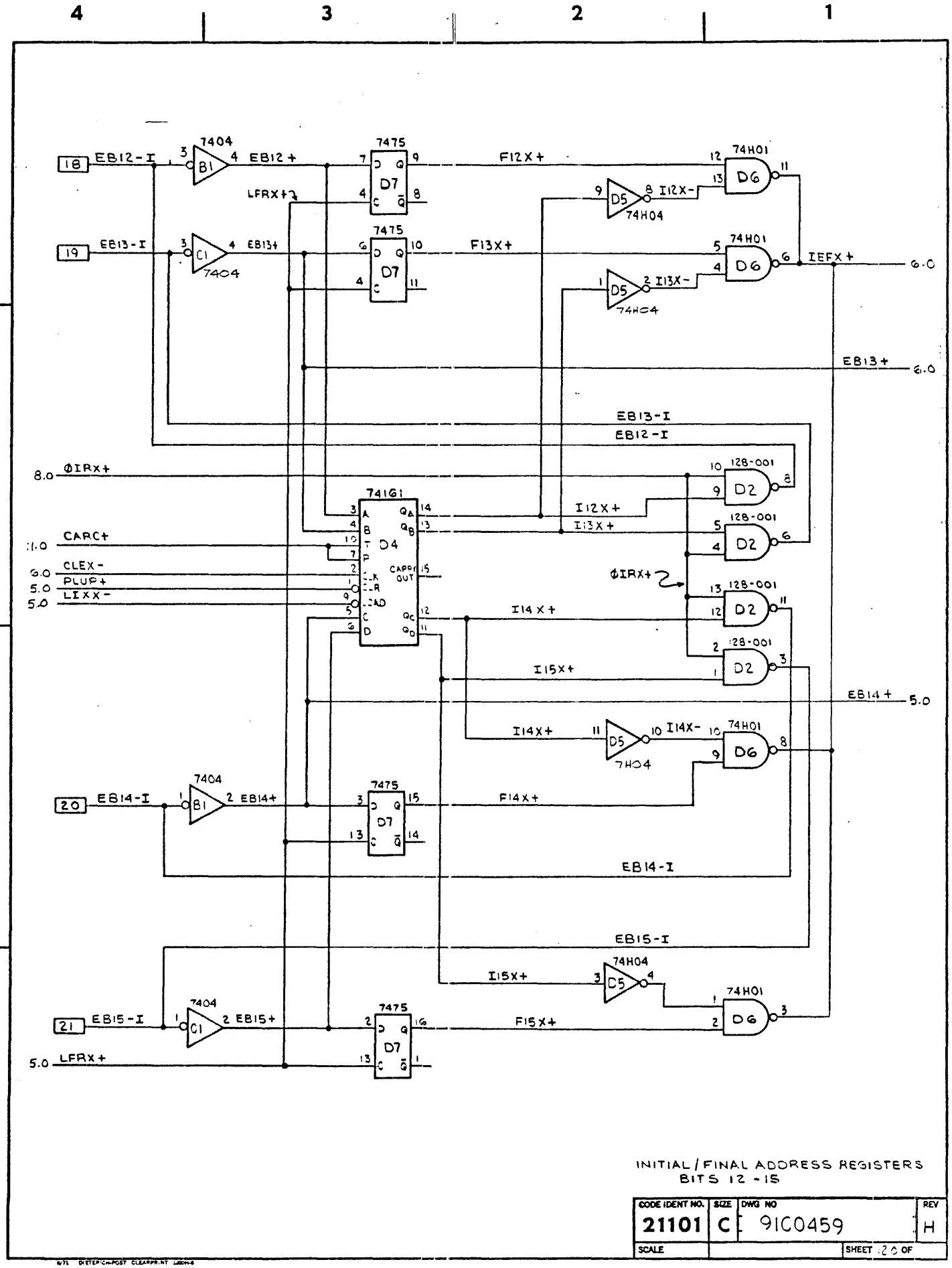

4
3
2
1
D
C
B
A
P1
10
EB04-I
7404
B1
EB04+
LFRX+
7475
B7
F04X+
74H04
B5
IO4X-
74H01
B6
IEFX+
EB04+ 5.0
P1
11
EB05-I
EB05+
F03X+
IO5X-
EB05+ 5.0
EB05-I
EB04-I
8.0 ØIRX+
ØIRX+
128-001
B2
74161
B3
IO4X+
IO5X+
9.0 CARA+
6.0 CLEX-
5.0 PLUP+
5.0 LIXX-
CARB+ 11.0
IO6X+
IO7X+
74H04
B5
IO6X-
74H01
B6
P1
12
EB06-I
EB06+
F06X+
EB06+
EB06- 5.0
EB06+ 13.0 (-0X3)
EB06-I
EB07-I
IO7X+
IO7X-
P1
13
EB07-I
EB07+
F07X+
IEFX+ 6.0
5.0 LFRX+
EB07+ 5.0
INITIAL / FINAL ADDRESS REGISTERS
BITS 4-7
CODE IDENT NO. 21101
SIZE C
DWG NO 9100459
REV H
SCALE
SHEET 10.0 OF



INITIAL / FINAL ADDRESS REGISTERS
BITS 8-11

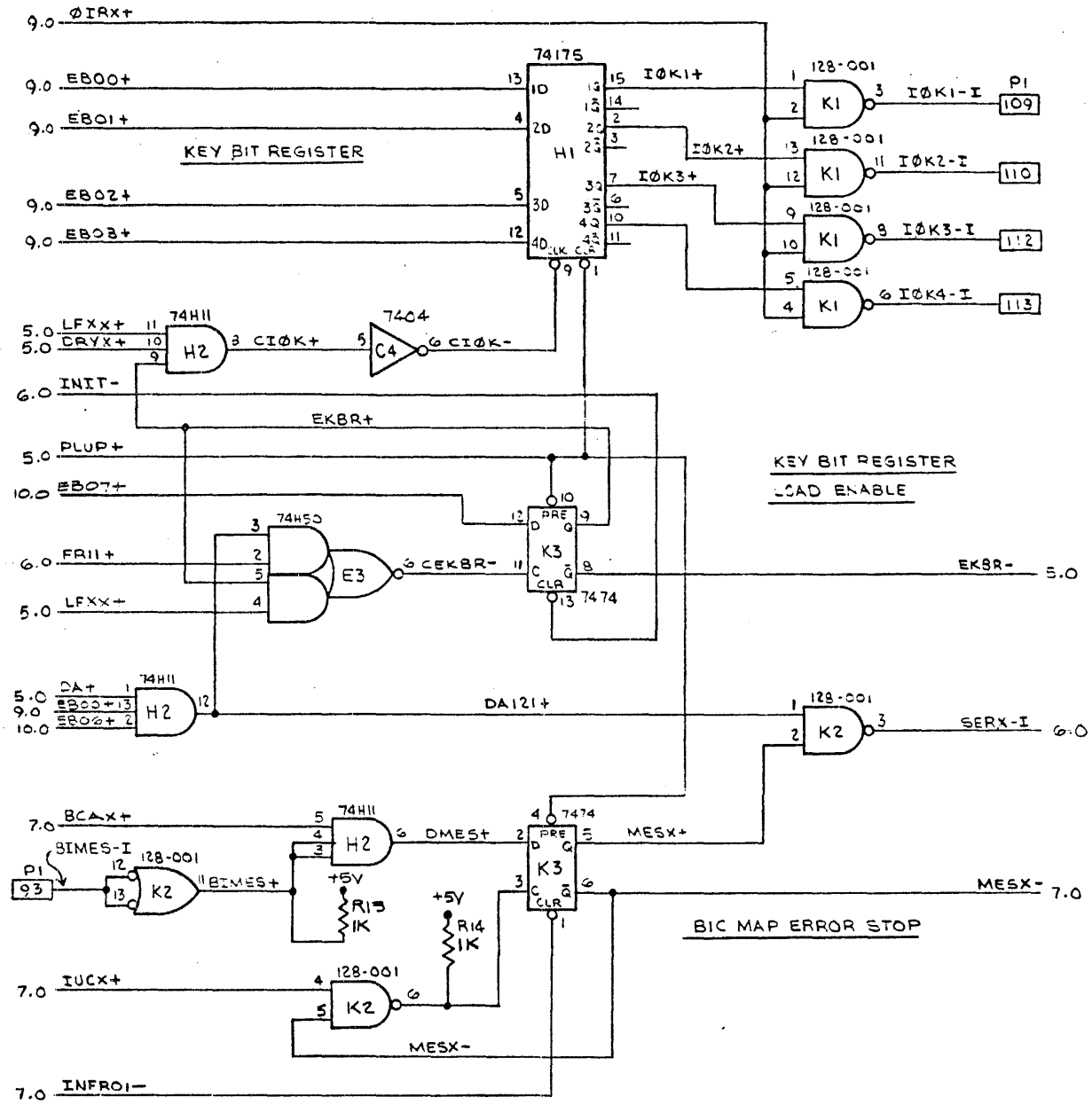
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100459	H
SCALE			SHEET 11.0 OF

6/71 DIETERICH-POST CLEARPRINT



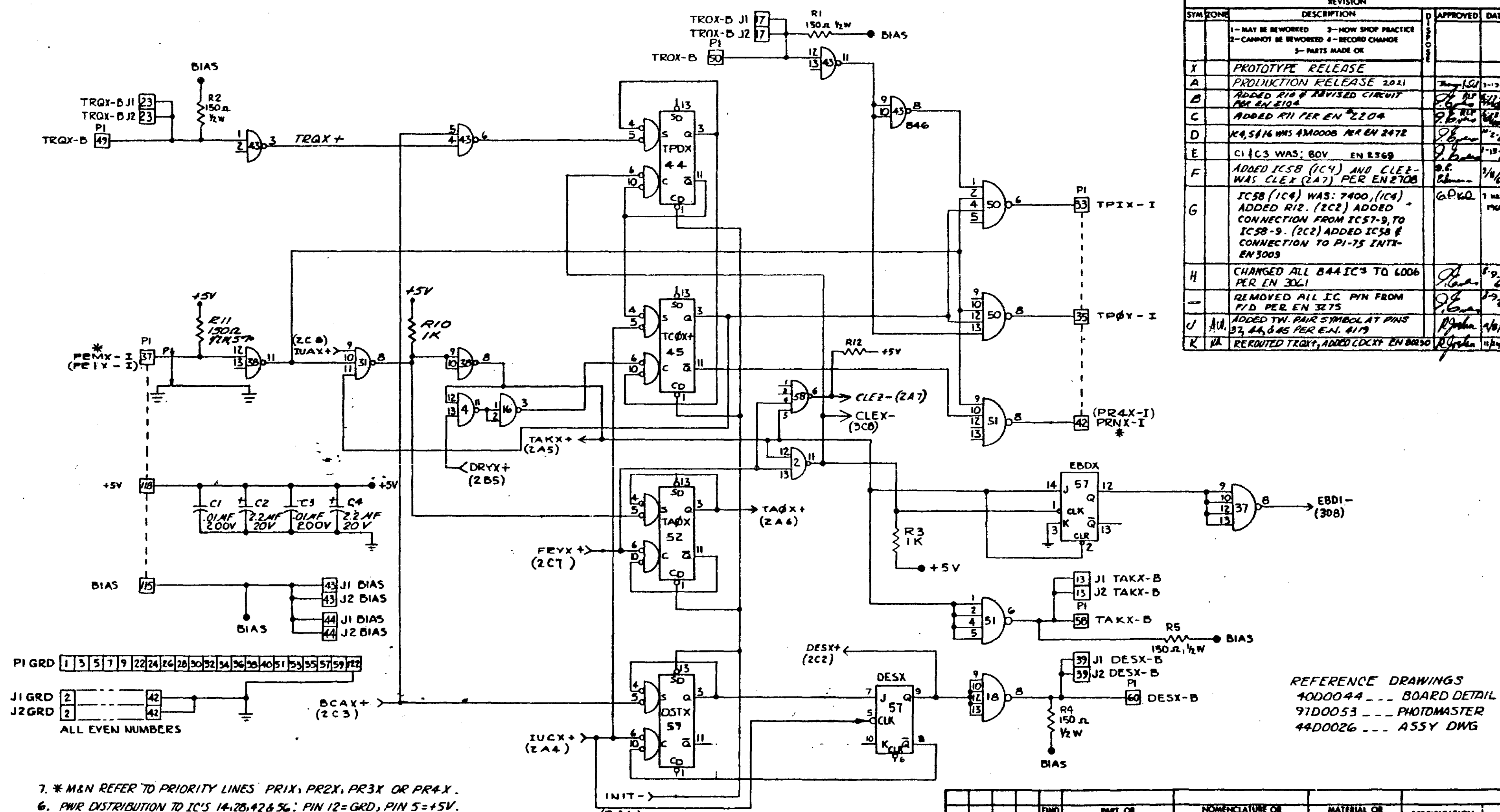
INITIAL / FINAL ADDRESS REGISTERS
BITS 12 - 15

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100459	H
SCALE			SHEET 20 OF



-003 ONLY

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100459	H
SCALE		SHEET 3 OF	



REVISION					
SYM	ZONE	DESCRIPTION (1—MAY BE REWORKED 3—HOW SHOP PRACTICE 2—CANNOT BE REWORKED 4—RECORD CHANGE 5—PARTS MADE OK)	D	APPROVED	DATE
X		PROTOTYPE RELEASE			
A		PRODUCTION RELEASE 2021			3-13-?
B		ADDED R10 & REVISED CIRCUIT PER EN 2104			
C		ADDED R11 PER EN #2204			
D		R4,5 & 16 WAS 4300008 PER EN 2472			
E		C1 & C3 WAS; 80V EN 2569			
F		ADDED IC58 (IC4) AND CLE2- WAS CLEX (2A7) PER EN 2708			3/4/69
G		IC58 (IC4) WAS: 7400, (IC4) ADDED R12. (2C2) ADDED CONNECTION FROM IC57-9, TO IC58-9. (2C2) ADDED IC58 & CONNECTION TO P1-75 INTR- EN 3009		GPKQ	1 MAY 1969
H		CHANGED ALL 844 IC'S TO 6006 PER EN 3061			8-9-69
—		REMOVED ALL IC PIN FROM F/D PER EN 3275			
J	All	ADDED TW. PAIR SYMBOL AT PINS 37, 44, & 45 PER E.N. 4119			4/8/70
K	All	REROUTED TRQX+, ADDED CDCX+ EN 80230			

7. * M&N REFER TO PRIORITY LINES PR1X, PR2X, PR3X OR PR4X.
6. PWR DISTRIBUTION TO IC'S 14, 28, 42 & 56: PIN 12 = GRD, PIN 5 = +5V.
5. PWR DISTRIBUTION TO IC57: PIN 11 = GRD, PIN 4 = +5V.
4. PWR DISTRIBUTION TO IC'S: PIN 7 = GRD, PIN 14 = +5V (EXCEPTIONS-NOTES 5 & 6).
3. ALL CAPACITOR VALUES ARE ± 10%.
2. RESISTORS ARE 1K, 1/4W, ± 5%.
1. THE SYMBOLS XXX> AND —> XXX INDICATE A SIGNAL SOURCE AND FLOW LOCATION CODE. THE FIRST DIGIT INDICATES SHEET NO., THE LETTER A HORIZONTAL ZONE AND THE SECOND DIGIT A VERTICAL ZONE. THE SYMBOL <—XXXX—> INDICATES A BI-DIRECTIONAL SIGNAL FLOW.

NOTE: UNLESS OTHERWISE SPECIFIED

HIGHEST REFERENCE DESIGNATIONS		
C4	R11	IC63
REFERENCE DESIGNATIONS NOT USED		

FIND NO.	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL OR CODE IDENT	SPECIFICATION
QTY REQD PER ASSY		LIST OF MATERIALS OR PARTS LIST		

DASH NO.	NEXT ASSY	N/A QTY
	44D0026	—

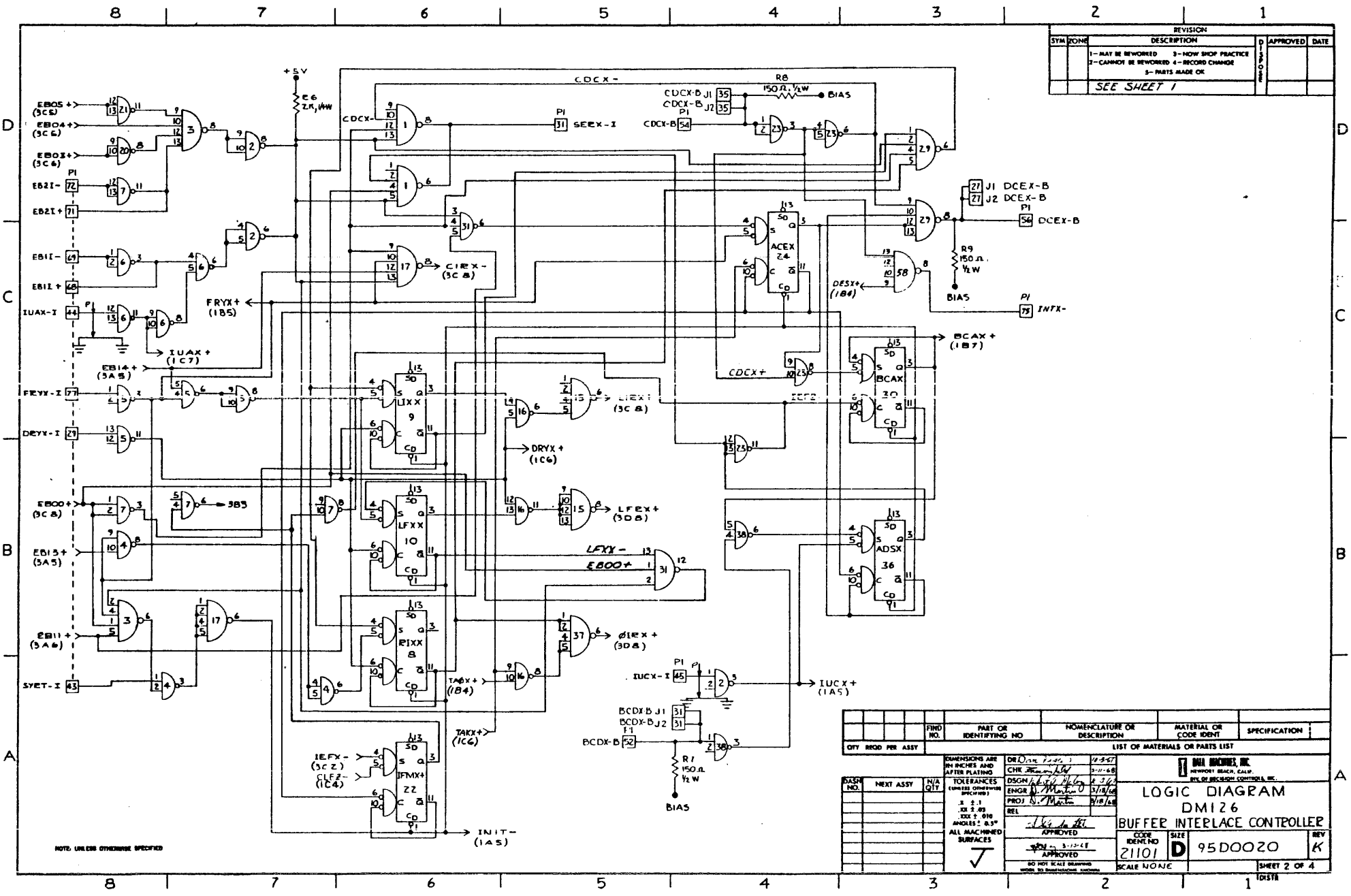
DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING
TOLERANCES (UNLESS OTHERWISE SPECIFIED) .X ± .1 .XX ± .03 .XXX ± .010 ANGLES ± 0.5° ALL MACHINED SURFACES √

DR | CHK | DSGN | ENGR | PROJ | REL
APPROVED
APPROVED
DO NOT SCALE DRAWING

DATA MACHINES, INC. NEWPORT BEACH, CALIF. DIV. OF DECISION CONTROLS, INC.

LOGIC DIAGRAM
DM126
BUFFER INTERFACE CONTROLLER

CODE IDENT NO 21101 | SIZE D | 95D0020 | REV K
SCALE NONE | 620-20 | SHEET 1 OF 4



REVISION					
SYM	ZONE	DESCRIPTION	DISPOSITION	APPROVED	DATE
		1 - MAY BE REWORKED 3 - NOW SHOP PRACTICE 2 - CANNOT BE REWORKED 4 - RECORD CHANGE 5 - PARTS MADE OK			
		SEE SHEET 1			

NOTE: UNLESS OTHERWISE SPECIFIED

FIND NO.	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL OR CODE IDENT	SPECIFICATION
QTY REQD PER ASSY		LIST OF MATERIALS OR PARTS LIST		

DASH NO.	NEXT ASSY	N/A QTY

DIMENSIONS ARE IN INCHES AND AFTER PLATING
TOLERANCES (UNLESS OTHERWISE SPECIFIED)
.X ± .1
.XX ± .03
.XXX ± .010
ANGLES ± 0.5°
ALL MACHINED SURFACES

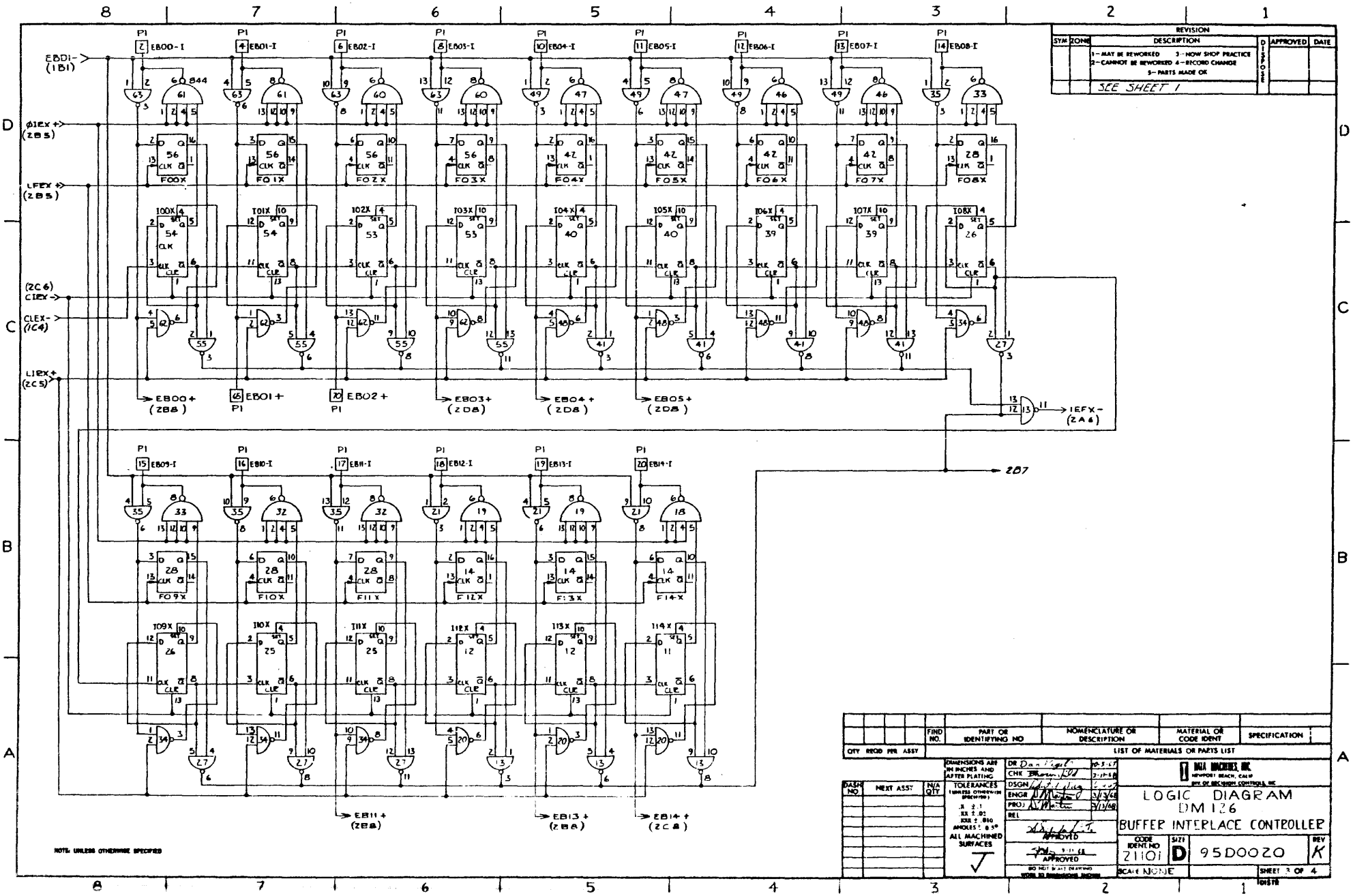
DR		12-5-67
CHK		3-11-68
DSGN		4-3-68
ENGR	D. Martin	3/18/68
PROJ	D. Martin	3/18/68
REL		
APPROVED		
APPROVED		3-13-68

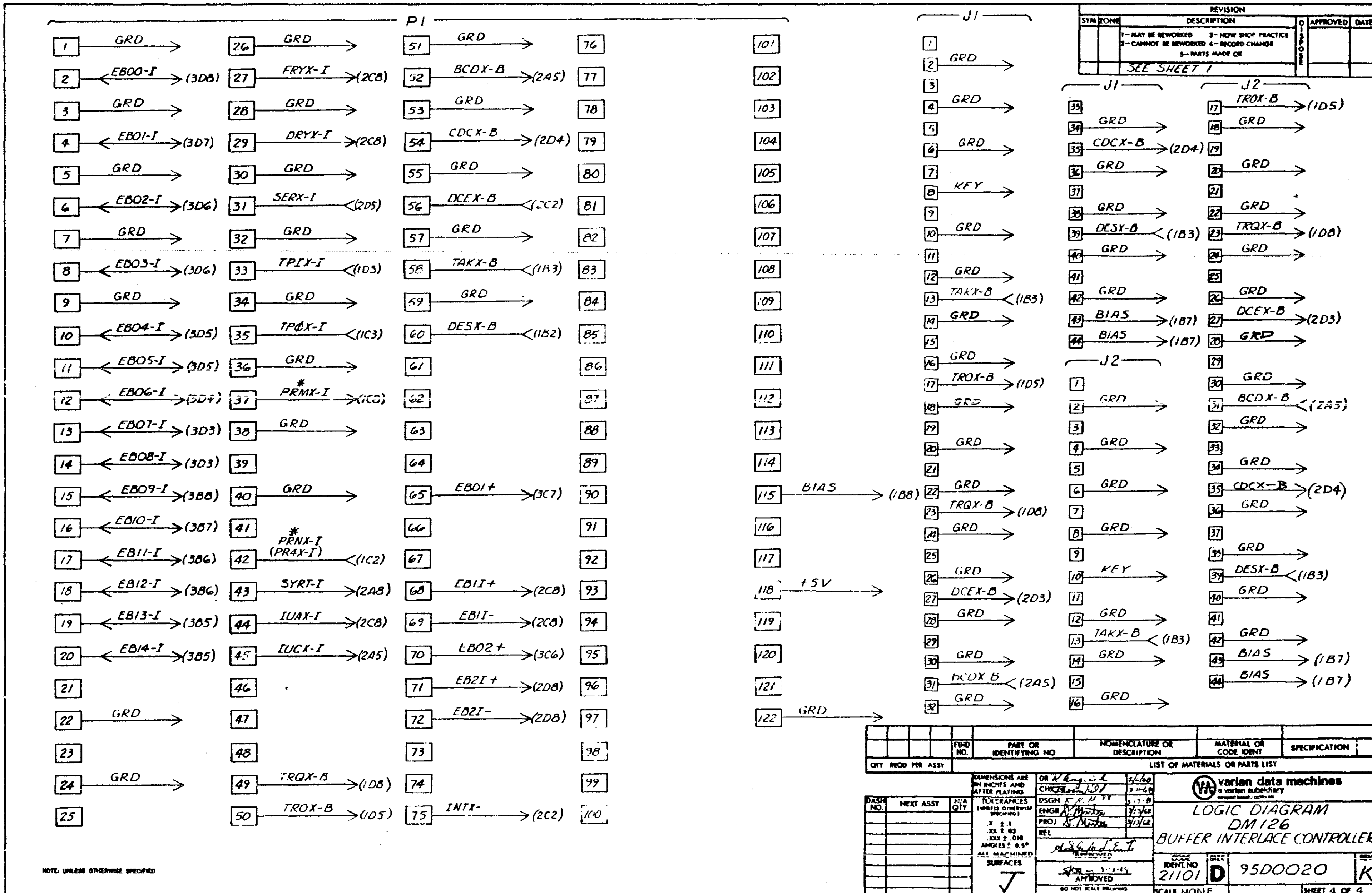
DO NOT SCALE DRAWING
WORK TO DIMENSIONS SHOWN

DIGI-DATA CORPORATION
SILVER SPRING, MARYLAND

LOGIC DIAGRAM
DM126
BUFFER INTERLACE CONTROLLER

CODE IDENT NO	SIZE		REV
21101	D	95D0020	K
SCALE NONE		SHEET 2 OF 4	


REVISION
SYM ZONE DESCRIPTION DISPOSE APPROVED DATE
1-MAY BE REWORKED 3-NOW SHOP PRACTICE
2-CANNOT BE REWORKED 4-RECORD CHANGE
5-PARTS MADE OK
SEE SHEET 1
EB00-I
EB01-I
EB02-I
EB03-I
EB04-I
EB05-I
EB06-I
EB07-I
EB08-I
EB09-I
EB10-I
EB11-I
EB12-I
EB13-I
EB14-I
EB01-
(1B1)
Ø1EX+
(2B5)
LFEX+
(2B5)
(2C6)
C1EX-
CLEX-
(1C4)
L1EX+
(2C5)
EB00+
(2B8)
EB01+
EB02+
EB03+
(2D8)
EB04+
(2D8)
EB05+
(2D8)
1EFX-
(2A6)
2B7
EB11+
(2B8)
EB13+
(2B8)
EB14+
(2C8)
NOTE: UNLESS OTHERWISE SPECIFIED
QTY REQD PER ASSY
FIND NO.
PART OR IDENTIFYING NO.
NOMENCLATURE OR DESCRIPTION
MATERIAL OR CODE IDENT
SPECIFICATION
LIST OF MATERIALS OR PARTS LIST
DASH NO.
NEXT ASSY
N/A QTY
DIMENSIONS ARE IN INCHES AND AFTER PLATING
TOLERANCES
ALL MACHINED SURFACES
DR
CHK
DSGN
ENGR
PROJ
REL
APPROVED
DO NOT SCALE DRAWING
DATA MACHINES, INC.
NEWPORT BEACH, CALIF.
DIV. OF MEASUREMENT CONTROLS, INC.
LOGIC DIAGRAM
DM126
BUFFER INTERLACE CONTROLLER
CODE IDENT NO 21101
SIZE D
95D0020
REV K
SCALE NONE
SHEET 3 OF 4


P1
1 GRD
2 EB00-I (3D8)
3 GRD
4 EB01-I (3D7)
5 GRD
6 EB02-I (3D6)
7 GRD
8 EB03-I (3D6)
9 GRD
10 EB04-I (3D5)
11 EB05-I (3D5)
12 EB06-I (3D4)
13 EB07-I (3D3)
14 EB08-I (3D3)
15 EB09-I (3B8)
16 EB10-I (3B7)
17 EB11-I (3B6)
18 EB12-I (3B6)
19 EB13-I (3B5)
20 EB14-I (3B5)
21
22 GRD
23
24 GRD
25
26 GRD
27 FRYX-I (2C8)
28 GRD
29 DRYX-I (2C8)
30 GRD
31 SERX-I (2D5)
32 GRD
33 TPIX-I (1D5)
34 GRD
35 TPØX-I (1C3)
36 GRD
37 PRMX-I *
38 GRD
39
40 GRD
41
42 PRNX-I * (PR4X-I) (1C2)
43 SYRT-I (2A8)
44 IUAX-I (2C8)
45 IUCX-I (2A5)
46
47
48
49 TRQX-B (1D8)
50 TROX-B (1D5)
51 GRD
52 BCDX-B (2A5)
53 GRD
54 CDCX-B (2D4)
55 GRD
56 DCEX-B (2C2)
57 GRD
58 TAKX-B (1B3)
59 GRD
60 DESX-B (1B2)
61
62
63
64
65 EB01+ (3C7)
66
67
68 EB1I+ (2C8)
69 EB1I- (2C8)
70 EB02+ (3C6)
71 EB2I+ (2D8)
72 EB2I- (2D8)
73
74
75 INTX- (2C2)
76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100
101 102 103 104 105 106 107 108 109 110 111 112 113 114
115 BIAS (1B8)
116 117
118 +5V
119 120 121
122 GRD
J1
1
2 GRD
3
4 GRD
5
6 GRD
7
8 KEY
9
10 GRD
11
12 GRD
13 TAKX-B (1B3)
14 GRD
15
16 GRD
17 TROX-B (1D5)
18 GRD
19
20 GRD
21
22 GRD
23 TRQX-B (1D8)
24 GRD
25
26 GRD
27 DCEX-B (2D3)
28 GRD
29
30 GRD
31 BCDX-B (2A5)
32 GRD
J1
33
34 GRD
35 CDCX-B (2D4)
36 GRD
37
38 GRD
39 DESX-B (1B3)
40 GRD
41
42 GRD
43 BIAS (1B7)
44 BIAS (1B7)
J2
1
2 GRD
3
4 GRD
5
6 GRD
7
8 GRD
9
10 KEY
11
12 GRD
13 TAKX-B (1B3)
14 GRD
15
16 GRD
J2
17 TROX-B (1D5)
18 GRD
19
20 GRD
21
22 GRD
23 TRQX-B (1D8)
24 GRD
25
26 GRD
27 DCEX-B (2D3)
28 GRD
29
30 GRD
31 BCDX-B (2A5)
32 GRD
33
34 GRD
35 CDCX-B (2D4)
36 GRD
37
38 GRD
39 DESX-B (1B3)
40 GRD
41
42 GRD
43 BIAS (1B7)
44 BIAS (1B7)
REVISION
SYM ZONE DESCRIPTION APPROVED DATE
1— MAY BE REWORKED 3— NOW SHOP PRACTICE
2— CANNOT BE REWORKED 4— RECORD CHANGE
5— PARTS MADE OK
SEE SHEET 1
D C B A
8 7 6 5 4 3 2 1
NOTE: UNLESS OTHERWISE SPECIFIED
FIND NO. | PART OR IDENTIFYING NO | NOMENCLATURE OR DESCRIPTION | MATERIAL OR CODE IDENT | SPECIFICATION
QTY REQD PER ASSY | LIST OF MATERIALS OR PARTS LIST
DASH NO. | NEXT ASSY | N/A QTY
DIMENSIONS ARE IN INCHES AND AFTER PLATING
TOLERANCES (UNLESS OTHERWISE SPECIFIED)
.X ±.1 .XX ±.03 .XXX ±.010 ANGLES ± 0.5°
ALL MACHINED SURFACES
DR CHKD DSGN ENGR PROJ REL
APPROVED
DO NOT SCALE DRAWING
varian data machines
a varian subsidiary
LOGIC DIAGRAM
DM126
BUFFER INTERLACE CONTROLLER
CODE IDENT NO 21101
SIZE D
95D0020
REV K
SCALE NONE
SHEET 4 OF 4

NOTE:

BIC SPS no longer used

See PTS SPS for BIC Test

DWG NO 98A0767

REVISIONS

COD	SYM	DESCRIPTION	APPROVED	DATE
-	A	PRODUCTION RELEASE PER EN 80371	[illegible]	1/11/72
-	B	REVISED PER EN 80548	RLO	3/22/72
3	C	LINED OUT 44D0587 AND 91C0352. ADDED 44D0677 & 91C0445 ON SHEET 4. REVISED NOTE SHEET 18. 91C0445 WAS 91C0352 PARA 6.0, 6.1.4, 6.3.1 PER EN 84187	SOH / MP.	10/17/75

DR	P. LUBY	11/15/71
CHK	WHD	12/2/71
DSGN	——	
ENGR	[signature]	11/22/71
APPD	[signature]	11/22/71
APPD	[signature]	12/6/72

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varian data machines /a varian subsidiary
2722 michelson drive / irvine / california / 92664

TITLE

ENGINEERING DESCRIPTION
~~620-82~~
UNIVERSAL ASYNCHRONOUS SERIAL CONTROLLER (UASC)

CODE IDENT NO.	SIZE	DWG NO.	REV
21101	A	98A0767	C

SCALE —— SHEET 1 OF 51

96A0153-16

INDEX

INDEX

SECTION VI - THEORY OF OPERATION

INDEX

PAGE

ILLUSTRATIONS

ENGINEERING DATA FORM

OPTION	Universal Asynchronous Serial Controller
MODEL	620-82 (Formerly E2184)
NO. OF LOGIC CARDS REQ'D.	1
NO. OF CARD SLOTS REQ'D.	1
LOCATION OF SLOTS (NUMBERING)	Any I/O slot
CONNECTORS REQ'D. (EXCLUDING I/O)	2- 44 pin burndy (supplied)
KEYING	NA
ST'D. DEVICE ADDRESS	02 thru 07 (01 if for TTY) (Can be 00 thru 77)
WIRELIST NUMBER	PC board
MANUAL PUBLICATIONS NUMBER	98A0767
PERIPHERAL EQUIPT. REQ'D	NA
MFG'R.	NA
MODEL	NA
GEN'L. SPECS	NA

NOTES:

RS232 version requires 100ma of +12V and -12V dc

Reference Documents:

Top Assembly	01A1259
Controller	~~44D0507~~ 44D0677
Test Specification	98A0768
Test Prog. SPS	89A0228
Logic Diagrams	~~91C0352~~ 91C0445
Test Routine	32A0107-010

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irvine/california/92664

CODE IDENT. NO		98A0767	REV C
PREPARED BY	APPR.	SHT 4 OF 53	

SECTION 1
DESCRIPTION

1.1 Introduction

The UASC (Universal Asynchronous Serial Controller) is a versatile character buffered serial controller which can operate in both half or full duplex modes. Four interfaces are available to the user: RS232, Current loop, relay and DTL/TTL. The DTL/TTL interface is always on the controller where as the RS232 or Current Mode or Relay interfaces are selected at time of purchase. The controller is not a data set controller but intended for use on direct connect interfaces.

The controller is capable of operating with one start bit and one or two stop bits, 5,6,7, or 8 bits of data, parity or no parity bit, and odd or even parity. Several operating frequencies from 9600 baud down to 45 baud are possible. All options and operating modes will be set up for the user by VDM, if all requirements are supplied at time of purchase. If the user does not specify the set up for the UASC, the RS232 version will be set up for 1200 baud with no parity, 8 bits of data and one stop bit. Also, the Current Mode version will be set up for 1200 baud with no parity, 8 bits of data and one stop bit. In addition, the relay version will be set up for 110 baud with no parity, 8 bits of data and two stop bits. Transmit and receive rates will always be equal. The user can easily modify the controller to his data transmission format by placing jumpers on the board as described in section 1.2.2.

1.2 Functional Description

Reference Block Diagram (Figure 1.1).

1.2.1 Timing

Transmit and Receive clocking to the LSI transmitter/receiver circuit is derived from a 4.608 meg Hz crystal oscillator. A clock rate is derived by setting up the appropriate count in the 12 bit counter. The clock is set up to provide a clock rate 16 times the transmit/receive rate. See Figure 1.2.

FIGURE 1.2 - BAUD RATE SELECTION CHART

Baud Rate	Div. By	E1.	E2.	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12
9600	15		X	X	X								
4800	30	X		X	X	X							
2400	60	X	X		X	X	X						
2000	72	X	X	X				X					
1800	80	X	X	X	X			X					
1200	120	X	X	X		X	X	X					
600	240	X	X	X	X		X	X	X				
300	480	X	X	X	X	X		X	X	X			
150	960	X	X	X	X	X	X		X	X	X		
110	1309			X	X	X				X		X	
75	1920	X	X	X	X	X	X	X		X	X	X	
45	3200	X	X	X	X	X	X	X				X	X

Note that jumper values are selected at one less than the desired divisor value. Other baud rates can be derived by the following formulas

$$D = \left(\frac{CR}{2} \div 16\right) \div BR - 1$$

or

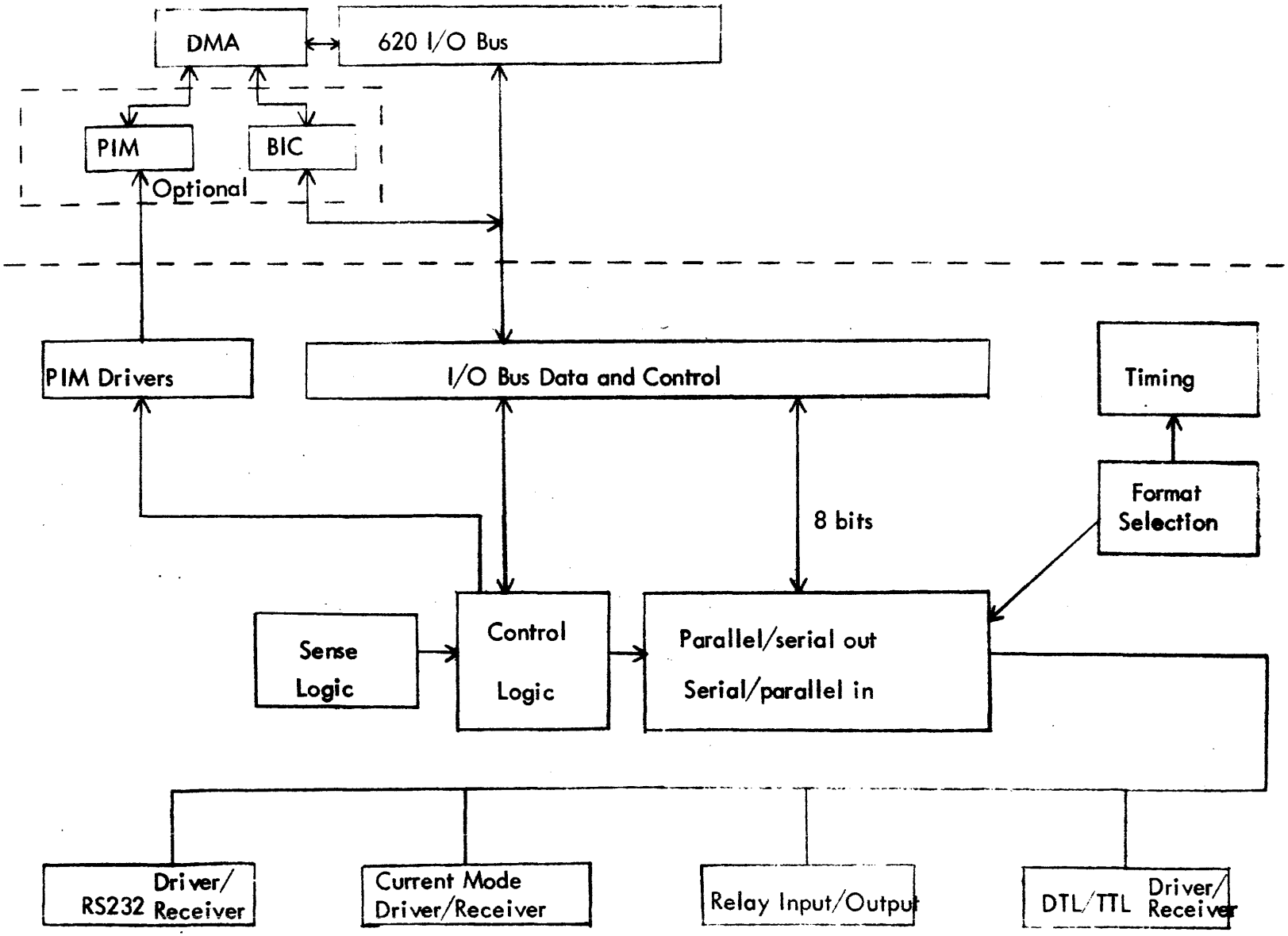
$$(144,00) \div BR - 1$$

D = Divisor
CR = Clock or Oscillator Rate
BR = Baud Rate desired

Note: Remainder should not exceed 1% of BR.

Jumpers E1 through E12 are placed on the controller (above the large chip) per the above chart.

FIGURE 1.1 - FUNCTIONAL BLOCK DIAGRAM



Choice of four user interface circuits.

98A0767 SH 7 C 53 REV C
CODE IDENT NO. 21101
varian data machines a varian subsidiary
96A0039-000B

1.2.2 Format Selection

Format selection is accomplished prior to initial operation or hookup to the serial device to be controlled. Choice of combinations of five jumpers will provide the following variations: One or two stop bits, 5-6-7 or 8 data bits, odd parity, even parity or no parity. (See Figure 1.3 and 1.4.)

1.2.3 620/I/O Bus

The I/O interface is an 8 bit interface to the 620 16 bit I/O. The most significant 8 bits are not used in the 16 bit data word. DMA data transfer in or out of the 620 is possible in conjunction with the BIC option. It should be noted that although this controller has full duplex capability, the BIC can only be connected to the transmit functions or to the receive function (not both at the same time).

1.2.4 Transmit Section

Data is transferred from the 620 I/O to the 8 bit parallel buffer register in the LSI circuit. The 8 bits are then transferred into the serial shift register and shifted out serially with the least significant bit (bit 0) shifted out first. A zero or "space" bit is inserted at the beginning of each serial word. This "Start Bit" preceeds the 5,6,7, or 8 data bits and the parity bit (if selected) and the "Stop Bit"(s). The stop bit(s) is a "1" or "mark" bit.

1.2.5 Receive

Data is received into the serial shift register with Start Bit first followed by 5,6,7, or 8 data bits (least significant bit first), a parity bit (if selected), and 1 or 2 Stop Bits. When the complete character is shifted into the serial register, it is transferred into the parallel buffer register. Immediately after loading the parallel register, the Input Ready Sense line is made "true". Inputting the character will set Input Ready "false". Both Transmit and Receive functions are character buffered and operate independently. The format of the data being received must be the same as that selected for proper operation.

1.2.6 Control Logic

The Control Logic provides direction control for data transfer to and from the I/O bus, BIC connect control, Initialize control, and control of an external line (option enable/disable).

FIGURE 1.3

FORMAT SELECTION CHART

Jumpers Added	Result
E13	Parity Bit Enabled
E14	One Stop Bit
E15 and 16	Five Data Bits per character
E15	Six Data Bits per character
E16	Seven Data Bits per character
E17	Odd Parity Bit

Jumpers Omitted	Result
E13	Parity Bit Disabled
E14	Two Stop Bits
E15 and 16	Eight DataBits per character
E17	Even Parity Bit

Typical ASCII devices use one start bit, 7 data bits and one parity or 8 data bits, with one or two stop bits.

FIGURE 1.4

ASYNCHRONOUS FORMAT EXAMPLES

1.

MSB ⟶ LSB

Stop Bit	Parity Bit	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Start Bit

a) 8 Data Bits Selected
b) Parity Bit Selected
c) One Stop Bit Selected

This is a good format for CPU to CPU.

2.

MSB ⟶ LSB

Stop Bit	Stop Bit	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Start Bit

a) 8 Data Bits Selected
b) Parity Bit not Selected
c) Two Stop Bits Selected

Typical for VDM teletype ASR 33 and 35.

3.

MSB ⟶ LSB

Stop Bit	Parity Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Start Bit

a) 7 Data Bits Selected
b) Parity Bit Selected
c) One Stop Bit Selected

4.

MSB ⟶ LSB

1/2 Stop Bit	Stop Bit	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Start Bit

a) 5 Data Bits Selected
b) Parity Not Selected
c) Two Stop Bits Selected

Typical Baudot code.

1.2.7 Sense Logic

The Sense Logic provides status information to the operating program. Status of Input and Output data registers, three error indications, and an external input line can be monitored.

1.2.8 PIM Drivers

Three PIM Drivers are made available. One line indicates Input Ready. A second line indicates Output Ready. A third indicates either an Input Overflow Error or a Frame Error (Break). An Overflow Error indicates a second character was transferred to the parallel buffer register before the first character was Input. A Frame Error indicates that the first stop bit received was not a "1" bit. The program can detect that a "Break" character was received by verifying that the character received with the Frame Error indication was also an "All Zero" character. Typically, a "Line Break" is more than one consecutive character time. The UASC can receive but cannot transmit a "Line Break".

1.2.9 RS232 Driver/Receivers

The RS232 version fulfills the electrical characteristic requirements of EIA-RS232 B and C. Transmit data, receive data, a control line out and a status line in are implemented with RS232 drivers and receivers.

1.2.10 Current Mode Driver/Receiver

Transmit Data and Receive Data lines only are implemented with this interface. This current loop is capable of operation from 20MA to 60MA at voltages not to exceed 120V across the Transmit Driver. The current loop provides isolation greater than 10 meg ohms at 500Vdc. Detailed specifications are in section 2.2

1.2.11 Relay Input/Output

The relay input/output section is mechanized mainly for use as a Teletype Interface. A 2.2K -2 Watt resistor in the Transmit or output circuit and a 2.7K - 2 Watt resistor in the Receive or input circuit are provided as dropping resistors to facilitate connection to the teletype provided line battery source on models 33 and 35. The line battery is a Teletype Option.

The resistors can be bypassed to provide a 20Ma - 12Vdc input/output circuit. Etched pads are made available for this purpose.

The relays are a "Reed" type relay which will function correctly from 0 to 300 baud (150 operations per second max).

1.2.12 DTL/TTL Driver/Receiver

The Transmit/Receive Data Lines, as well as the option driver line and option status line, are made available to the user for direct connect to DTL/TTL interfaces. These lines should not exceed 20 feet in cable length. The three previously described interfaces are routed through the DTL/TTL Receivers via the input connectors (J1 and J2).

1.3 Logic Mnemonics List

BRYX	BIC Data Ready
BTIA	Byte Transfer In
BTOA	Byte Transfer Out
CLK 16	Clock, 16 times data rate
CDCX	BIC Controlled Device Connect
CODX	Function Decode - CODO thru COD7
DAXX	Device Address
DRYX	Data Ready, I/O
DTIX	Data Transfer In
DTOX	Data Transfer Out
E/B Int	Framing Error or Overrun Error
EBXX	620 I/O Data Lines - EB00 thru EB15
EPE	Even Parity Select
FE	Framing Error on line break
FNCODX	Function Code EXC 0 thru EXC7
FRYX	Function Ready I/O
FUNCA	Function order any EXC command
INIT	Initialize
OE	Overrun Error
OPIN	Option Status Line
OPON	Optional Control Line Command Storage
ØSC	4.608 Mhz Oscillator Output
ØSC 1	2.304 Mhz Clock Rate
PE	Parity Error
PI	Parity Enable Line
RCRDY	Receive Data Buffer Ready
RCRINT	Receive Data Ready Interrupt
RD	Receive Data DTL/TTL Input
RD1	Receive Data Current Loop Input

Logic Mnemonics List

RD2	Receive Data RS232 Input
RD3	Receive Data Relay Input
RSFF+	Clock Counter Reset Flip Flop
RRX	Received Data - 8 bits parallel 9 thru 7
SBS	Stop Bit Select
SD	Send Data (Transmit)
SERX	Sense Response
TXRDY	Transmit Data Buffer Ready
TXRINT	Transmit Ready Interrupt
WLS1	Data Bits per Word Select
WLS2	Data Bits per Word Select

SECTION II
INTERFACE AND CONNECTIONS

2.1 RS232 Option

Conforms to EIA RS232 B and C as applicable.

2.1.2 Logic 0 = +4 to +24V

Logic 1 = 0V to -24V

2.2 Current Mode Option

2.2.1 Driver Specification (Note 1)

Collector Emitter Voltage	V_{CEO}	150Vdc Max
Collector Current - Continuous	I_C	500 MAdc Max
Total Dissipation @25°C	P_d	1 Watt Max

2.2.2 Receiver Specification (Note 1)

Input Forward Voltage Drop	V_F	1.5Vdc Max
Input Forward Continuous Current	I_F	60MA Max

2.2.3 Isolation

Common Mode Protection	500V dc
Common Mode Resistance	10 Meg Ohms

2.2.4 Logic 0 = No loop current

Logic 1 = Loop current (20 ma min)

NOTE 1: Current limiting resistors (2.0K - 2W) are mounted in the input and output circuits. Values of these resistors may require change or shorted out. Current ratings above must not be exceeded.

2.3 Relay Option

2.3.1 Input (Note 2)

Relay Input Coil Rating 12.5Vdc max.

Relay Input Coil Resistance 1250 ohms

2.3.2 Output (Note 2)

Reed Relay Contact Closure - Form A

2.3.3 Isolation

Common mode resistance 10Meg Ohm @400Vdc

2.3.4 Logic 0 = No current
Logic 1 = Current (10 ma min)

Note 2: Current limiting resistors of 2.7K in the input side and 2.0K in the output side may be changed or shorted out. Caution must be used not to exceed 100 Ma through input relay coil.

2.4 DTL/TTL (not available when used with RS232)

2.4.1 Input

Both inputs present a 10Ma load at +5Vdc to the user.

2.4.2 Output

Both drivers are capable of sinking 50Ma at +5Vdc.

2.4.3 Logic 0 = $\geq$ +2.4Vdc

Logic 1 = 0 $\pm$ .5Vdc

FIGURE 2.1

PIN ASSIGNMENT CHART

RS 232

FUNCTION	PIN LOCATION
Serial Data Transmit	J2-36
Return	J2-35
Serial Data Receive	J2-42
Return	J2-41
Data In (Jumper)	J2-44 to J2-28
Optional Use Control Line	J2-34
Return	J2-33
Optional Use Status Line	J2-40
Return	J2-39

* CURRENT MODE VERSION

FUNCTION	PIN LOCATION
Serial Data Transmit +	J2-4
Serial Data Transmit -	J2-10
Serial Data Receive +	J2-24
Serial Data Receive -	J2-18
Data In (Jumper)	J2-26 to J2-28

* CAUTION: Excessive reverse current may damage the current mode interface.

FIGURE 2.1 (Cont'd)

RELAY VERSION	
FUNCTION	PIN LOCATION
Serial Data Transmit +	J1-26
Serial Data Transmit -	J1-20
Serial Data Receive +	J1-36
Serial Data Receive -	J1-38
Data In (Jumper)	J1-40 to J1-2

* DTL/TTL CONNECTION	
FUNCTION	PIN LOCATION
Serial Data Transmit	J2-2
Return	J2-1
Serial Data Receive	J2-28
Return	J2-27
Optional Use Control Line	J2-22
Return	J2-21
Optional Use Status Line	J2-38
Return	

* Note: The above Driver/Receiver cannot be used when the RS232 Driver/Receivers are in place.

FIGURE 2.2

DEVICE ADDRESS SELECTION							
TENS DIGIT				UNITS DIGIT			
D.A.	JUMPERS			D.A.	JUMPERS		
0X	76 to 83	77 to 85	78 to 87	X0	66 to 65	69 to 68	72 to 71
1X	76 to 82	77 to 85	78 to 87	X1	66 to 64	69 to 68	72 to 71
2X	76 to 83	77 to 84	78 to 87	X2	66 to 65	69 to 67	72 to 71
3X	76 to 82	77 to 84	78 to 87	X3	66 to 64	69 to 67	72 to 71
4X	76 to 83	77 to 85	78 to 86	X4	66 to 65	69 to 68	72 to 70
5X	76 to 82	77 to 85	78 to 86	X5	66 to 64	69 to 68	72 to 70
6X	76 to 83	77 to 84	78 to 86	X6	66 to 65	69 to 67	72 to 70
7X	76 to 82	77 to 84	78 to 86	X7	66 to 64	69 to 67	72 to 70

All pins on this page are on the I/O Back Panel.

INTERRUPT (PIM LINES)		
FUNCTION	PIN	Suggested Order of Priority
Transmit Data Reg. Ready	89	#2
Return	90	
Receive Data Reg. Ready	91	#1
Return	94	
Error or Break Interrupt	93	#3
Return	94	

2.5 Device Address and PIM Drivers

The DA for the UASC is wired on I/O back panel. The entire address, both octal digits, must be properly wired for the selected address. DA02 is the first standard address. Add 6 jumpers for the address selected per Figure 2.2.

The PIM drivers are implemented as pulse drivers and can be tied together as an "or" function or can be used on a one for one basis. The program must sense all three functions per interrupt if all are tied together to one PIM input. Reference Figure 2.2 for pin connections.

SECTION III
PROGRAMMING - UASC

3.1 Instruction Set

Execute Instructions

EXC 0	1000XX	Connect BIC (output)
EXC 1	1001XX	Connect BIC (output)
EXC 2	1002XX	Connect BIC (input)
EXC 3	1003XX	Not used
EXC 4	1004XX	Initialize Controller
EXC 5	1005XX	Connect BIC (input)
EXC 6	1006XX	Enable (option)
EXC 7	1007XX	Disable (option)

Sense Instructions

SEN 0	1010XX	Frame Error or Break
SEN 1	1011XX	Output Ready
SEN 2	1012XX	Input Ready
SEN 3	1013XX	Not used
SEN 4	1014XX	Input Parity Error
SEN 5	1015XX	Not used
SEN 6	1016XX	Sense (option)
SEN 7	1017XX	Input overflow error

Data Transfer Instructions

OAR	1031XX	XFER "A" reg to controller
OBR	1032XX	XFER "B" reg to controller
OME	1030XX	XFER Memory to controller
INA	1021XX	XFER Data to "A" reg
INB	1022XX	XFER Data to "B" reg
IME	1020XX	XFER Data to Memory
CIA	1025XX	XFER Data to cleared "A" reg
CIB	1026XX	XFER Data to cleared "B" reg.

Standard Device Address is as follows:

1st Unit	=	02
2nd Unit	=	03
3rd Unit	=	04
4th Unit	=	05
5th Unit	=	06
6th Unit	=	07

DA01 may be used if UASC is used on the first teletype in a system.

3.2 Explanation of Instruction Set

3.2.1 EXC Instructions

EXC 0 and EXC 1 are both (either one) used to connect the BIC to output control of the UASC.

EXC 2 and EXC 5 are both (either one) used to connect the BIC to control input of the UASC. The multiple BIC connect instructions are implemented for compatibility of the UASC, Teletype Controller, Paper Tape Controller, etc., instruction sets. The EXC 6 and EXC 7 instructions are used to turn on optional control line on and off. EXC 4 is used to reset all functions on the UASC.

3.2.2 Sense Instructions

SEN 0, Frame Error or Break, is used to detect that a character received did not have "mark" or "1" stop bits. The program can check the received character to verify that the data was all "zeros". If the data was all zeros and a Frame Error was sensed, a "Line Break" was received. If the data was not all zeros, the error was probably a "hit' on the line or noise.

SEN 1 and SEN 2 indicate the status of the Transmit and Receive buffer registers. SEN 4 indicates, when true, that a parity error has been detected on a character received.

SEN 6 indicates the status of an optional status line. SEN 7 indicates that another character was received before the prior character was removed from the input register.

3.2.2 Data Transfer Instructions

These instructions are self explanatory. See 3.1.

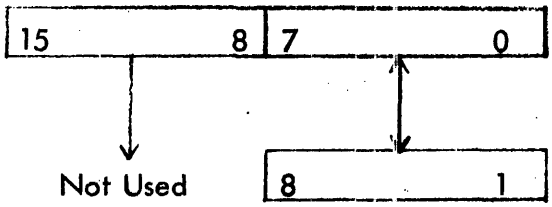
3.2.3 Interrupts

The interrupt functions are implemented on an individual system basis. SEN 1 and SEN 2 are implemented with individual drivers. SEN 0 and SEN 7 are "ORed" together on the same driver. All may be "ORed" together if desired.

3.3 Word/Character Format (UASC to CPU)

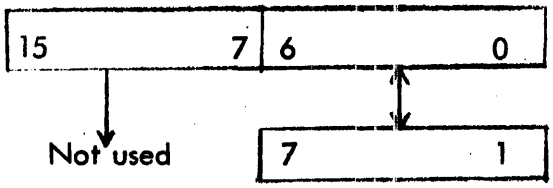
Only data is transferred. Parity, if selected, is not transferred as part of data to or from the CPU.

3.3.1 16 Bit Word - 8 Bit Character



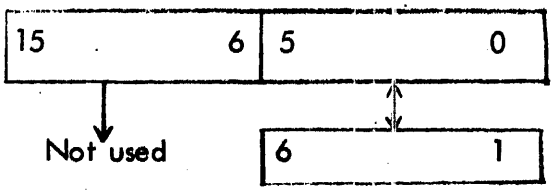
Transmitted or received character

3.3.2 16 Bit Word - 7 Bit Character



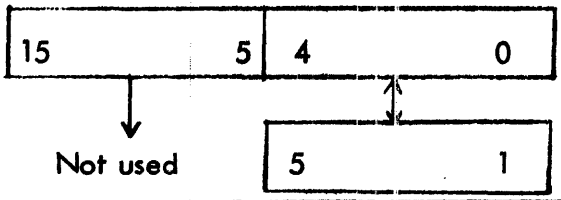
Transmitted or received character.

3.3.3 16 Bit Word - 6 Bit Character



Transmitted or received character.

3.3.4 16 Bit Word - 5 Bit Character



Transmitted or received character

SECTION IV
APPLICATION DATA

4.1 General Data

As previously mentioned in Section I, the controller is available in several versions. The general purpose nature of the controller logic and the three available interface types makes it adaptable for use in many applications where a serial bit/non-modem type interface is required. It is suggested that the user read and study this entire section prior to attempting operation.

The chart below gives the general characteristics of each model along with the cable length/rate restrictions.

FIGURE 4.1

Model	Serial Rate, BPS (bits per second)	Character Size	Stop Bit	Cable and Distance	Miscellaneous
RS232	45 to 9600 bps depending upon cable length (See Fig. 4.2)	5,6,7, or 8 level (bits). Parity bit (if any) is added to the data bits.	One or Two	Standard length=20ft., optionally up to 100ft.	
Current Mode	Same as RS232	Same as RS232	Same as RS232	Standard length=20ft. optionally up to more than one mile	User must provide "line battery" for loop current.
Relay	45 to 330 bps. Typically would be 75 or 110 bps. Relays will not operate reliably at higher than 300 bps.	Same as RS232	Same as RS232	Same as current mode	Same as current mode.

4.2 Cable Length Versus Rate of Operation

As noted in Figure IV, the RS232 model cable length is restricted to 100'. The RS232 interface is not isolated and operates in a voltage mode as set forth in RS232 B and C. Therefore, the maximum cable distance must be observed. RS232 is typically restricted to 50 feet of cable distance, but usually operates well up to 100 feet. The other models operate on a current loop (isolated interface) basis and cables can be much longer. Table below gives some general guidelines. Cables should be twisted pair using 24 gauge (or larger) wire. Note that maximum operating rate of the relay version is 330 bps so Figure 4.2 applies primarily to the Current Mode version.

FIGURE 4.2

Cable Length	Rate in BPS
Distance up to 1,000 feet	10,000 bps maximum
Distance up to 2,000 feet	4,800 bps maximum
Distance up to 3,500 feet	1,800 bps maximum
Distance up to 5,000 feet	900 bps maximum
Distance up to 10,000 feet	300 bps maximum

4.3 Version Selection

The three versions of the controller will cover a wide field of applications. The version of controller to be used depends primarily on the peripheral device interface. For example, a full-duplex terminal with an RS 232 I.F. (capable of operating with a 103 or 202 modem), but located within 100' of the computer, can usually be driven via the RS 232 version controller by adding a few jumpers at the peripherals (modem) connector. Typically, the modem control leads are jumpered "on" simulating the presence of the modem. "On" can be maintained by tying +12Vdc thru the IK source to the control lead pins.

In the case where a user needs an isolated interface, he would use the current mode or relay version of the controller.

The data below will assist users in configuring workable systems. Several application cabling examples are shown for each version of the controller following the general discussion of cabling, full/half duplex, 20/60 ma and line battery implementation.

4.3.1 Full-Half Duplex Discussion

All models can operate in a true (simultaneous send and receive) full duplex manner or in a send only, receive only, send or receive - half - duplex manner.

If the controller is cabled up in a full duplex (4 wire) manner, it will not see a reflected (echoed) input of what it is sending. If, however, the controller is cabled up in a half-duplex manner (only one pair of wires used), the outputted data on the send circuit will be reflected (echoed) back into the controller's receive section as input. The CPU software must ignore this "echoed" input during output of a message in this case. See cabling examples and discussion of signal routing.

4.3.2 20/60 MA Current Mode Operation

The Current Mode interface is limited at 20 to 60 MA operation. Two 2K-2 Watt dropping resistors are provided for use with a fixed voltage current source such as a model 33 or 35 teletype. Etched pads are provided for jumpering out the 2K resistors if a variable voltage current source (line battery) is available. The current loop interface provides DC isolation up to 500Vdc. If the user supplies the line battery, this isolation will be maintained. If loop current is derived from the 12V source on the controller board, isolation at the controller end is lost.

4.3.3 Relay Current Loop Operation

The relay current loop is limited to 20 to 60 MA operation as well as the discrete current loop. 2K-2 Watt dropping resistors are provided for use with fixed voltage current sources (line battery), such as a model 33 or 35 teletype. Normal relay isolation is obtained with this interface when line battery is supplied by user.

4.3.4 One and a Half Stop Bits

Although the user has the ability to select only one or two stop bits, he can operate with a 1-1/2 stop bit format. This is done by simply selecting two stop bits. For a Transmit function, the end result is that the maximum transfer rate is lowered by 1/2 bit time per character. For Received data, the controller ignores the second stop bit completely. Thus, the 1/2 bit time can be handled nicely and without noticable speed reduction.

4.3.5 Line Battery Requirements

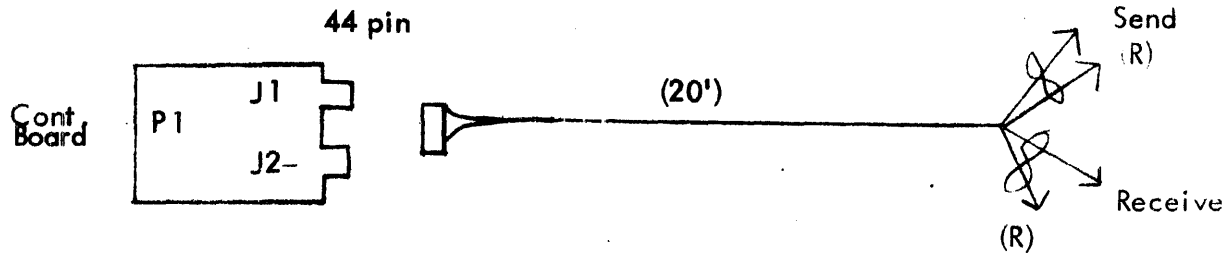
VDM may provide a controller only or a peripheral device along with the controller. If both the controller and VDM peripheral device is provided, VDM will supply "line battery". If VDM provides the controller only, the user (or peripheral supplier) will normally supply "line battery".

4.3.5.1 What is "Line Battery"?

This is normally a power source (supply) capable of providing enough current for "loop" operation. In the case of a 20ma, full duplex loop application, a power supply capable of supplying 20ma to both loops is required. Voltage for proper operation of the VDM current loop (or relays) can be from 12V to 100V at 60ma maximum. Besides the power supply itself, a means of adjusting (and/or regulating) the amount of current is required. A trimpot or fixed resistor network (per loop supplied) is adequate. One "battery" supply can supply many current loops; Typically, a one amp, 24Vdc supply could handle 20 (20ma-full duplex) controller-peripheral device hookups. VDM suggests usage of a barrier strip approach for a multiple relay type loop installation. See next pages. Use of an isolated "separate" power supply is the preferable method of implementing line battery.

4.4 Assembly of Cable (to peripheral device)

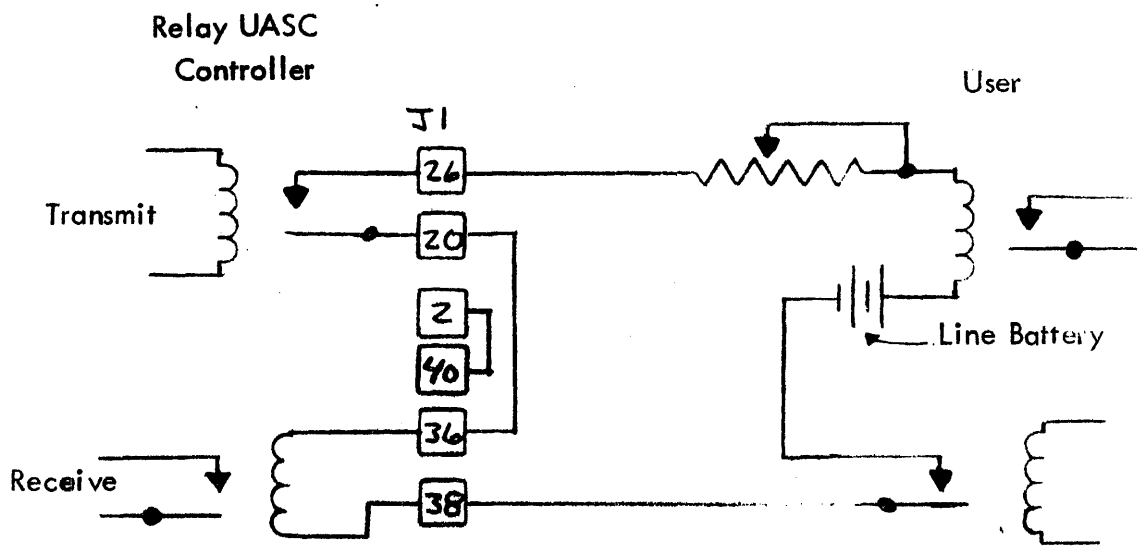
VDM provides a 20' open-ended cable kit with each controller. This cable kit includes a 44 pin Burndy type edge-on connector and hood, extra pins, and two twisted pairs in a jacket. The user makes up his cable to fit the application. See the examples for each type of controller. The cable routes from the top or bottom edge connector labled J1-J2 on the controller, to the peripheral device. (Reference: figure 2.1) The two pairs provided in the 20'cable kit are needed for "send" signals and "receive" signals. The twisted pairs are connected to the 44 pin connector as shown on the following pages. Wires required for operation with the (option) control and status lines are not included.



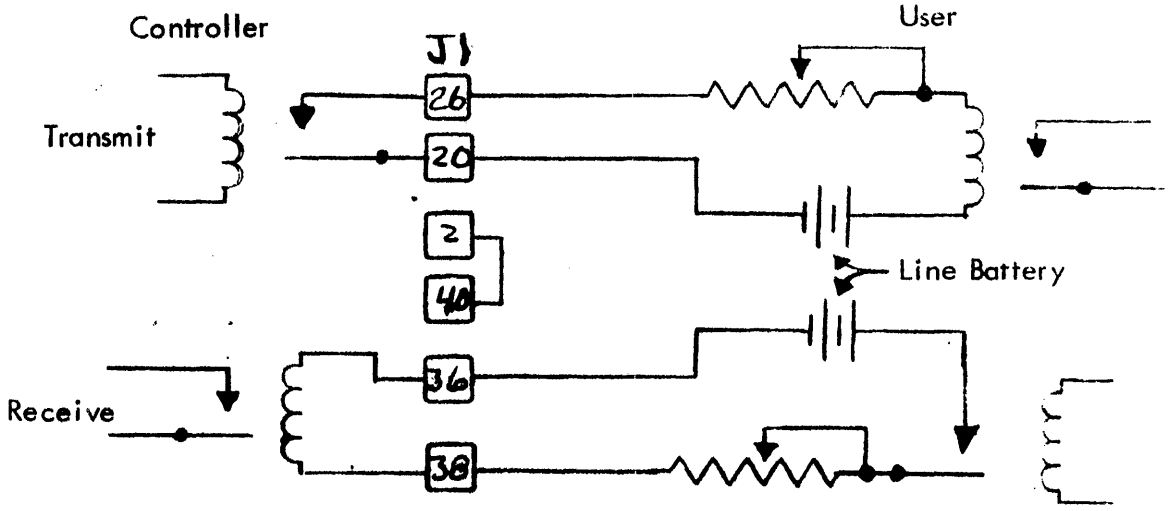
Users must determine the proper pin numbers at the peripheral device if the peripheral is not supplied by VDM.

4.4.1 Line Battery Hookup

4.4.1.1 Line Battery/Device Hookup - Half/Duplex



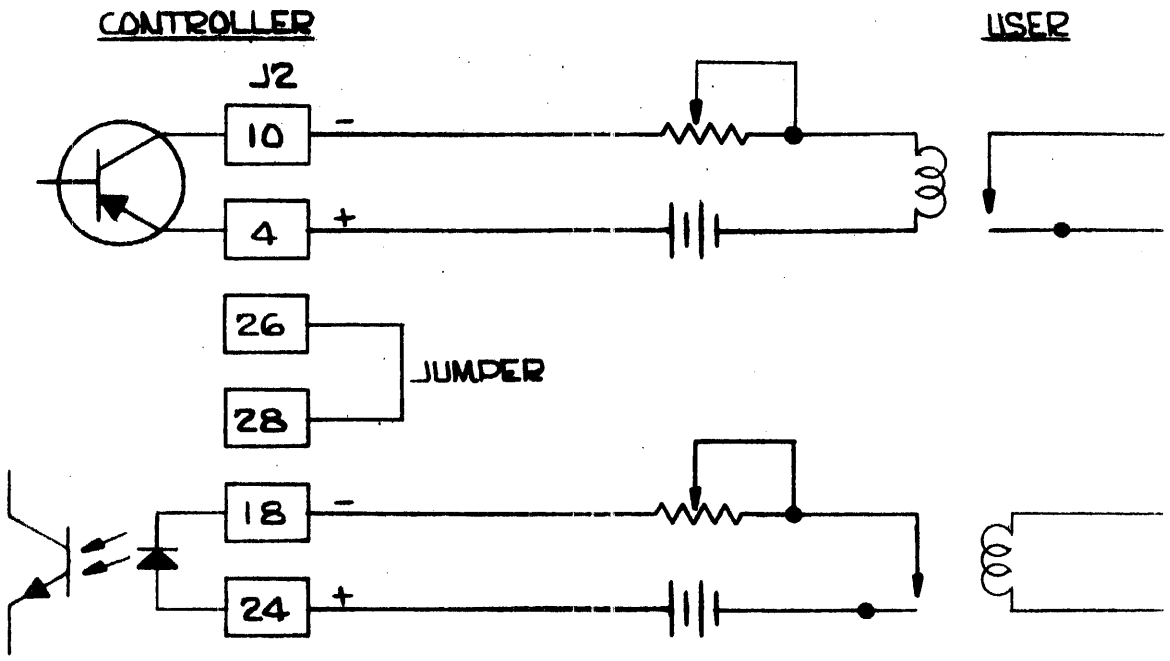
4.4.1.2 Line Battery/Device Hookup - Full Duplex



Note: Line Battery can be from one source if separate current limiting resistors are used.

4.4.1.3 Line Battery/Device Hookup - Full Duplex

Current Mode UASC

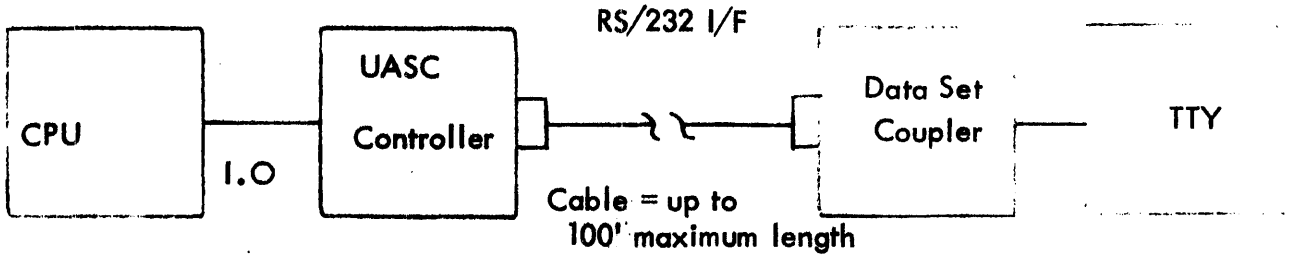


Note: As in 4.4.1.2, line battery can be one source if separate current limiting resistors are used.

4.5 Examples: Usage of RS232

4.5.1 Example #1 - Data Set Coupler

ASR-33 Teletype equipped with a dataset coupler.
Hardwire controller to 110bps, 2 stop bits, no parity, 8 bits. Hook-up cable as shown.



Dataset coupler
This is an RS/232 adapter normally used to interface to a 103 dataset

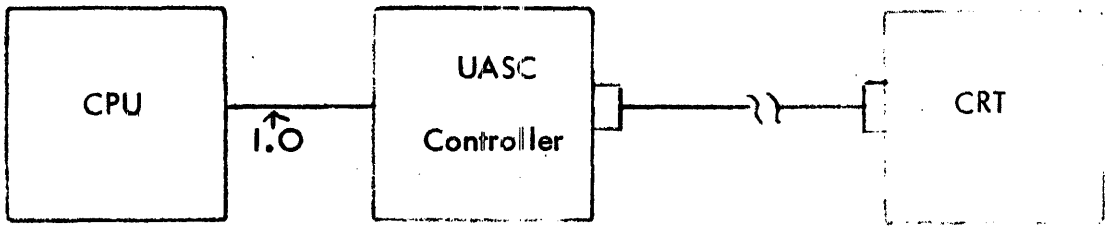
Signal Routing

UASC Pin	Signal		Dataset Coupler Signal
J2-36	SD	———	RD
J2-35	(R)	———	(R)
J2-42	RD	———	SD
J2-41	(R)	———	(R)
J2-44	←	Jumper	
J2-28			
J2-30	+V	———	CO-CTS-DSR

Tie to +V for "on" condition

4.5.2 Example #2 - CRT Hookup

CRT with RS232 I/F (202 Modem).. Hardwirecontroller to rate desired: Probably, 1200, 2400, or 4800 bps, 8 bits, 1 stop bit, parity.



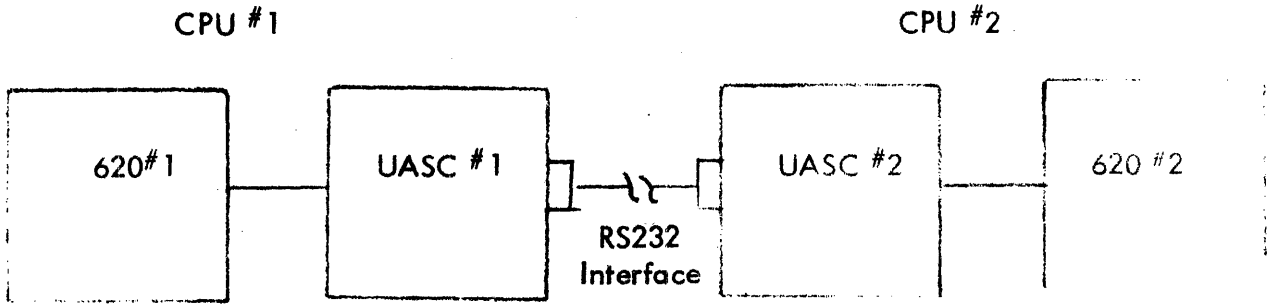
Cabling

UASC Pin	UASC Signal		CRT Signal
J2-36	SD	twisted pair	RD
J2-35	(R)	twisted pair	(R)
J2-42	RD	twisted pair	SD
J2-41	(R)	twisted pair	(R)
J2-30		CTS, CO, DSR	Tie to +V. For "on" condition

J2-44 ← Jumper → J2-28

4.5.3 Example #3 - 620 CPU to 620 CPU

Hardwire the controller to 2400, 4800, or 9600 bpi. Set character size to 8 bits plus odd or even parity, one stop bit. Hook up the cable as shown.



Cabling

#1 Controller		#2 Controller	
Pin	Signal	Signal	Pin
J2-36	SD	RD	J2-42
J2-35	R	(R)	J2-41
J2-42	RD	SD	J2-36
J2-41	R	(R)	J2-35
J2-44	Jumpers		J2-44
J2-28			J2-28

There are no control leads to "tie on" in this case.

J2-34	OPC	OPS	J2-40
J2-33	R	R	J2-39
J2-40	OPS	OPC	J2-34
J2-39	R	R	J2-33

Optional control capability

This hookup provides an additional control and status line.

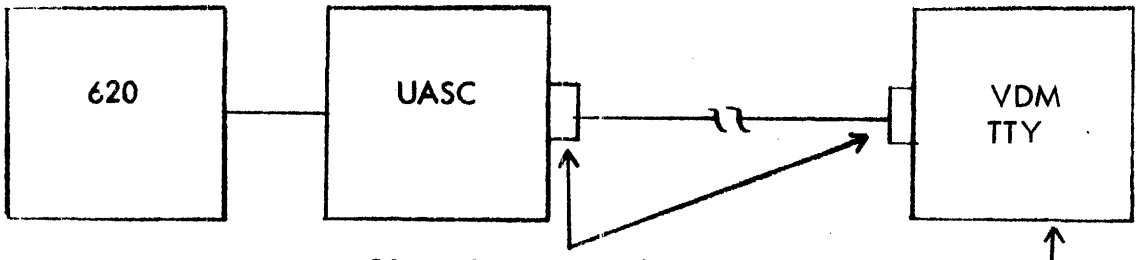
4.6 Usage of Current Mode Model

Unit has a solid state discrete current loop interface. It can typically be used to handle devices employing a current interface such as teletypes and/or terminals equipped with a 20/60ma current loop. Either half or full duplex operation is possible. This model has a major advantage over the RS232 interface in that the maximum cable length may be much longer. (See Figure 4.1). It has a major advantage over the relay interface in that the rate can be much higher than with electro-mechanical relays. See controller characteristics table and line battery discussion.

4.6.1 Example #1 - Interface to TTY

VDM modified KSR-ASR 33, 35 teletypes. Prepare the controller for 110 bps, 8 bits, no parity, 2 stop bits. Cable as shown.

Cable may be upito 10,000 feet long.



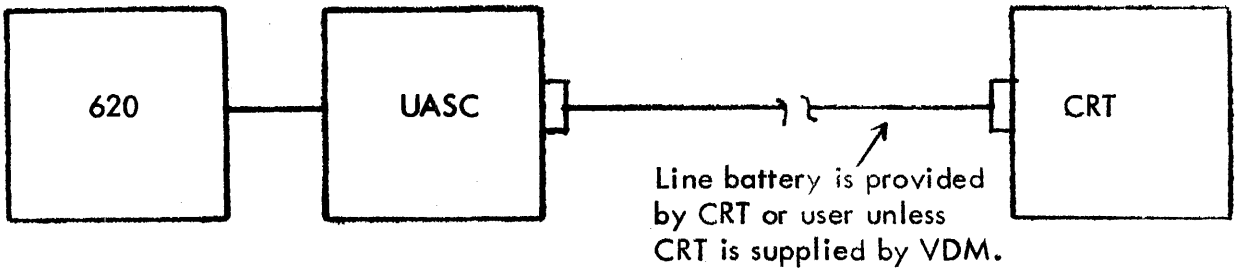
Line Battery is provided by a VDM mod to TTY - if purchased from VDM. TTY is enabled for 20 ma, full duplex, no parity operation.

Cable Signals Note: 2.0K current limiting resistors must be in place for this hookup.

UASC		ASR 33 TTY		KSR/ASR 35
Pin	Signal	Signal	Pin	Terminal Board
J2-10	SD	RD	P2-8	Terminal 7
J2-4	(R)			
J2-18	RD	SD	P2-6	Terminal 5
J2-24	(R)	(R)	P2-9	Terminal 4
J2-26	Jumper			
J2-28				

4.6.2 Example #2 - CRT Hookup

CRT equipped with "current loop". Hardwire the controller to: bps = 1200, 2400, or 4800 bps, 8 data bits, 7 data plus parity, one stop bit. Hook-up cable as shown. See rate/distance table for maximum length of cable.

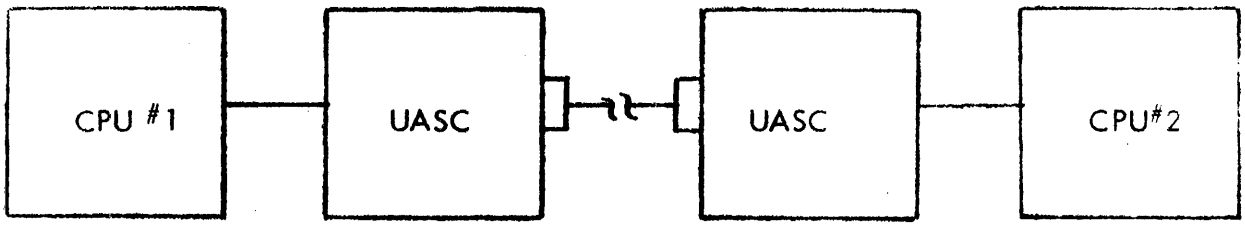


Cable Pin	Signal	CRT Signal
J2-4	SD	RD
J2-10	R	R
J2-24	RD	SD
J2-18	R	R
J2-26		
J2-28	Jumper	

Note: Current limiting resistors (R9 and R12) may require modification of value. 20ma min - 60 ma. max for logic "1".

4.6.3 Example #3 620 CPU to 620 CPU

Hardwire controller to: bps = 1200, 2400, 4800, or 9600 bps. Set to 8 bits plus odd or even parity, 1 stop bit. Hook up cable as shown. See rate/distance table for max. length of cable.



Cable hookup on next page.

4.6.3 (Cont'd)

Cable

UASC#1 (Master)

Pin	Signal
J2-4	SD+
J2-10	SD-
J2-14	20ma
J2-15	GND
J2-18	RD-
J2-24	RD+
J2-17	GND
J2-16	20ma
J2-26	Jumper
J2-28	

Jpr

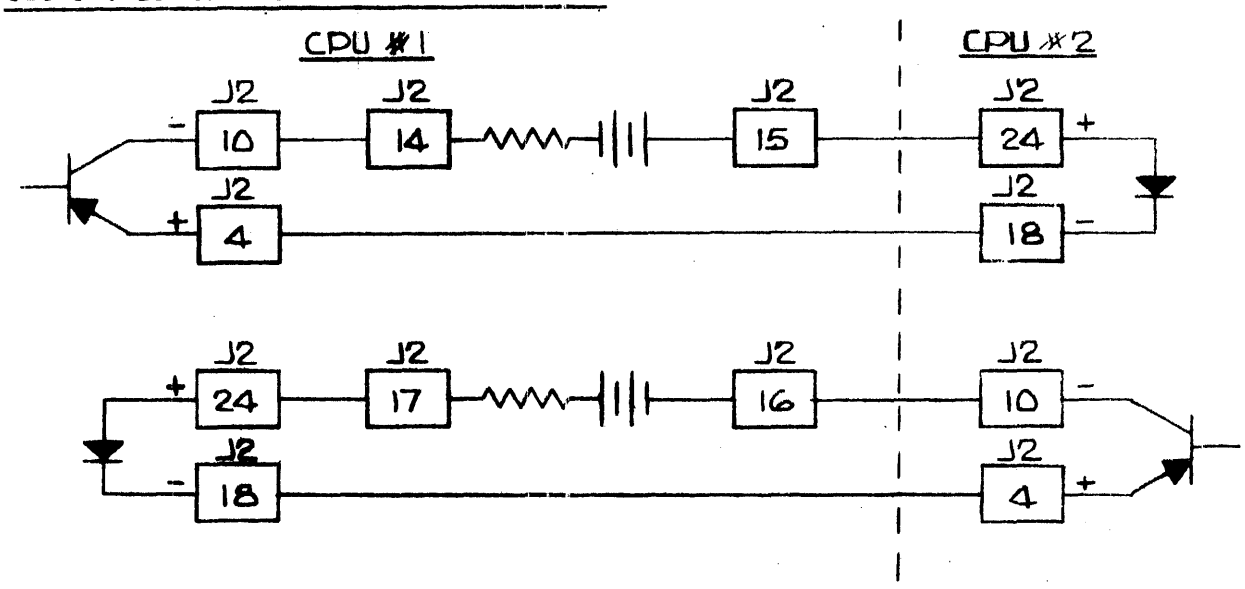
Jumper

UASC#2 (Slave)

Signal	Pin
RD-	J2-18
RD+	J2-24
SD+	J2-4
SD-	J2-10
Jumper	J2-26
	J2-28

Note: Current limiting resistors R9 and R12 on both ends are shorted out for this application.

620-620 Current Mode Interface Schematic



4.7 Usage of Relay Version

This model is equipped with a set of electromechanical (reed) relays and is designed for usage with teletype-telegraph (current loop) type equipment. It can handle 5 or 8 level applications such as (5 level) models 28, 32 (8 level) models 33 and 35 teletypes and 83B type polling (5 level) equipment. The relay interface can be hooked up to handle full or half-duplex "loops" as required. In the case of half-duplex operation, the CPU must ignore the "received" input while it is sending. The "received" input (while sending) is an "echo" only.

4.7.1 Full Duplex - Cable Routing - Schematic

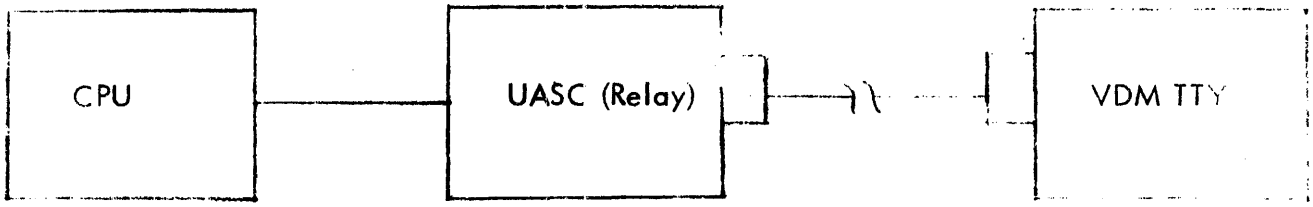
See 4.4.1.2

4.7.3 Examples - Usage of Relay UASC

Example #1 - ASR/KSR 33 and ASR/KSR 35

VDM provided 33/35 Teletype = same hook-up as 4.6.1.

Cable Routing



Cable Routing

UASC

Pin	Signal		Signal	ASR 33	ASR 35
J1-26	SD	———	RD	P2-8	TB-7
J1-20	R				
J1-36	RD	———	SD	P2-6	TB-5
J1-38	R	———	R	P2-9	TB-4
J1-2					
J1-40		Jumper			

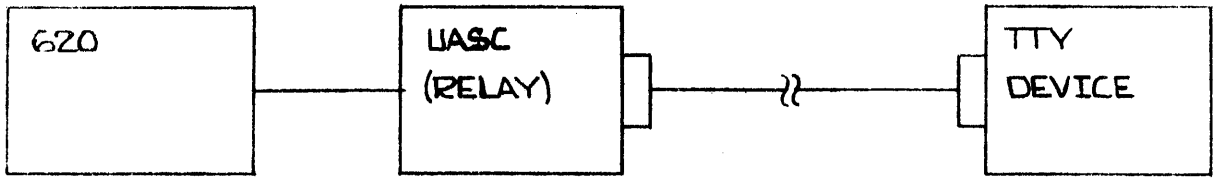
Note: The 2.0K and 2.7K resistors (R13 and R14) must be in place when the UASC is interfaced to the TTYs as noted above.

4.7.4 Example #2 - 5 Level TTY

620 CPU to user provided model 28 or 32 teletype or 83B unit.

Hardwire the controller to:

75 bps, 5 bit data, no parity, 2 stop bits, probably 60ma. Route cable and line battery as shown. See cable distance chart.



Signal Cable

See general cabling and previous page. Route cable for full or half duplex operation as required.

Half duplex - one pair cable used (ref: 4.4.1.1)
Full duplex - two pair cable used (ref: 4.4.1.2)

SECTION V
TESTING

5.0 General

The three interfaces, RS232, Current Mode, and Relay can be tested in a back-to-back configuration. Included in the UASC package is a test connector kit which can easily be assembled for the version purchased. The relay version can be tested when used with a TTY with standard VDM TTY test routines. VDM tests controllers prior to delivery using Test Specification 98A0768 as a guide.

5.1 Test Routine

The test routine requires that the UASC is installed in a 620 CPU slot with a properly wired test connector. Procedure for using this test routine is described in SPS 89A0228. This SPS also includes a description of the Test Routine.

5.2 Test Connector

The test connector is supplied in kit form. The test connector is assembled and used as further described.

5.2.1 Assembly of Test Connector

5.2.1.1 Model A - RS232C Test Connector

Install jumpers between the following pins:

36 to 42
44 to 28
34 to 40

Install test connector on J2.

5.2.1.2 Model B - Current Mode Test Connector

Install jumpers between the following pins:

10 to 14
4 to 18
24 to 23
26 to 28
22 to 38

R9 and R12 must be temporarily jumpered (shorted)

Install test connector on J2.

5.2.1.3 Model C - Relay I/O Test

The relay version of the UASC can most easily be tested with a VDM modified ASR 33 teletype. The cable is wired per 4.7.3. Standard teletype test routines will verify operation.

SECTION VI
THEORY OF OPERATION

6.0 General

Sections 1 thru 5 should be reviewed prior to using this Theory of Operation section. This section is written in a sequence that begins with the logic on page 1 and follows through to page 6 of 91C0445.

6.1 Control Logic

6.1.1 Page 1

Contains power distribution, D.C. line filtering, and E-Bus connections. DAXX+, the Device Address, is made up of a 7 input "AND" function which is selectable at P1 on the back panel. Reference 2.5 and Fig. 2.2.

6.1.2 Page 2

Contains the balance of the E-Bus connections which are further defined in the 620 interface manuals. CODO+ thru COD7+ are decoded at octal to 8 line decoder IC2. CODO+ thru COD7- are used for both Sense and Command Instructions (Reference 3.1). EXC Commands are made up of FRYX (Function Ready), EB11+, DAXX (Device Address), and the appropriate COD(X) functions. WBBC is a nand gate latch which is set (EXC 0 or EXC 1) when transferring data out under BIC control. The latch is reset (EXC 2 or EXC 5) when transferring data in under BIC control. INIT (Initialize) is implemented on a "one shot" to assure that the LSI chip has a 2 usec reset pulse. INIT is pulsed by either a "SYSTEM RESET" from the control panel or an initialize command, EXC 4. OPON flip flop is set by EXC 6 and reset by EXC 7. OPON is storage for a control line that can be used for various different peripheral devices, an optional control.

6.1.3 Page 3

Generally contains data control, interrupt drivers, and BIC control logic. The following terms are BIC oriented and are further defined in the BIC manual TAKK (Trap Acknowledge), DCEX (Device Connect Enable), CDCX (Controlled Device Connected), TROX (Trap Out), BCDX (BIC Disconnect), and TRQX (Trap Request). DTOX (Data Transfer Out) and DTIX (Data Transfer In) are used to steer data onto the E-Bus during data transfer commands such as an OAR or CIA instruction (Ref. 3.1).

The three interrupt drivers, TXRINT, RCRINT, and E/BINT are implemented as pulse drivers. Pulses are generated at the leading edge of the associated sense response term. For example, TXRDY- (Transmit Ready) initiates TXRINT.

(PIM Driver Pulse) at the leading edge of TXRDY+. The interrupt drivers are pulsed to permit hardwire "OR'ing" of all three drivers to one PIM input.

6.1.4 Page 4

Contains the Sense response logic, the E-Bus drivers, and amplified outputs from the LSI chip. The Sense logic consists of the decoded control function bits (EB06, EB07, and EB08) which are decoded to CODO thru COD7 on page 2 of 91C0445. CODO is gated with FEB+ to obtain the first term in the Sense structure. CODO thru COD7 is used to implement SEN 0 thru SEN 7 respectively (Ref. 3.1).

6.1.5 Page 5

Consists of the LSI Transmitter/Receiver chip and the four types of interface to the user. The LSI chip is covered in Section 6.2. Only one of the three optional interfaces will be found on a given board. The interface circuit specifications are found in Section II.

The RS232 interface is driven via IC21 for both TXDAT2 (Transmit Data) and OPCON2(Option Control). RECDAT2 (Receive Data) and OPTION (Option Status Line) are received via IC 28. Both IC 21 and IC 28 are RS232 B & C compatible.

The Current Mode interface does not utilize the Option Control and Option Status lines. TXDAT1 (Transmit Data) is DC isolated via transformer coupling from signal ground. OSC1 running at a 2.3 MHZ rate transfers the output data (SD+) to the secondary of T1 via IC7. The pulsed data seen on the primary of T1 is effectively rectified by CR1. The voltage divider R7 and R8 properly bias the output driver Q1 which reconstructs the SD+ signal. Input data is also DC isolated from signal ground via an LED/Transistor, IC14.

The Relay interface is mechanized to permit utilization of 3 or 4 wire connections. Transmit Data is sent via K1 by means of a contract closure. Receive Data is received via K2. Normal D.C. isolation from signal ground is obtained with the relay interface.

The DTL/TTL interface is present on all three of the previously described interfaces. In fact, the other three interfaces utilize the DTL/TTL interface. The Receive Data is routed to RD at J1 or J2 and thru IC12. As an example the RS232 Receive Data line RD2 at J2-44 must be routed back thru the DTL/TTL receiver RD at J2-28. The optional control and Status lines OPCON1 and OPTION at J2-22 and J2-38 respectively are also always present on the three versions of the UASC. The DTL/TTL Transmit Data driver (TD at J2-2) is also always present on the three versions.

6.1.6 Page 6

Is covered in Section 6.3 .

6.2 Transmitter/Receiver Operation

6.2.1 Transmitter Operation

(Ref. Fig. 6.1, 6.3, and 6.5)

Power is applied, external reset is enabled and a clock pulse is applied having a frequency of 16 times the desired baud rate. The above conditions will set TXRDY+, TRE+, and SD+ to logic "1" (Line is marking).

Once data strobe BTOA- is pulsed the TXRDY+ signal will change from a logic "1" to a logic "0" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SD+ and TRE+ going to a logic "0", and TXRDY+ will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering.

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, TRE+ will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TXRDY+ is a logic "0" as was previously discussed.

It should be noted that the TRE+ line is not used. It can be used for timing reference when trouble shooting , however.

6.2.2 Receiver Operation

(Ref. Figs. 6.2, 6.4, and 6.6)

Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud rate. The previous conditions will set data available RCRDY+ to a logic "0".

Data reception starts when serial input signal changed from Marking (logic "1") to spacing (logic "0") which initiated a start bit. The start bit is valid if after transition from logic "1" to logic "0", the RD line continues to be at logic "0", when center

sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16x clock is in a logic "1" state, the bit time, for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in a orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip flop and/or the framing error flip flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditionaly set to a logic "0".

Once a full character is received, internal logic looks at the data available (DR) signal to determine if data has been read out. If the DR+ signal is at a logic "1" the receiver will assume data has not been read out and the over run flip flop of the status word holding register will be set to a logic "1". If the DR signal is at a logic "0" the receiver will assume that data has been read out. After DR goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.

6.2.3 Description of Pin Functions

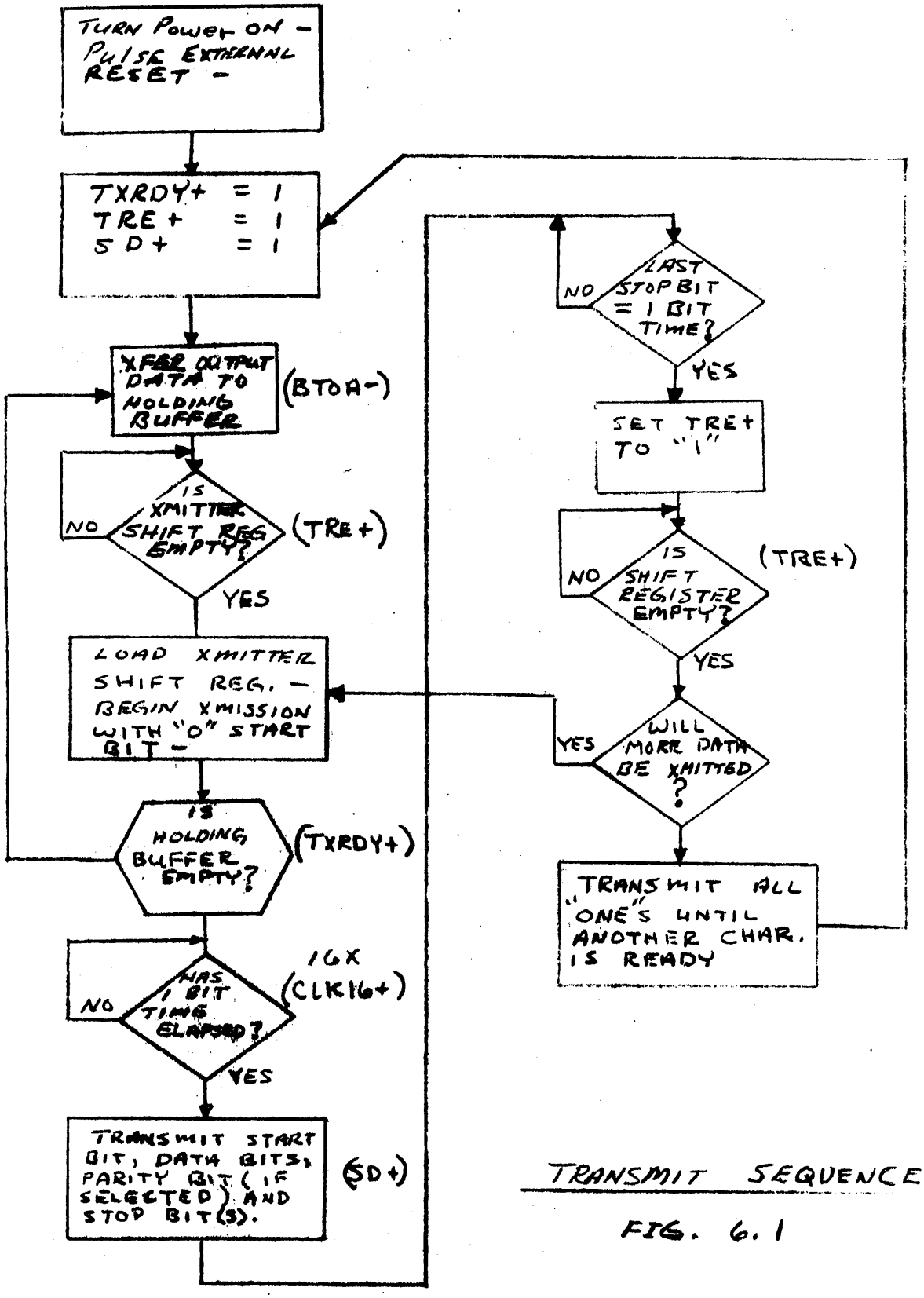
Pin No.	Name	Symbol	Function
1	V_{cc} Power Supply	V_{cc}	+5V Supply
2	V_{gg} Power Supply	V_{gg}	-12V Supply
3	Ground	GRD	Ground
4	Received Data Enable	RDE	A logic "0" on the receiver enable line places the received data onto the output lines. (Grounded)
5-12	Received Data Bits	RR7-RRO	These are the 8 data output lines. Received characters are right justified, the LSB always apprears on RRO.
13	Receive Parity Error	PE	This line goes to a logic "1" if the received character parity does not agree with the selected parity.

Pin No.	Name	Symbol	Function
14	Framing Error	FE	This line goes to a logic "1" if the received character has no valid stop bit.
15	Over-Run Error	OE	This line goes to a logic "1" if the previously received character is not read (DR line not reset) before the present character is transferred to the receiver holding register.
16	Status Enable	SE	A logic "0" on this line places the status bits onto the output lines. (Grounded)
17	Receiver Clock	CLK16	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	Reset Data	BTIA-	A logic "0" will reset the DR line. Data remains available until replaced with new data.
19	Receive Data Ready	DR	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register.
20	Serial Input	RD	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception.
21	External Reset	INIT	Resets all registers except RR7 - RR0 registers. Sets SD, TRE, and THRE to a logic "1".
22	Transmitter Buffer Empty	THRE	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character.
23	Data Strobe	BTOA-	A strobe on this line will enter the data bits into the data bits holding register.
24	End of Character	TRE	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character. (Not used).

Pin No.	Name	Symbol	Function
25	Serial Output	SD	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitte l.
26-33	Data Bits Out	EB00-07	There are up to 8 data bits used.
34	Control Level	CRL	A logic "1" on this lead will enter the control bits (PI, SBS, WLS1, WLS2, EPE) into the control bits holding register. This line is hard wired to a logic "1" level.
35	No Parity	PI	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0".
36	Number of Stop Bits	SBS	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop and a logic "1" will insert 2 stop bits.
37-38	Number of Bits/ Character	WLS2 WLS1	These two leads will be internally decoded to select either 5,6,7, or 8 data bits/character. WLS1 WLS2 Bits/Character 0 0 5 1 0 6 0 1 7 1 1 8
39	Odd/Even Parity	EPE	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock Line	CLK16	This is a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

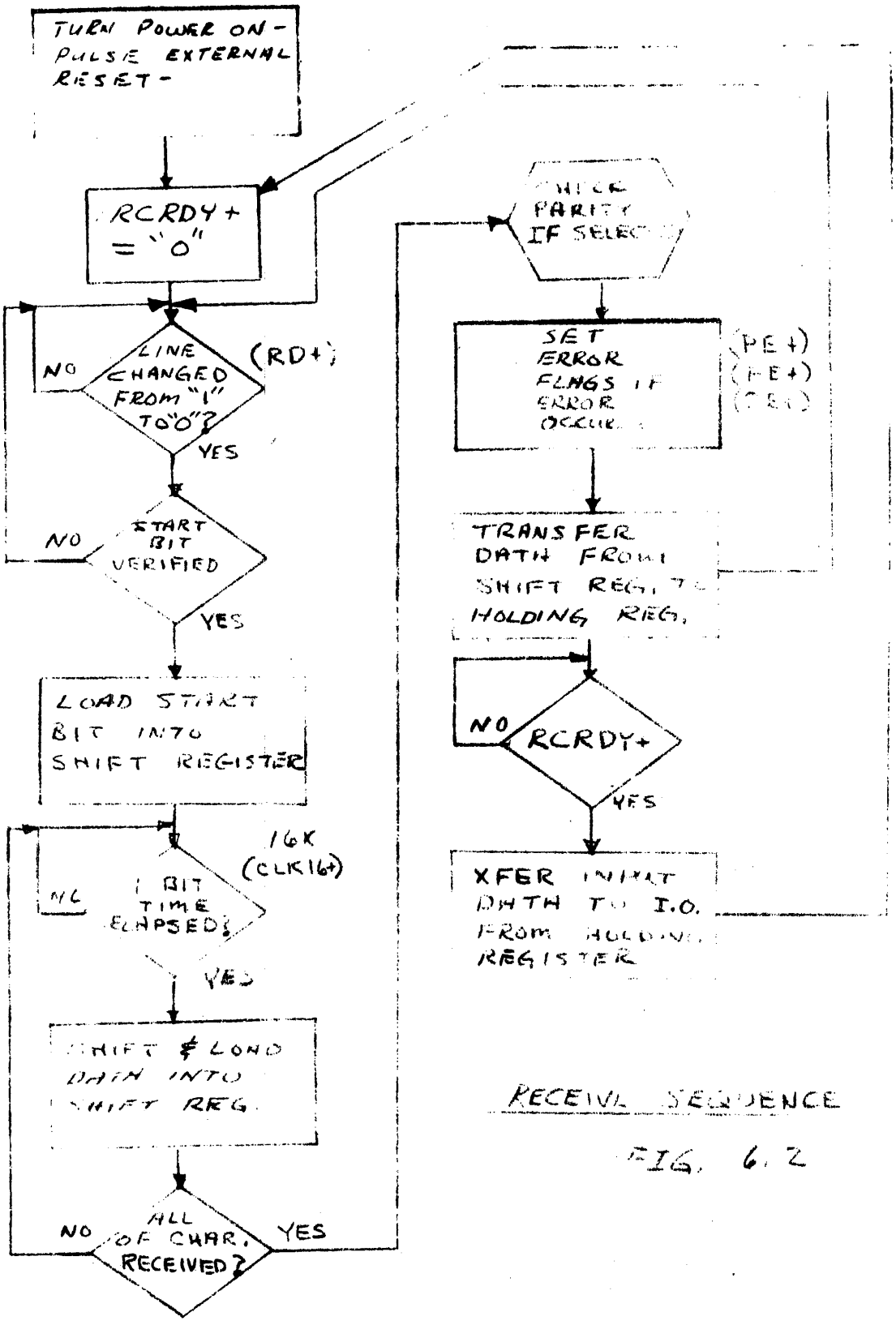
6.3.1 Timing

Page 6 contains the crystal oscillator and the presetable counter for dividing the clock frequency to 16 times the data or baud rate. OSC1 (IC33) divides the oscillator output (4.608MHZ) by two. OSC+ and OSC1+ are gated together to create a 2.304 MHZ input to the 12 bit presetable ripple counter (IC13, IC20, and IC27). The down going edge of the carry line at pin 12 of IC27 causes the reset flip flop RSFF to set. The alternate clock pulse (OSC- and OSC) is gated into the preset line (pin 1 of IC12, IC20, and IC27) to preset the counter. The preset pulse rate is governed by the jumper combination as shown in Table II, Sheet 6 of 91C0445. The leading edge of the next count pulse resets the reset or preset flip flop, RSFF. (Ref. Fig. 6.7).



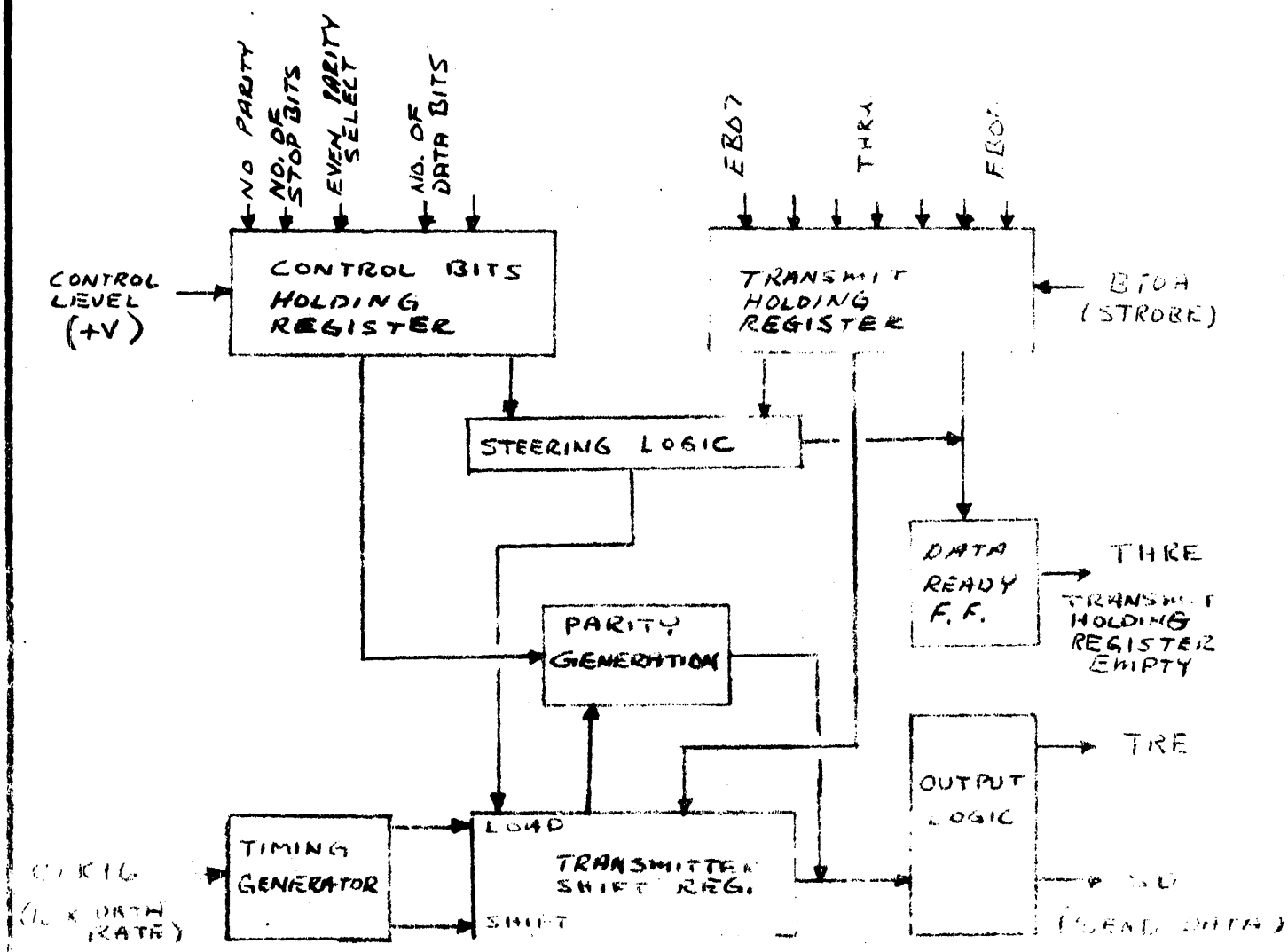
TRANSMIT SEQUENCE

FIG. 6.1



RECEIVE SEQUENCE

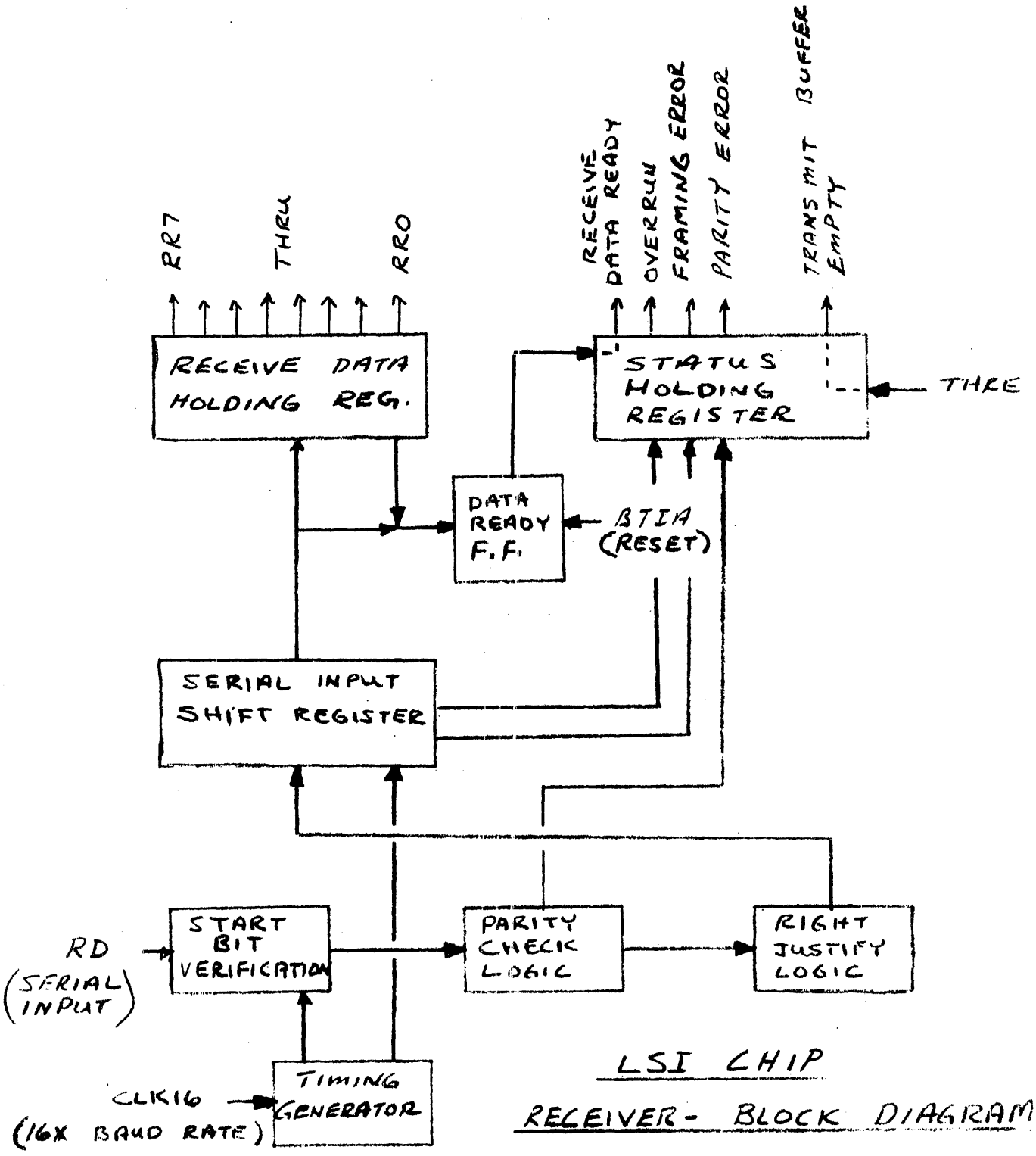
FIG. 6.2



LSI CHIP

TRANSMITTER - BLOCK DIAGRAM

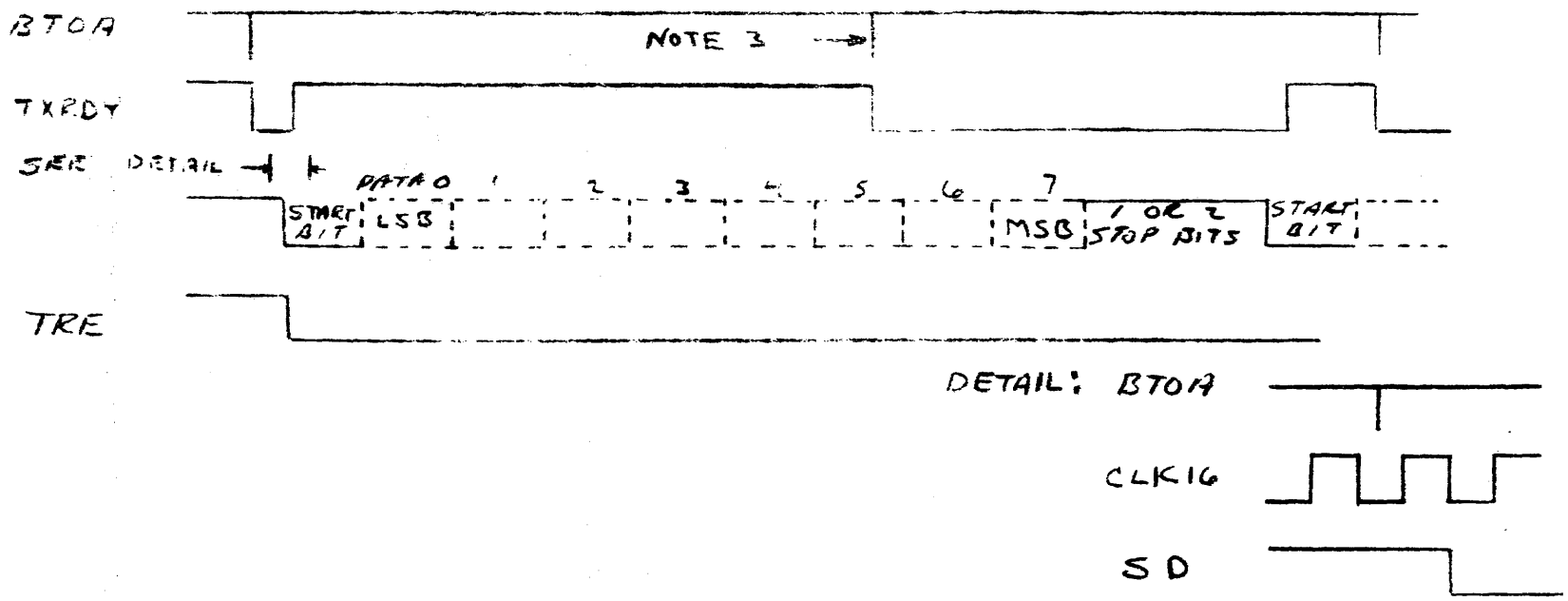
FIG. 6.3



LSI CHIP

RECEIVER - BLOCK DIAGRAM

FIG 6.4



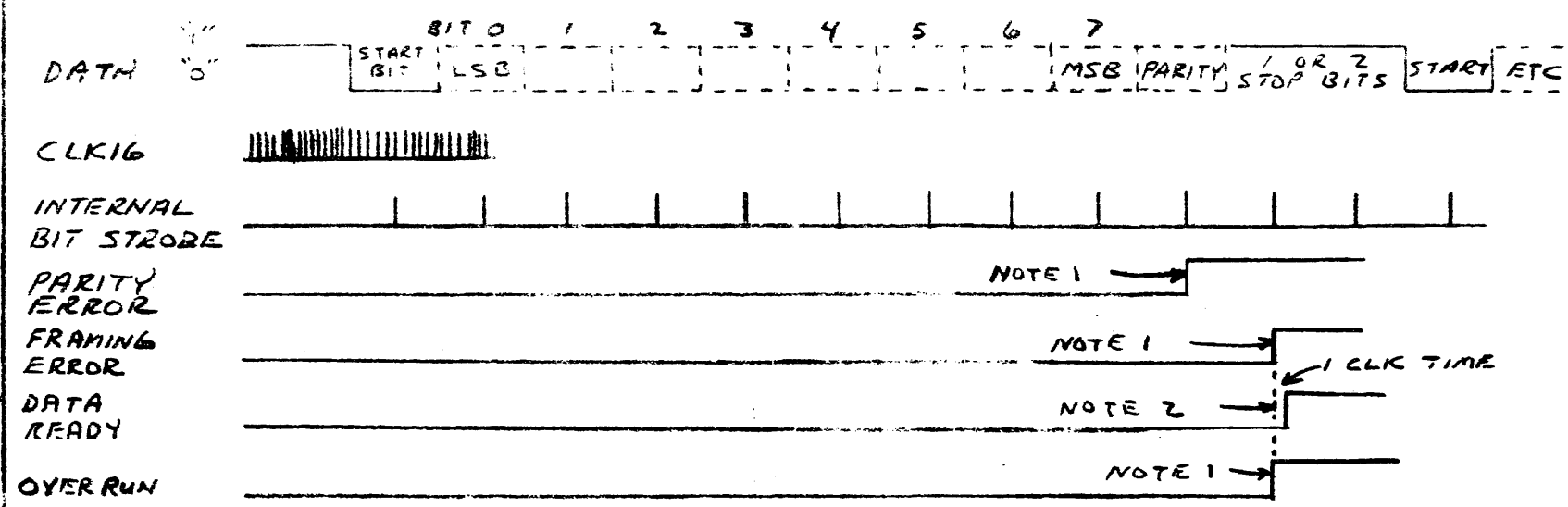
NOTE:

Transmitter initially assumed inactive at start of diagram. Shown for 8 level code and parity and two stops.

1. Bit time = 16 clock cycles.
2. If transmitter is inactive the start pulse will appear on line within 1 clock cycle of time data strobe occurs. See detail.
3. Since transmitter is double buffered another data strobe can occur anywhere during transmission of character 1.

LSI CHIP TRANSMITTER TIMING

FIG 6.5

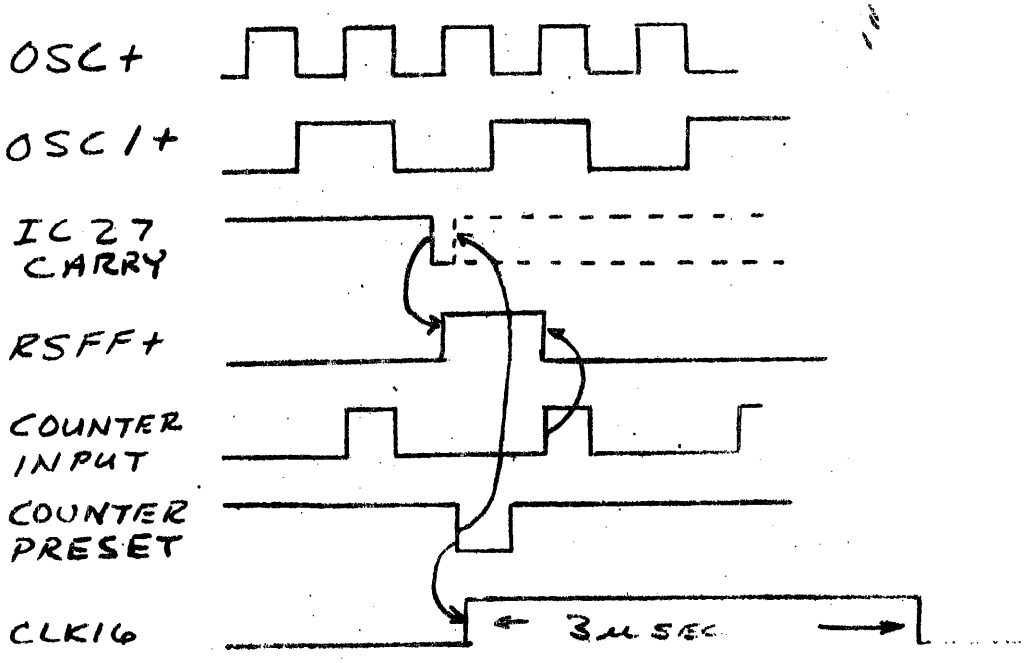


NOTES:

1. This is the time when the error conditions are detected, if error occurs.
2. Data available is set only when the received data, PE, FE, or has been transferred to the holding registers. (See receiver block diagram).
3. All information is good in holding register until data available tries to set for next character.
4. Above shown for 8 level code parity and two stop for no parity, stop bits follow data.
5. For all level code the data in the holding register is RIGHT JUSTIFIED; that is, LSB always appears in RRO (pin 12).

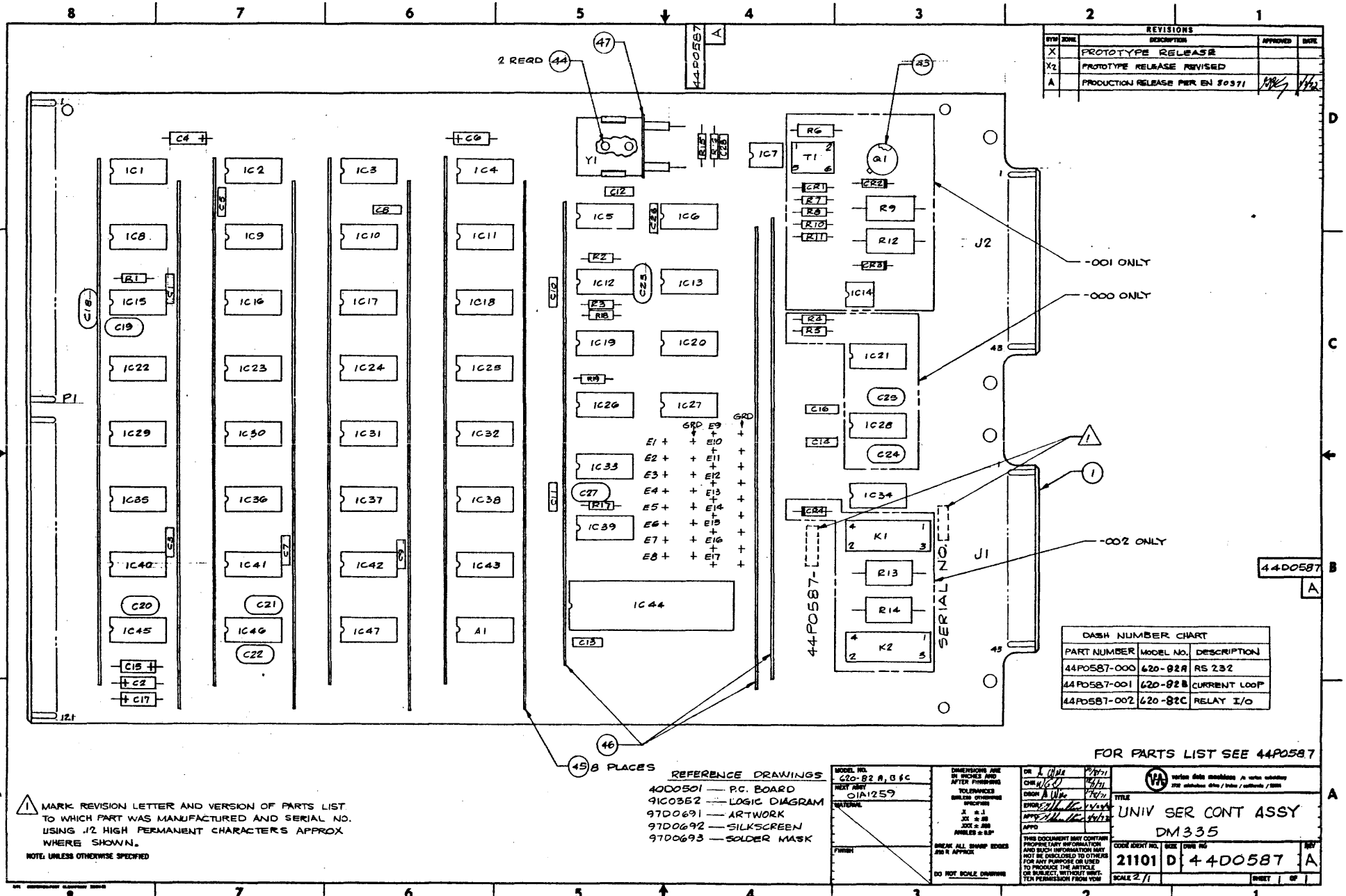
LSI CHIP RECEIVER TIMING

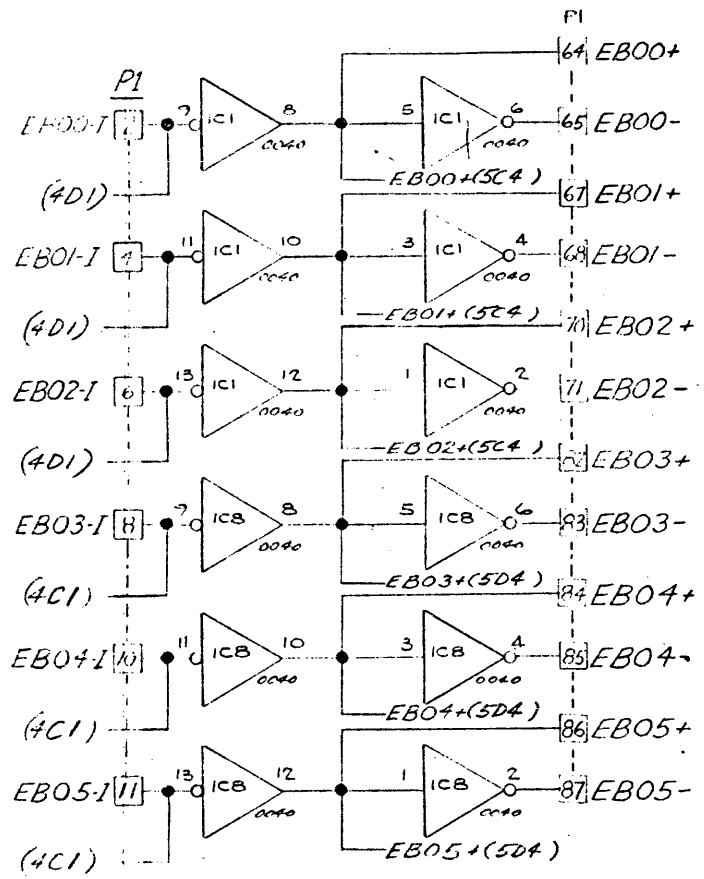
FIG 6.6

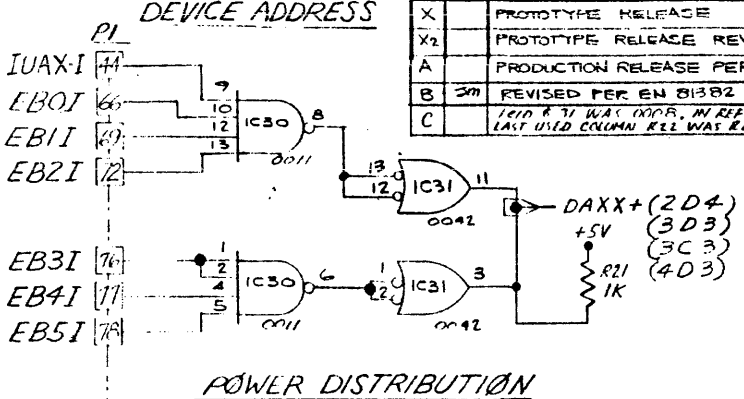


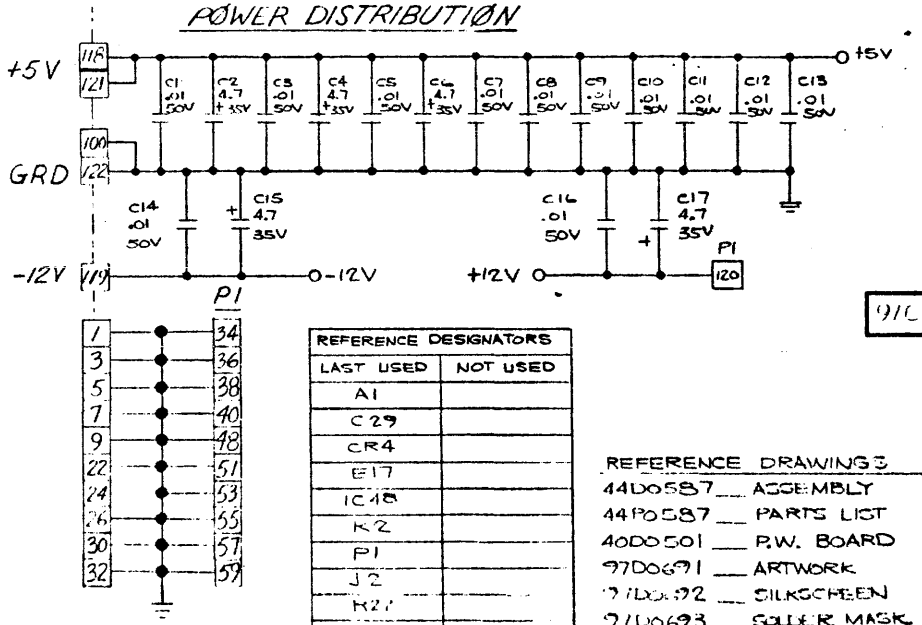
OSCILLATOR/ COUNTER TIMING

FIG 6.7


REVISIONS
SYM | ZONE | DESCRIPTION | APPROVED | DATE
X | PROTOTYPE RELEASE
X2 | PROTOTYPE RELEASE REVISED
A | PRODUCTION RELEASE PER EN 50371
2 REQD
44P0587 A
-001 ONLY
-000 ONLY
-002 ONLY
44P0587-
SERIAL NO.
J1
J2
P1
8 PLACES
44P0587 A
FOR PARTS LIST SEE 44P0587
DASH NUMBER CHART
PART NUMBER | MODEL NO. | DESCRIPTION
44P0587-000 | 620-82A | RS 232
44P0587-001 | 620-82B | CURRENT LOOP
44P0587-002 | 620-82C | RELAY I/O
REFERENCE DRAWINGS
4000501 — P.C. BOARD
9100352 — LOGIC DIAGRAM
9700691 — ARTWORK
9700692 — SILKSCREEN
9700693 — SOLDER MASK
MARK REVISION LETTER AND VERSION OF PARTS LIST TO WHICH PART WAS MANUFACTURED AND SERIAL NO. USING .12 HIGH PERMANENT CHARACTERS APPROX WHERE SHOWN.
NOTE: UNLESS OTHERWISE SPECIFIED
MODEL NO. 620-82 A, B & C
NEXT ASSY 01A1259
MATERIAL
FINISH
DIMENSIONS ARE IN INCHES AND AFTER FINISHING
TOLERANCES UNLESS OTHERWISE SPECIFIED
BREAK ALL SHARP EDGES .010 R APPROX
DO NOT SCALE DRAWING
DR J. CAMPS 10/19/71
CHK W.G.D. 10/21/71
DSGN A. WAN 11/4/71
ENGR
APPD
APPD
THIS DOCUMENT MAY CONTAIN PROPRIETARY INFORMATION AND SUCH INFORMATION MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE OR USED TO PRODUCE THE ARTICLE OR SUBJECT, WITHOUT WRITTEN PERMISSION FROM VDM
TITLE UNIV SER CONT ASSY DM335
CODE IDENT NO. 21101
SIZE D
DWG NO 44D0587
REV A
SCALE 2/1
SHEET OF







REVISIONS				
SYM	ZONE	DESCRIPTION	APPROVED	DATE
X		PROTOTYPE RELEASE		
X2		PROTOTYPE RELEASE REVISED		
A		PRODUCTION RELEASE PER EN 80371		4/1/72
B	3m	REVISED PER EN 81382		8/4/73
C		ADD R 21 WAS DOOR. IN REF DESIG BLOCK LAST USED COLUMN R22 WAS R10 EN 82285		8/14/73

REFERENCE DESIGNATORS	
LAST USED	NOT USED
A1	
C29	
CR4	
E17	
IC48	
K2	
P1	
J2	
R21	
T1	
Q1	
Y1	

REFERENCE DRAWINGS

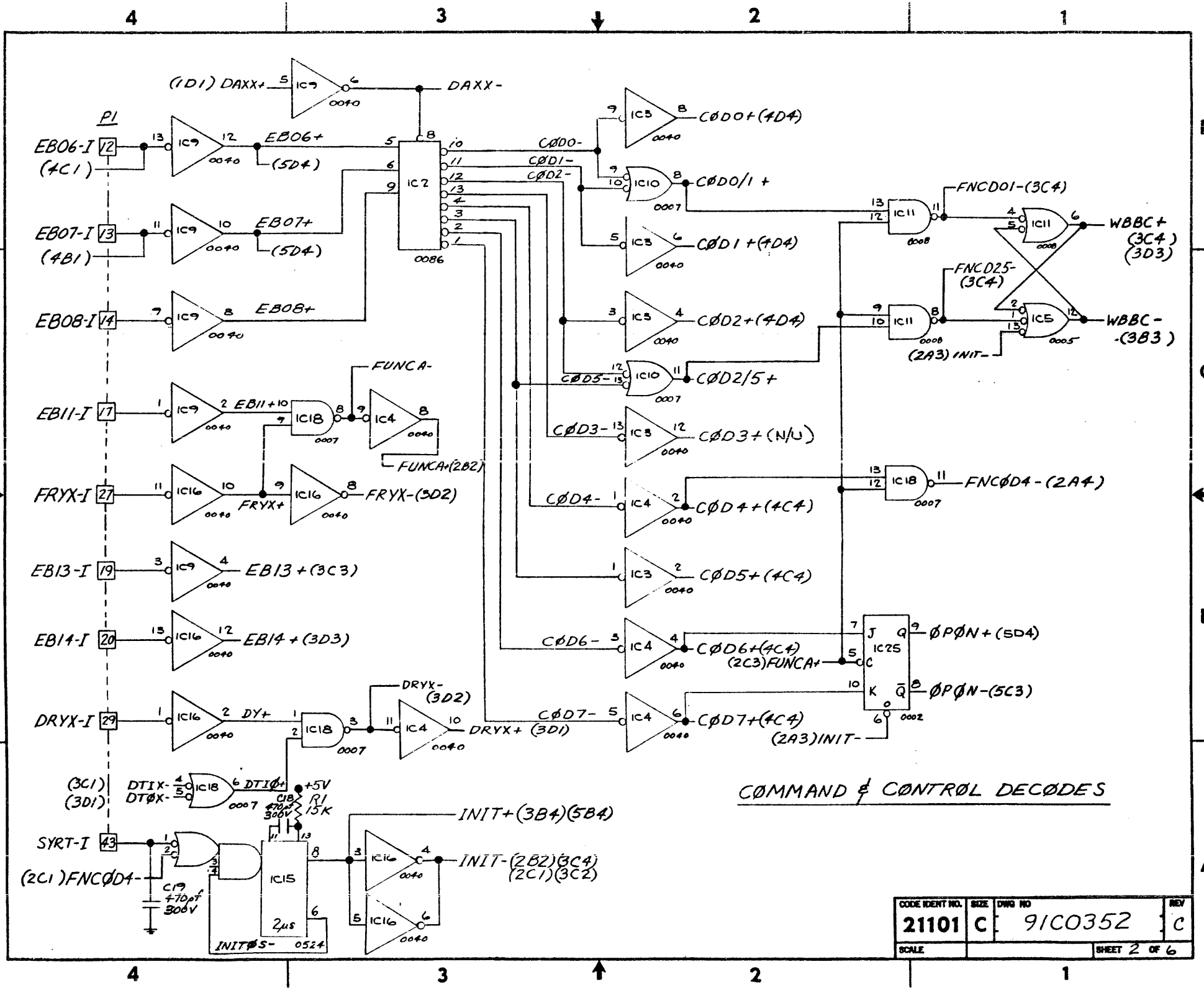
- 44D0587 ___ ASSEMBLY
- 44P0587 ___ PARTS LIST
- 40D0501 ___ P.W. BOARD
- 97D0691 ___ ARTWORK
- 97D0692 ___ SILKSCREEN
- 97D0693 ___ SOLDER MASK

5. R3 = 750Ω FOR -000 AND -002, R3 = 4.7KΩ FOR -001
4. POWER TO IC17,25 AND 33 IS GRD=PIN 11, +5V= PIN 4. (3 PLACES)
3. POWER TO IC's : PIN 14 = +5V, PIN 7 = GRD
2. ALL CAPACITOR VALUES ARE IN μf, 20VDC
1. ALL RESISTORS ARE ¼ W, 5%.

NOTES: (UNLESS OTHERWISE SPECIFIED)

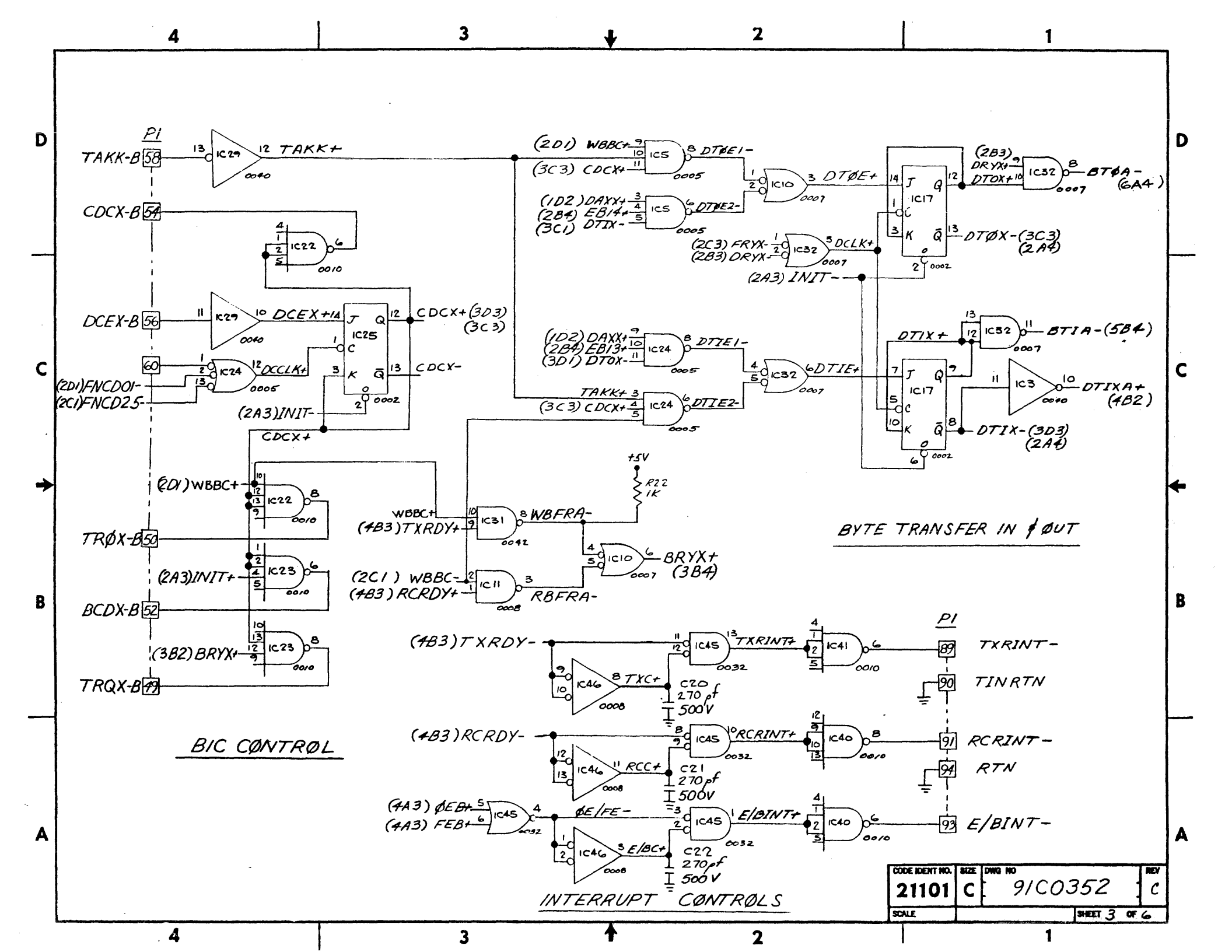
91C0352
C

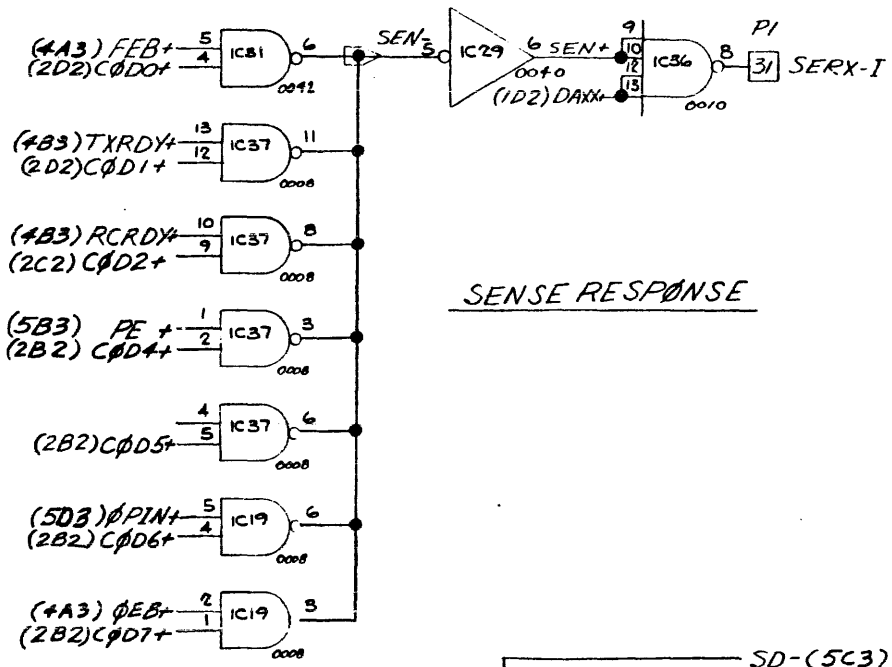
MODEL NO. 620-82 A, B&C	DIMENSIONS ARE IN INCHES AND AFTER FINISHING	DR C. Greenman 9-9-71	varian data machines /a varian subsidiary 2722 michelson drive / irvine / california / 92664
NEXT ASSY 44D0587	TOLERANCES (UNLESS OTHERWISE SPECIFIED) X ±.1 XX ±.03 XXX ±.010 ANGLES ± 0.5°	CHK [illegible] 9/9/71	TITLE LOGIC - UNIV SER CONT DM335
MATERIAL	BREAK ALL SHARP EDGES .010 R APPROX	DSGN	
FINISH	DO NOT SCALE DRAWING	ENGR [illegible] 9/14/71	
		APPD [illegible] 9/14/72	
		APPD	
		THIS DOCUMENT MAY CONTAIN PROPRIETARY INFORMATION AND SUCH INFORMATION MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE OR USED TO PRODUCE THE ARTICLE OR SUBJECT, WITHOUT WRITTEN PERMISSION FROM VDM	CODE IDENT NO. 21101 / SIZE C / DWG NO 91C0352 / REV C / SCALE / SHEET 1 OF 6



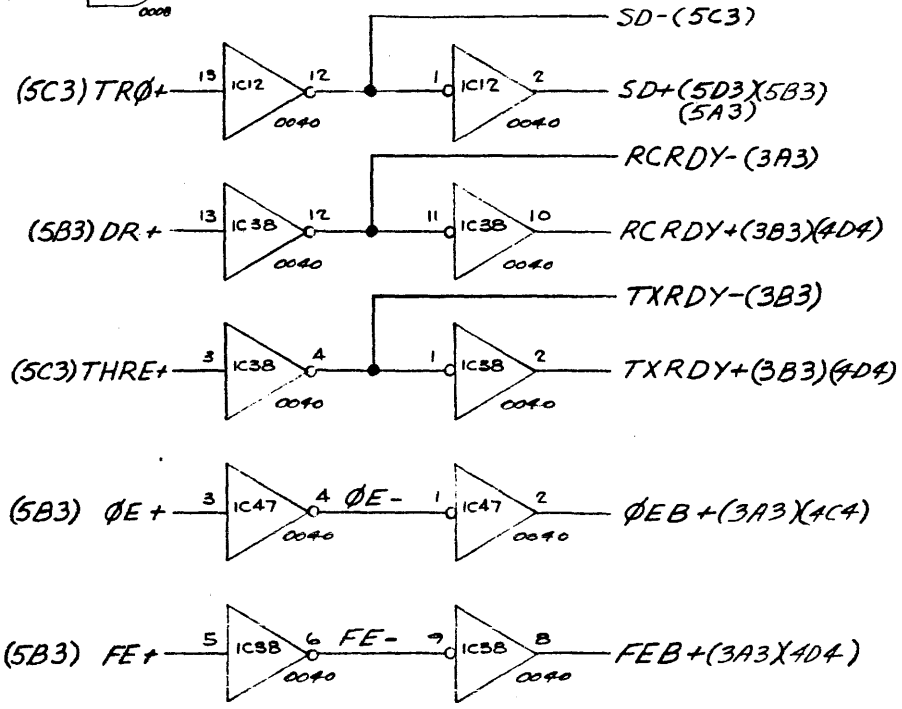
CØMMAND & CØNTRØL DECØDES

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0352	C
SCALE		SHEET 2 OF 6	

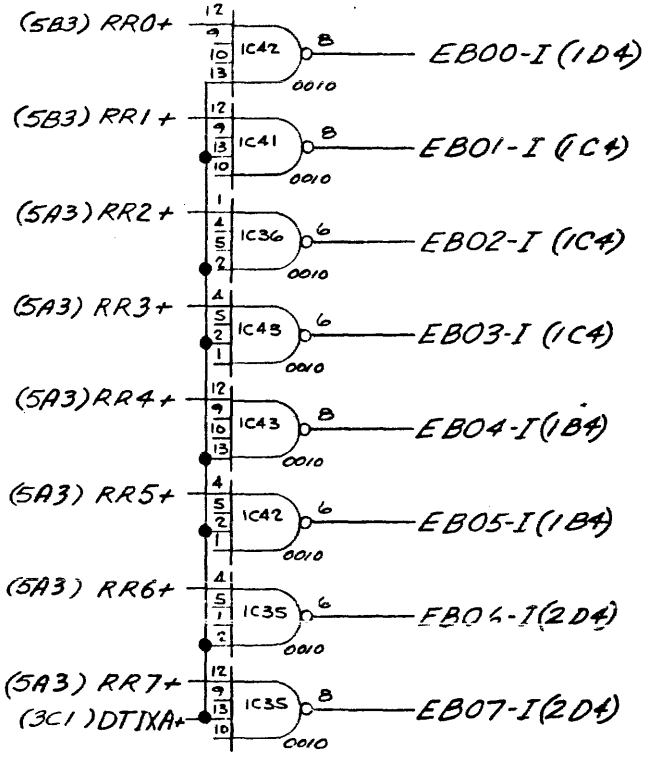

P1
TAKK-B 58
IC29
TAKK+
CDCX-B 54
IC22
DCEX-B 56
IC29
DCEX+1A
IC25
CDCX+ (3D3) (3C3)
CDCX-
60
IC24
DCCLK+
(2D1) FNCD01-
(2C1) FNCD25-
(2A3) INIT-
CDCX+
(2D1) WBBC+
IC22
TRØX-B 50
(2A3) INIT+
IC23
BCDX-B 52
(3B2) BRYX+
IC23
TRQX-B 49
BIC CØNTRØL
(2D1) WBBC+
IC5
DTØE1-
(3C3) CDCX+
(1D2) DAXX+
(2B4) EB14+
(3C1) DTIX-
IC5
DTØE2-
IC10
DTØE+
(2C3) FRYX-
(2B3) DRYX-
IC32
DCLK+
IC17
DTØX- (3C3) (2A4)
(2A3) INIT-
(2B3) DRYX+
DTØX+
IC32
BTØA- (6A4)
(1D2) DAXX+
(2B4) EB13+
(3D1) DTØX-
IC24
DTIE1-
TAKK+
(3C3) CDCX+
IC24
DTIE2-
IC32
DTIE+
DTIX+
IC32
BTIA- (5B4)
IC17
IC3
DTIXA+ (4B2)
DTIX- (3D3) (2A4)
+5V
R22 1K
WBBC+
(4B3) TXRDY+
IC31
WBFRA-
IC10
BRYX+ (3B4)
(2C1) WBBC-
(4B3) RCRDY+
IC11
RBFRA-
BYTE TRANSFER IN / OUT
(4B3) TXRDY-
IC45
TXRINT+
IC41
P1
89
TXRINT-
IC46
TXC+
C20 270 pf 500V
90
TINRTN
(4B3) RCRDY-
IC45
RCRINT+
IC40
91
RCRINT-
IC46
RCC+
C21 270 pf 500V
94
RTN
(4A3) ØEB+
(4A3) FEB+
IC45
ØE/FE-
IC45
E/BINT+
IC40
93
E/BINT-
IC46
E/BC+
C22 270 pf 500V
INTERRUPT CØNTRØLS
CODE IDENT NO. 21101
SIZE C
DWG NO 91C0352
REV C
SCALE
SHEET 3 OF 6



SENSE RESPØNSE

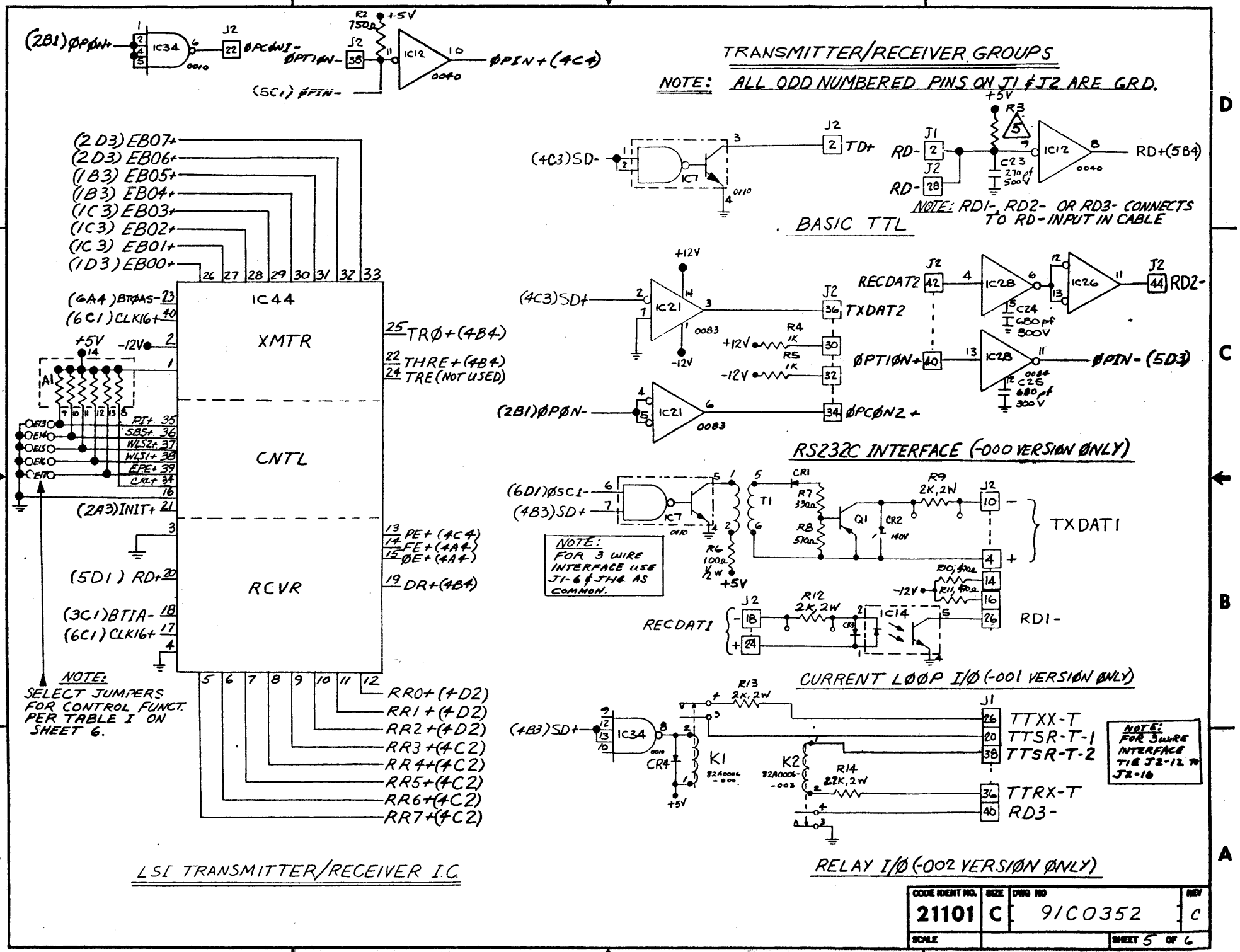


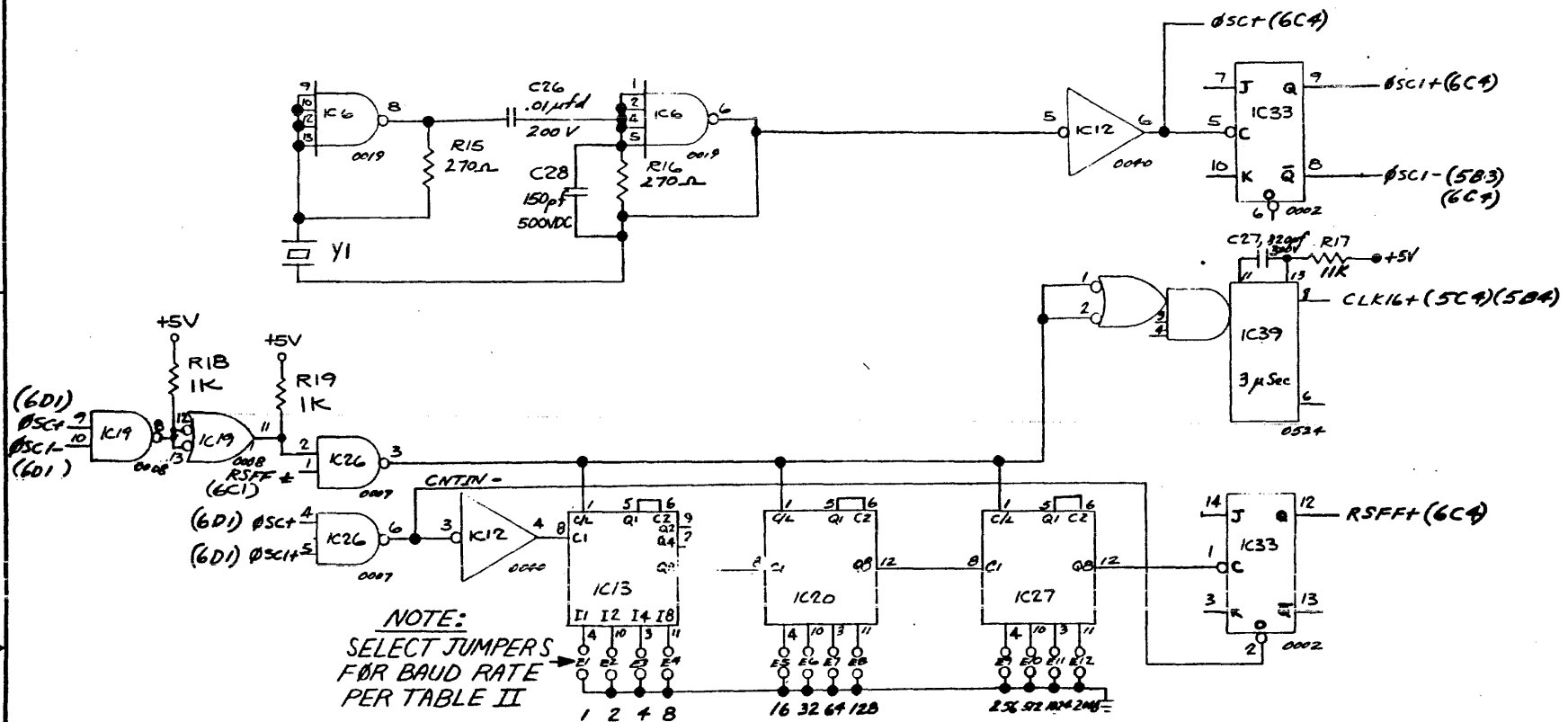
LSI OUTPUT BUFFERS



E-BUSS INPUT DRIVERS

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0352	C
SCALE		SHEET 4 OF 6	


TRANSMITTER/RECEIVER GROUPS
NOTE: ALL ODD NUMBERED PINS ON J1 & J2 ARE G.R.D.
(2B1) ØPPØN+
ØPCØN1-
ØPTIØN-
(5C1) ØPIN-
ØPIN+ (4C4)
(2D3) EB07+
(2D3) EB06+
(1B3) EB05+
(1B3) EB04+
(1C3) EB03+
(1C3) EB02+
(1C3) EB01+
(1D3) EB00+
IC44
XMTR
CNTL
RCVR
(6A4) BTØAS-
(6C1) CLK16+
(2A3) INIT+
(5D1) RD+
(3C1) BTIA-
(6C1) CLK16+
TRØ+ (4B4)
THRE+ (4B4)
TRE (NOT USED)
PE+ (4C4)
FE+ (4A4)
ØE+ (4A4)
DR+ (4B4)
RR0+ (4D2)
RR1+ (4D2)
RR2+ (4C2)
RR3+ (4C2)
RR4+ (4C2)
RR5+ (4C2)
RR6+ (4C2)
RR7+ (4C2)
NOTE: SELECT JUMPERS FOR CONTROL FUNCT. PER TABLE I ON SHEET 6.
LSI TRANSMITTER/RECEIVER I.C.
(4C3) SD-
TD+
RD-
RD+ (5B4)
NOTE: RD1-, RD2- OR RD3- CONNECTS TO RD- INPUT IN CABLE
BASIC TTL
(4C3) SD+
TXDAT2
ØPTIØN+
ØPIN- (5D3)
(2B1) ØPØN-
ØPCØN2+
RECDAT2
RD2-
RS232C INTERFACE (-000 VERSION ØNLY)
(6D1) ØSC1-
(4B3) SD+
NOTE: FOR 3 WIRE INTERFACE USE J1-6 & J1-16 AS COMMON.
TXDAT1
RECDAT1
RD1-
CURRENT LOOP I/Ø (-001 VERSION ØNLY)
(4B3) SD+
TTXX-T
TTSR-T-1
TTSR-T-2
TTRX-T
RD3-
NOTE: FOR 3 WIRE INTERFACE TIE J2-12 TO J2-16
RELAY I/Ø (-002 VERSION ØNLY)
CODE IDENT NO. 21101
SIZE C
DWG NO 91C0352
REV C
SCALE
SHEET 5 OF 6



CLØCK ØSCILLATØR & DIVIDER

TABLE I

JUMPER	IN	ØUT
E13	PARITY	NO PARITY
E14	1 STOP BIT	2 STOP BITS
E17	ODD PARITY	EVEN PARITY
E15, E16	5 DATA BITS	8 DATA BITS
E15	6 DATA BITS	(IF E16 OUT)
E16	7 DATA BITS	(IF E15 OUT)

REFER TO CONTROL FUNCTIONS @ 5C4 FOR INSTALLATION

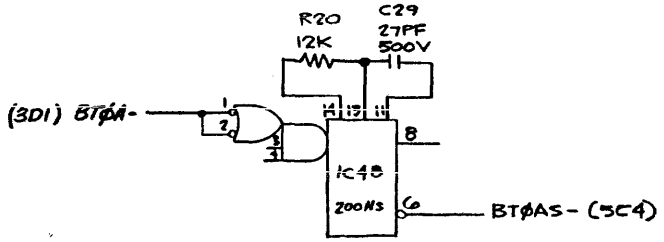


TABLE II

BAUD RATE	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12
9600		X	X	X								
4800	X		X	X	X							
2400	X	X		X	X	X						
2000	X	X	X				X					
1800	X	X	X	X			X					
1200	X	X	X		X	X	X					
600	X	X	X	X		X	X	X				
300	X	X	X	X	X		X	X	X			
150	X	X	X	X	X	X		X	X	X		
110			X	X	X				X		X	
75	X	X	X	X	X	X	X		X	X	X	
45	X	X	X	X	X	X	X				X	X

INSTALL JUMPERS MARKED "X" FOR BAUD RATE DESIRED

21101	C	91C0352	L
SCALE			SHEET 6 OF 6

DWG NO 89A0228

REVISIONS			
SYM	DESCRIPTION	APPROVED	DATE
A	PRODUCTION RELEASE PER EN 80364		1/7/72

J. Spencer
Director
Engineering Operations

T. H. Sweere
Director
Systems Engineering

DR	Sue Johnson	10-1-71
CHK		1-7-72
DSGN		
ENGR		
APPD		12/3/71
APPD		12/3/71

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varian data machines /a varian subsidiary
2722 michelson drive / irvine / california / 92664

TITLE
SOFTWARE PERFORMANCE SPECIFICATION
ASYNCHRONOUS SERIAL CONTROLLER TEST

CODE IDENT NO.	SIZE	DWG NO.	REV
21101	A	89A0228	A
SCALE		SHEET 1 OF 70	

96A0153-0005

TABLE OF CONTENTS

SECTION 1
TEST PROGRAM OVERVIEW

1.1 INTRODUCTION

The purpose of this program is to provide the user with an adaptable routine to test the operational status of the Universal Asynchronous Serial Controller (UASC) and to assist in isolating malfunctions.

1.2 PROGRAM DESIGN OVERVIEW

The UASC test program is designed to operate with the 620 Test Executive which provides all the user interface routines, utility functions and standard subroutines. Consequently, the Test Executive must be loaded prior to operating the UASC (see Software Performance Specification No. 89A0122).

1.2.1 Sense Mode

512 words are generated from the selected pattern, transmitted under sense mode, received under sense mode, and compared. This will cycle continuously until sense switch 3 is set. At which time the program, if in teletype mode, will type the number of passes and return to the pattern message.

1.2.2 BIC Mode

1.2.2.1 BIC Transmit

512 words are generated from the selected pattern, transmitted under BIC mode, received under sense mode, and compared. This will cycle continuously until sense switch 3 is set. At which time the program, if in teletype mode, will type the number of passes and return to the pattern message.

1.2.2.2 BIC Receive

512 words are generated from the selected pattern, transmitted under sense mode, received under BIC mode, and compared. This will cycle continuously until sense switch 3 is set. At which time the program, if in teletype mode, will type the number of passes and return to the pattern message.

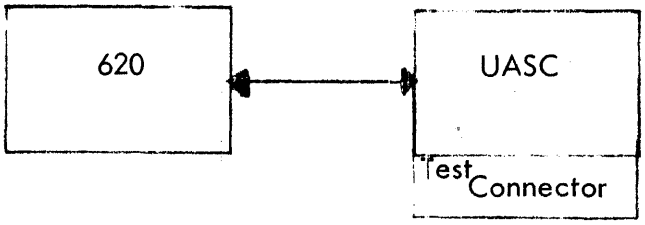
1.2.3 PIM Mode

The program provides for operating under the program interrupt mode in either sense, BIC transmit or BIC receive. The program functions as above.

1.3 HARDWARE SUMMARY

The normal minimum hardware configuration for the UASC test program is one 4K (minimum) 620 series computer, one ASR teletype (optional) and a UASC with test connector. No mainframe options or other peripherals are required.

In the absence of a teletype the program may be supplied in a form suitable for other input media (card reader, paper tape, etc.) and executed in the console mode.



SECTION 2
EXTERNAL SPECIFICATIONS

2.1 GENERAL

The external specification provides all the operating procedures and information pertinent to user interface. The UASC test is normally loaded and executed via teletype keyboard commands from the user. The 620 Test Executive program is the software interface for accomplishing these functions.

2.2 LOADING PROCEDURE

The 620 Test Executive must be loaded before the UASC test program will operate correctly in either mode. All of the teletype input/output subroutines are resident in the Test Executive and will be called by the test program.

a. Load the Test Executive, which includes the binary object tape loader, per the procedure outlined in the Test Executive external specifications, (89A0122).

b. The individual test tapes begin with leader. Position the leader preceeding the test program in the reader.

2.3 OPERATING PROCEDURE

2.3.1 Teletype Mode

The 620 Test Executive must be in the teletype mode.

2.3.1.1 Loading the UASC Test

Type L. The test tape will be loaded, and execution will take place automatically.

2.3.1.2 Parameter Setup

Typeout: Universal Asynchronous Serial Controller Test
Response: (None)

Typeout: UASC DA
Response: A 2 digit octal number for the UASC device address followed by a comma or period. (If sense switch 3 is set, control is returned to the Exec.)

Typeout: DATA LENGTH
Response: A single digit number for data word length. (If SS3 is set, control is returned to the Exec.)

Typeout: PATTERN
Response: A single alphabetic character. A for an alternating pattern, F for a fixed pattern, or I for an incrementing pattern followed by a 3 digit octal number for the initial pattern followed by a comma or period. NOTE: If the following conditions are not to be changed, type C for continue as the first and only character of this response. (If SS3 is set, control is returned to the UASC DA message.)

Typeout: PIM REQUIRED
Response: A single alphabetic character. Y for yes, N for no (if SS3 is set, control is returned to the pattern message).

Typeout: PIM DA
NOTE: If the response to PIM required is N, this message will not appear.
NOTE: Once the PIM device address is input, this message will not appear unles the program is restarted from the beginning.
Response: A 2 digit octal number for the PIM device address followed by a comma or period. (If SS3 is set, control is returned to the pattern message.)

Typeout: TX INT LOC
NOTE: If the response to PIM REQUIRED is N, this message will not appear.
Response: A 1 - 6 digit octal number for the transmit interrupt location.

Typeout: RX INT LOC
NOTE: If the response to PIM required is N, this message will not appear.
Response: A 1 - 6 digit octal number for the receive interrupt location.

Typeout: ER INT LOC
NOTE: If the response to PIM required is N, this message will not appear.
Response: A 1 - 6 digit octal number for the error interrupt location.

Typeout: MASK
NOTE: If the response to PIM required is N, this message will not appear.
Response: A 3 digit octal number for the PIM mask.

Typeout: MODE
Response: Two alphabetic characters. SE for sense mode or BI for BIC mode. (If SS3 is set,control is returned to the pattern message.)

If Sense Mode is selected, no further setup is required.

Typeout: BIC DA
NOTE: Once the BIC device address is input, this message will not appear unles the program is restarted from the beginning.
Response: A 2 digit octal number for the BIC device address followed by a comma or period. (If SS3 is set, control is returned to the pattern message.)

Typeout: BIC DIRECTION
Response: A single alphabetic character.R for sense mode write, BIC mode read, T for BIC mode write, sense mode read. (If SS3 is set, control is returned to the pattern message.)

This completes the UASC setup.

2.3.2 Console Mode

The 620 Test Executive must be in the console mode (see section 2 of 89A0122).

2.3.2.1 Load the UASC Test

(See section 2 of 89A0122.)

2.3. 2.2 Parameter Setup

Start the test at location 0500. Observe the U register for the appropriate halt instruction. At halt instruction 01 set A = UASC device address, and B = Data length (037 for 5 bit, 077 for 6 bit, 0177 for 7 bit, 0377 for 8 bit) press run. At halt instruction 02 set A = pattern type (0 = ALT, 06 = FIX, 011 = INC) and B = pattern configuration. Press run at halt instruction 03 set A = PIM device address (if no PIM is required set A = 0) press run. At halt instruction 04 (if PIM device address $\neq$ 0) set A = transmit interrupt location, B = receive interrupt location, and X = error interrupt location. Press Run. At halt instruction 5 set A = mode (0 = sense, 1 = BIC), B = BIC device address, X = BIC direction (0 = receive, 1 = transmit) press run. The program will run to halt instruction 0704 at which time the A register will be minus for a functioning sense option or the A register will be positive or zero for a non-functioning sense option. Press run to continue test.

2.3.3 Operating in Sense Mode

A quick test of the UASC is made to determine if the data length is correct and to see if the sense option is functioning.

2.3.3.1 Method of Test

The program builds 512 words to be transmitted, outputs them and reads them back. When all 512 words have been read, a compare of transmitted to received data is made. Errors and malfunctions are reported to the operator via teletype messages or halts.

2.3.3.2 Messages and Their Meanings

Message: TRANSMIT NOT READY
Meaning: After initializing the controller the output section was not immediately ready.

Message: RECEIVE SHOULD NOT BE READY
Meaning: After initializing the controller the input section was immediately ready.

Message: LENGTH ERROR
Meaning: The length selected by the operator does not match that of the controller.

Message: NON-FUNCTIONING SENSE OPTION
Meaning: Either the sense option is not installed or the sense option is malfunctioning.

Message: FUNCTIONING SENSE OPTION
Meaning: The sense option is installed and functioning.

Message: CONTROLLER NOT READY
Meaning: A timeout has occurred while awaiting a response from the UASC.

Message: BUFFER SIZE ERROR.
Meaning: The size of either the input or output buffers was not 512 words.

Message: ERROR i WORD j TX k RX l
Meaning: The read error status of the jth word was set (i = error: 1 = input overflow error, 2 = input parity error, 3 = input overflow error and input parity error, 4 = frame error or break, 5 = input overflow, error and frame error or break, 6 = input parity error and frame error or break, 7 = input overflow error and input parity error and frame error or break) k = the transmitted character, l = the

received character.

Message: CMP ERR WORD j TX k RX l m
Meaning: A compare error at word j has occurred between the transmitted character k and the received character l with m being the exclusive ORing of the two characters.

2.3.4 Operating in BIC Mode

2.3.4.1 Operating in BIC Read Mode

A quick test of the UASC is made to determine if the data length is correct and to see if the sense option is functioning.

2.3.4.1.1 Method of Test

The program builds 512 words to be transmitted, outputs them and reads them back. When all 512 words have been read a compare of transmitted to received data is made. Errors and malfunctions are reported to the operator via teletype messages or halts.

2.3.4.1.2 Messages and Their Meanings

Message: TRANSMIT NOT READY
Meaning: After initializing the controller the output section was not immediately ready.

Message: RECEIVE SHOULD NOT BE READY
Meaning: After initializing the controller input section was immediately ready.

Message: LENGTH ERROR
Meaning: The length selected by the operator does not match that of the controller.

Message: NON-FUNCTIONING SENSE OPTION
Meaning: Either the sense option is not installed or the sense option is malfunctioning.

Message: FUNCTIONING SENSE OPTION
Meaning: The sense option is installed and functioning.

Message: CONTROLLER NOT READY
Meaning: A timeout has occurred while awaiting a response from the UASC.

Message: BIC NOT READY
Meaning: A timeout has occurred while awaiting a response from the BIC.

Message: BIC ABNORMAL
Meaning: The BIC has reported an abnormal condition.

Message: BUFFER SIZE ERROR
Meaning: The size of either the input or output buffers was not 512 words.

Message: ERROR i WORD j TX k RX l
Meaning: The read error status of the jth word was set (i = error: 1 = input overflow error, 2 = input parity error, 3 = input overflow error and input parity error, 4 = frame error or break, 5 = input overflow, error and frame error or break, 6 = input parity error and frame error or break, 7 = input overflow error and input parity error and frame error or break) k = the transmitted character, l = the received character.

Message: CMP ERR WORD j TX k RX l m
Meaning: A compare error at word j has occurred between the transmitted character k and the received characters l with m being the exclusive ORing of the two characters.

2.3.4.2 Operating in BIC Write Mode

A quick test of the UASC is made to determine if the data length is correct and to see if the sense option is functioning.

2.3.4.2.1 Method of Test

The program builds 512 words to be transmitted, outputs them and reads them back. When all 512 words have been read a compare of transmitted to received data is made. Errors and malfunctions are reported to the operator via teletype messages or halts.

2.3.4.2.2 Messages and Their Meanings

Message: TRANSMIT NOT READY
Meaning: After initializing the controller the output section was not immediately ready.

Message: RECEIVE SHOULD NOT BE READY
Meaning: After initializing the controller, the input section was immediately ready.

Message: LENGTH ERROR
Meaning: The length selected by the operator does not match that of the controller.

Message: NON-FUNCTIONING SENSE OPTION
Meaning: Either the sense option is not installed or the sense option is malfunctioning.

Message: FUNCTIONING SENSE OPTION
Meaning: The sense option is installed and functioning.

Message: CONTROLLER NOT READY
Meaning: A timeout has occurred while awaiting a response from the UASC.

Message: BIC NOT READY
Meaning: A timeout has occurred while awaiting a response from the BIC.

Message: BIC ABNORMAL
Meaning: The BIC has reported an abnormal condition.

Message: BUFFER SIZE ERROR
Meaning: The size of either the input or output buffers was not 512 words.

Message: ERROR i WORD j TX k RX l
Meaning: The read error status of the jth word was set (i = error: 1 = input overflow error, 2 = input parity error, 3 = input overflow error and input parity error, 4 = frame error or break, 5 = input overflow, error and frame or break, 6 = input parity error and frame error or break, 7 = input overflow error and input parity error and frame error or break) k = the transmitted character, l = the received character.

Message: CMP ERR WORD j TX k RX l m
Meaning: A compare error at word j has occurred between the transmitted character k and the received characters l with m being the exclusive ORing of the two characters.

2.4 SENSE SWITCH SETTINGS

Switch 1 off: Print all error messages.
on: Do not print routine error messages.

Switch 2 off: Do not halt on 9 errors.
on: Halt when errors detected. (This halt will occur after the error message is typed if SS1 is off.)

Switch 3 off: Normal operation.
on: Return as soon as possible to the pattern message or halt instruction 01 (see section 2.3.1.2).

2.5 MESSAGES

Universal Asynchronous Serial Controller Test
UASC DA
DATA LENGTH
PATTERN
PIM REQUIRED
PIM DA
XMIT INT LOC
RCVE INT LOC
ERR INT LOC
MASK
MODE
BIC DA
BIC DIRECTION
TRANSMIT NOT READY
RECEIVE SHOULD NOT BE READY
LENGTH ERROR
NON-FUNCTIONING SENSE OPTION
FUNCTIONING SENSE OPTION
BIC ABNORMAL
BIC NOT READY
BUFFER SIZE ERROR
CONTROLLER NOT READY
ERROR n WORD nnnnnn TX nnnnnn RX nnnnnn
CMP ERR WORD nnnnnn TX nnnnnn RX nnnnnn nnnnnn

2.6 HALTS

Instruction	Register Setting or Meaning
01	Set A = UASC device address B = data length (037 = 5 bit, 077 = 6 bit, 0177 = 7 bit, 0377 = 8 bit)
02	Set A = pattern type (1 = alternating, 6 = fixed, 011 = incrementing) B = initial pattern configuration
03	Set A = PIM device address (if no PIM required, set A = 0)
04	This is an optional halt Set A = transmit interrupt location B = receive interrupt location X = error interrupt location
05	Set A = mode (0 = sense, 1 = BIC) B = BIC device address X = BIC direction (0 = receive, 1 = transmit)
040	"Controller not ready"
041	"Buffer size error"
042	"BIC not ready"
043	"BIC abnormal"
0102	"Hardware detected error" Read A = word within the buffer B = data word transmitted X = data word received with the flags in the most significant part of the word.
0103	"Compare error" Read A = word within the buffer B = data word transmitted C = data word received

Instruction	Register Setting or Meaning
0700	Output not ready
0701	Input should not be ready
0702	Length error
0704	A < 0 Functioning sense option A > 0 Non-functioning sense option

SECTION 3
INTERNAL SPECIFICATION

3.1 COMPONENT SPECIFICATIONS

Title:	Sense Switch 3 Return
Symbolic Name:	SS3R
Purpose:	Termination of Test
Description:	If in teletype mode, type out the octal number of passes mode through the previous test. If in console mode, returns to initial parameter setup.
Entry Points:	SS3R
Calling Sequence:	JSS3 SS3R
Entrance Parameters:	None
Exit Point:	CMOD or TM5
Exit Parameters:	Not applicable

Table or Files Modified or Read: Pass is set to zero.

Tables or Files Created:	Not applicable
Called By:	OUTC, OUTE, OUTD
Called From:	SENM, BICW, BICR, QKY, SCK
Exception Conditions:	Not applicable
Timing:	Not applicable
Size:	26 octal words

Title:	Console Mode Parameter Input
Symbolic Name:	CMOD
Purpose:	Set up parameter values from the console.
Description:	The routine clears all registers and halts at various points to allow for operator inputs.
Entry Points:	CMOD, CMO, CM2, CM3
Calling Sequence:	LDA $CON JAZ CMOD
Entrance Parameters:	Not applicable
Exit Point:	SENM, BICR, BICW
Exit Parameters:	Operating parameters

Tables or Files Modified or Read: DA, DLGH, PATT, PTRN, PDA, PIMR, BDA, MASK

Tables or Files Created:	Not applicable
Called By:	TDA, TPDA, SETI, TBDA
Called From:	Start and end of test.
Exception Conditions:	Not applicable
Timing:	Not applicable
Size:	65 octal words

Title:	Teletype Mode Parameter Input
Symbolic Name:	TMOD
Purpose:	Set up parameter values from the teletype.
Description:	The routine asks for and accepts parameter values from the operator.
Entry Points:	TMOD, TDA, TM5, TPDA, TBDA
Calling Sequence:	JMP TMOD
Entrance Parameters:	Not applicable
Exit Point:	SENM, BICR, BICW
Exit Parameters:	Operating parameters

Tables or Files Modified or Read: DA, DLGH, PATT, PTRN, PDA, PIMR, BDA, MASK

Tables or Files Created:	Not applicable
Called By:	INPB, INPE, INPG, OCT1, OUTD, SETI
Called From:	SS3R, Start and end of test.
Exception Conditions:	Not applicable
Timing:	Not applicable
Size:	642 octal words

Title:	Sense In, Sense Out Mode
Symbolic Name:	SENM
Purpose:	Test the UASC in sense mode with or without PIM.
Description:	Outputs 512 words of data, inputs 512 words of data, and monitors and flags hardware errors.
Entry Points:	SENM
Calling Sequence:	JMP SENM
Entrance Parameters:	Operating parameters.
Exit Point:	SCK, SS3R
Exit Parameters:	Not applicable
Tables or Files Modified or Read:	JUMP, U1, U2, PIM BI
Tables or Files Created:	Not applicable
Called By:	QKY, FOB, IPIM, TOUT, CUR, BSE
Called From:	CMOD, TMOD
Exception Conditions:	Not applicable
Timing:	Approximately 514 decimal UASC word times.
Size:	151 octal words

Title:	Sense In, BIC Out
Symbolic Name:	BICW
Purpose:	Test the UASC using sense in mode and BIC out mode with or without PIM.
Description:	Outputs 512 words of data, inputs 512 words of data, and monitors and flags hardware errors.
Entry Points:	BICW
Calling Sequence:	JMP BICW
Entrance Parameters:	Operating parameters
Exit Point:	SCK, SS3R
Exit Parameters:	Not applicable
Tables or Files Modified or Read:	JUMP, U1, PIM, BI
Tables or Files Created:	Not applicable
Called By:	QKY, FOB, IPIM, TOUT, BNR, CNR, BAB, BSE
Called From:	CMOD, TMOD
Exception Conditions:	Not applicable
Timing:	Approximately 514 decimal UASC word times.
Size:	175 octal words

Title:	BIC In, Sense Out
Symbolic Name:	BICR
Purpose:	Test the UASC using BIC in mode and sense out mode with or without PIM.
Description:	Outputs 512 words of data, inputs 512 words of data, and monitors and flags hardware errors.
Entry Points:	BICR
Calling Sequence:	JMP BICR
Entrance Parameters:	Operating parameters
Exit Point:	SCK, SS3R
Exit Parameters:	Not applicable
Tables or Files Modified or Read:	JUMP, U2, PIM, BI
Tables or Files Created:	Not applicable
Called By:	QKY, FOB, IPIM, TOUT, BNR, CNR, BAB, BSE, BERR
Called From:	
Exception Conditions:	Not applicable
Timing:	Approximately 514 decimal UASC word times.
Size:	174 octal words

Title:	Data check
Symbolic Name:	SCK
Purpose:	To check the input buffer for error flags and to compare output to input data.
Description:	Not applicable
Entry Points:	SCK
Calling Sequence:	JMP SCK
Entrance Parameters:	Not applicable
Exit Point:	Return to the contents of JUMP.
Exit Parameters:	Not applicable
Tables or Files Modified or Read:	BI, BO
Tables or Files Created:	Not applicable
Called By:	OUTD, OUTA, OUTE
Called From:	SENM, BICW, BICR
Exception Conditions:	Routine halts on errors if SS2 set or in console mode.
Timing:	Not applicable
Size:	240 octal words

Title:	BIC abnormal typeout
Symbolic Name:	BAB
Purpose:	Type the message "BIC ABNORMAL".
Description:	Not applicable
Entry Points:	BAB
Calling Sequence:	JMPM BAB
Entrance Parameters:	Not applicable
Exit Point:	Return to caller.
Exit Parameters:	Not applicable
Tables or Files Modified or Read:	Not applicable
Tables or Files Created:	Not applicable
Called By:	OUTD
Called From:	BICU, BICR
Exception Conditions:	No type out if SS1 on. Halt instruction 043 if SS1 on or in console mode.
Timing:	Not applicable
Size:	31 octal words

Title:	BIC read error
Symbolic Name:	BERR
Purpose:	Place flags in the input buffer.
Description:	The flag in the B register is ORed into the current BIC address less 1.
Entry Points:	BERR
Calling Sequence:	LDBI FLAG JMPM BERR
Entrance Parameters:	Not applicable
Exit Points:	Return to caller
Exit Parameters:	Not applicable
Tables or Files Modified or Read:	BI
Tables or Files Created:	Not applicable
Called By:	Not applicable
Called From:	BICR
Exception Conditions:	Not applicable
Timing:	Not applicable
Size:	12 octal words

Title:	BIC not ready type out
Symbolic Name:	BNR
Purpose:	Type the message "BIC NOT READY"
Description:	Not applicable
Entry Points:	BNR
Calling Sequence:	JMPM BNR
Entrance Parameters:	Not applicable
Exit Point:	Return to caller
Exit Parameters:	Not applicable
Tables or Files Modified or Read:	Not applicable
Tables or Files Created:	Not applicable
Called By:	OUTD
Called From:	BICW, BICR
Exception Conditions:	No typeout if SS1 on, halt instruction 042 if SS2 on or in console mode.
Timing:	Not applicable
Size:	33 octal words

Title:	Buffer size error type out
Symbolic Name:	BSE
Purpose:	Type the message "BUFFER SIZE ERROR"
Description:	Not applicable
Entry Points:	BSE
Calling Sequence:	JMPM BSE
Entrance Parameters:	Not applicable
Exit Point:	Return to caller
Exit Parameters:	Not applicable
Tables or Files Modified or Read:	Not applicable
Tables or Files Created:	Not applicable
Called By:	OUTD
Called From:	SENM, BICW, BICR
Exception Conditions:	No type out if SS1 on, halt instruction 041 if SS2 on if in console mode.
Timing:	Not applicable
Size:	34 octal words

Title:	Controller not ready type out
Symbolic Name:	CNR
Purpose:	Type the message "CONTROLLER NOT READY"
Description:	Not applicable
Entry Points:	CNR
Calling Sequence:	JMPM CNR
Entrance Parameters:	Not applicable
Exit Point:	Return to caller
Exit Parameters:	Not applicable
Tables or Files Modified or Read:	Not applicable
Tables or Files Created:	Not applicable
Called By:	OUTD
Called From:	SENM, BICW, BICR, QKY
Exception Conditions:	No type out if SS1 on, halt instruction 040 if SS2 on or in console mode.
Timing:	Not applicable
Size:	42 octal words

Title:	Set in device address
Symbolic Name:	DVAD
Purpose:	To place the device address into referenced I/O instructions.
Description:	The routine picks up the referenced I/O instruction, masks out the device address, replaces it with the referenced device address, and restores the instruction.
Entry Points:	DVAD
Calling Sequence:	JMPM DVAD DATA DEVICEADDRESSLOCATION DATA I/OINSTRUCTION, I/O INSTRUCTION DATA 0
Entrance Parameters:	Not applicable
Exit Point:	Return to caller following the DATA 0.
Exit Parameters:	Not applicable
Tables or Files Modified or Read:	Referenced I/O instructions
Tables or Files Created:	Not applicable
Called By:	Not applicable
Called From:	TMOD
Exception Conditions:	Not applicable
Timing:	Not applicable
Size:	24 octal words

Title:	Fill output buffer
Symbolic Name:	FOB
Purpose:	Fill the output buffer with the requested data pattern.
Description:	Not applicable
Entry Points:	FOB
Calling Sequence:	JMPM FOB
Entrance Parameters:	Not applicable
Exit Point:	Return to caller
Exit Parameters:	Not applicable
Tables or Files Modified or Read:	BO
Tables or Files Created:	Not applicable
Called By:	Not applicable
Called From:	SENM, BICW, BICR
Exception Conditions:	Not applicable
Timing:	Not applicable
Size:	21 octal words

Title:	Get next character to transmit
Symbolic Name:	GNCX
Purpose:	Return a 16 bit data word, and update for the next call according to the pattern type.
Description:	Not applicable
Entry Points:	GNCX
Calling Sequence:	JMPM GNCX
Entrance Parameters:	Not applicable
Exit Point:	Return to caller
Exit Parameters:	Data word in B
Tables or Files Modified or Read:	PTRN
Tables or Files Created:	Not applicable
Called By:	Not applicable
Called From:	FOB
Exception Conditions:	Not applicable
Timing:	Not applicable
Size:	22 octal words

Title:	Initialize PIM
Symbolic Name:	IPIM
Purpose:	Initialize the PIM if required.
Description:	Not applicable
Entry Points:	IPIM
Calling Sequence:	JMPM IPIM
Entrance Parameters:	Not applicable
Exit Point:	Return to caller
Exit Parameters:	Not applicable
Tables or Files Modified or Read:	PIM
Tables or Files Created:	Not applicable
Called By:	Not applicable
Called From:	SENM, BICW, BICR
Exception Conditions:	Not applicable
Timing:	Not applicable
Size:	15 octal words

Title:	Accept an octal input from teletype
Symbolic Name:	OCTI
Purpose:	Type the parameter message and accept an octal number.
Description:	Not applicable
Entry Points:	OCTI
Calling Sequence:	LDXI MESSAGE JMPM OCTI STA NUMBER
Entrance Parameters:	X = MESSAGE ADDRESS
Exit Point:	Return to caller to RM5
Exit Parameters:	A = NUMBER

Tables or Files Modified or Read: Not applicable

Tables or Files Created:	Not applicable
Called By:	OUTD, INPG
Called From:	TMOD
Exception Conditions:	SS3 will cause return to TM5
Timing:	Not applicable
Size:	16 octal words

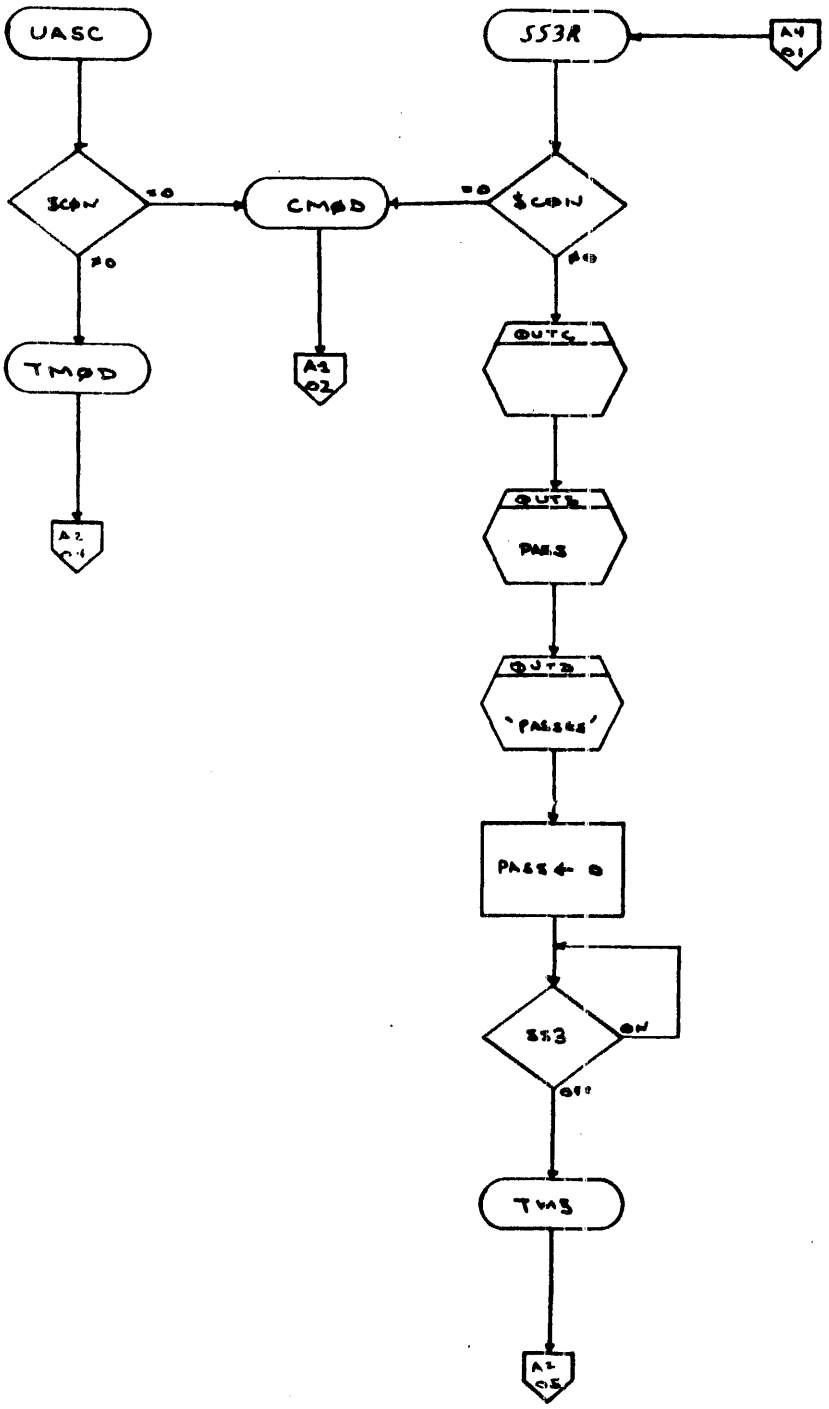
Title:	PIM interrupt
Symbolic Name:	PIMI
Purpose:	Process a PIM interrupt
Description:	Decrement PIM for each interrupt
Entry Points:	PIMI
Calling Sequence:	Interrupt driven routine JMPM PIMI
Entrance Parameters:	Not applicable
Exit Point:	Returns to interrupted routine.
Exit Parameters:	Not applicable
Tables or Files Modified or Read:	Not applicable
Tables or Files Created:	Not applicable
Called By:	Not applicable
Called From:	Not applicable
Exception Conditions:	Not applicable
Timing:	Not applicable
Size:	12 octal words

Title:	Quick test of the UASC
Symbolic Name:	QKY
Purpose:	Provides a quick test of operation, data length and sense option.
Description:	Not applicable
Entry Points:	QKY
Calling Sequence:	JMPM QKY
Entrance Parameters:	Not applicable
Exit Point:	Return to caller
Exit Parameters:	Not applicable
Tables or Files Modified or Read:	Not applicable
Tables or Files Created:	Not applicable
Called By:	TYPE, TOUT, CNR, OUTC, OUTD
Called From:	SENM, BICW, BICR
Exception Conditions:	If an error occurs, the routine will halt. If in console mode, routine will halt after testing the sense option.
Timing:	Not applicable
Size:	63 octal words

Title:	Set PIM interrupt words
Symbolic Name:	SETI
Purpose:	To place a 'JMPM PIMI' in the PIM interrupt locations.
Description:	Not applicable
Entry Points:	SETI
Calling Sequence:	LDA INTERRUPTLOCATION JMPM SETI
Entrance Parameters:	A = INTERRUPT LOCATION
Exit Point:	Return to caller
Exit Parameters:	Not applicable
Tables or Files Modified or Read:	PIM INTERRUPT LOCATIONS
Tables or Files Created:	Not applicable
Called By:	Not applicable
Called From:	TMOD, CMOD
Exception Conditions:	Not applicable
Timing:	Not applicable
Size:	11 octal words

Title:	Type the messages in X
Symbolic Name:	TYPE
Purpose:	Type the message pointed to by the X register.
Description:	Not applicable
Entry Points:	TYPE
Calling Sequence:	LDXI MESSAGE JMPM TYPE
Entrance Parameters:	X = MESSAGE ADDRESS
Exit Point:	Return to caller
Exit Parameters:	Not applicable
Tables or Files Modified or Read:	Not applicable
Tables or Files Created:	Not applicable
Called By:	OUTD
Called From:	QKY
Exception Conditions:	If $CON is zero (console mode), there is no type out.
Timing:	Not applicable
Size:	10 octal words

PROGRAMMER	PROGRAM NO.	DATE	PAGE 01
CHART I.D.	CHART NAME	PROGRAM NAME	

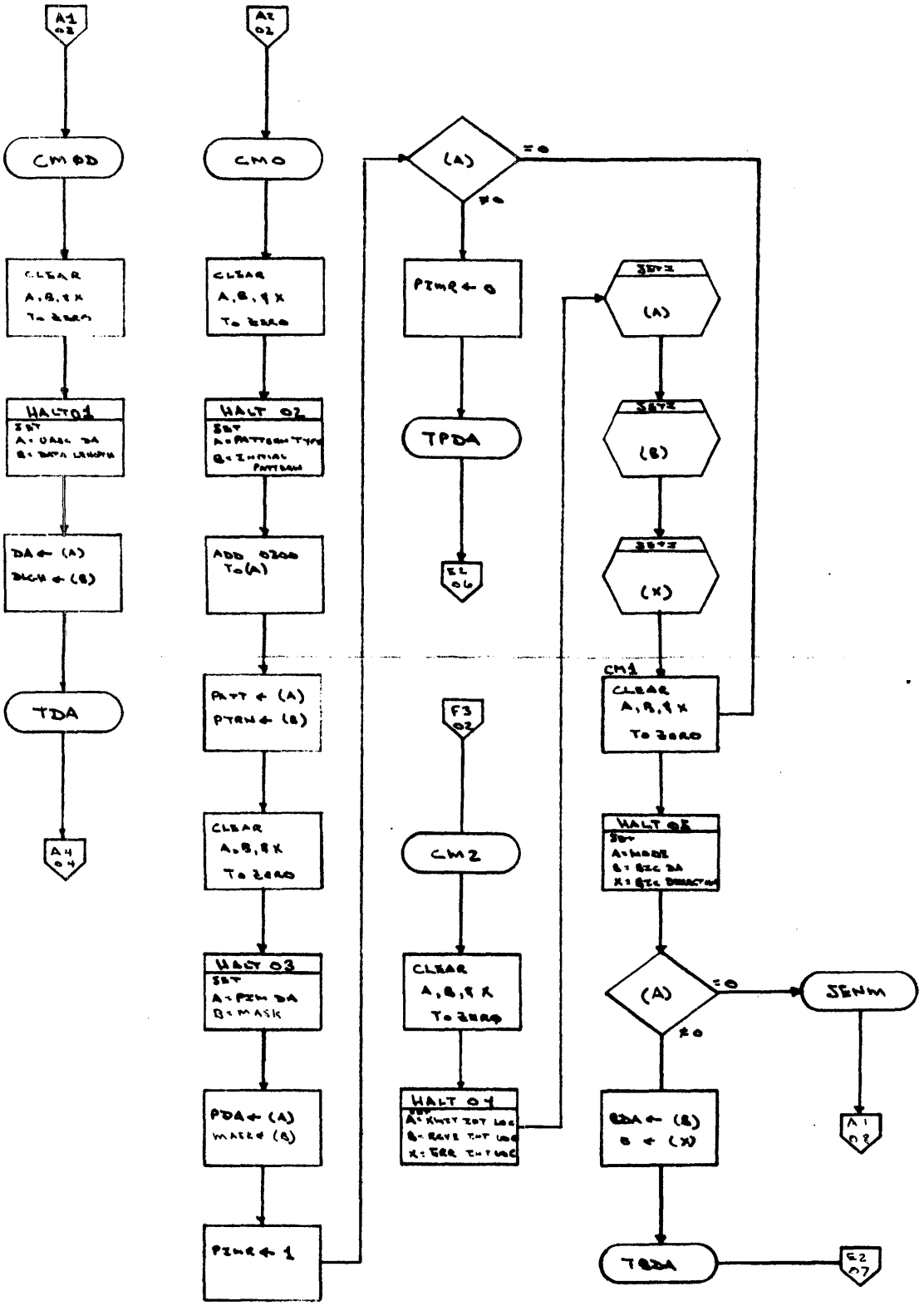


FOLD UNDER AT DOTTED LINE

FOLD UNDER AT DOTTED LINE

varian data machines a varian subsidiary	CODE IDENT. NO.		89A0228	REV. A
	PREPARED BY	APPROVED BY	SHEET 36 OF 70	

90A0048-000A



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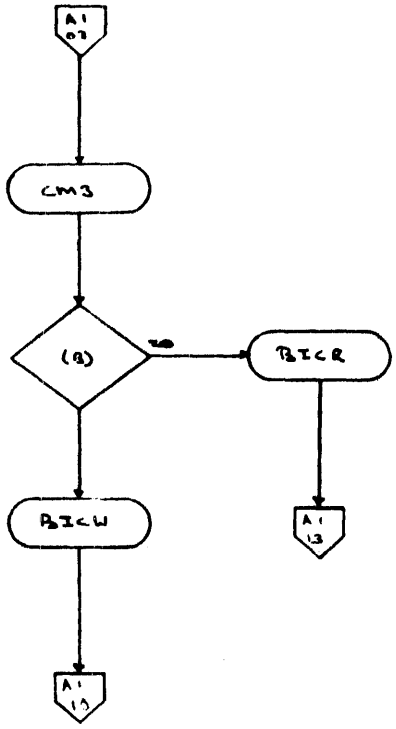
PROGRAMMER	PROGRAM NO.	DATE	PAGE C3
CHART I.D.	CHART NAME	PROGRAM NAME	



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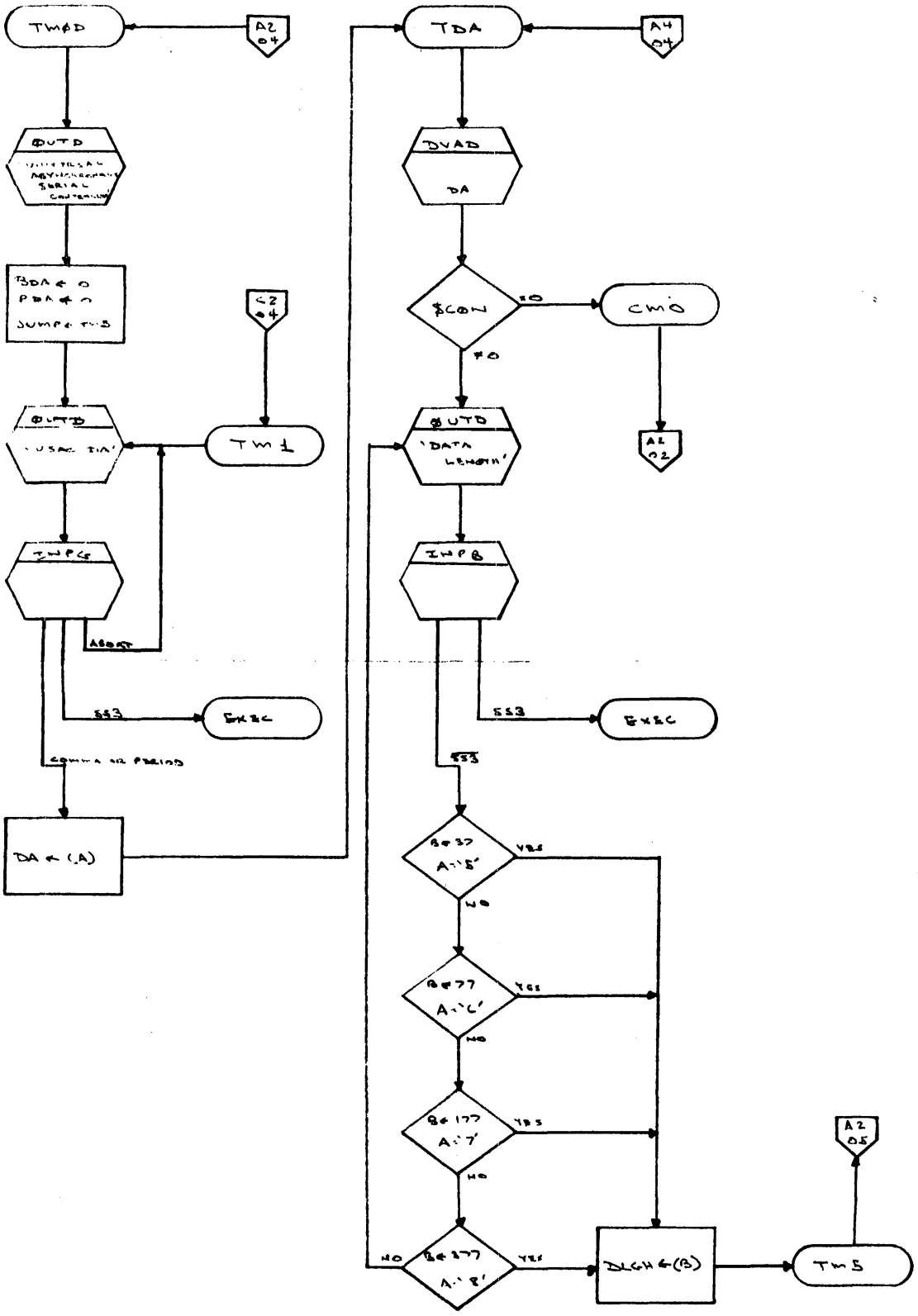
verian data machines a verian subsidiary	CODE IDENT. NO.	89A0228	REV. A
	PREPARED BY	APPROVED BY	SHEET 38 OF 70

90A0540-000A



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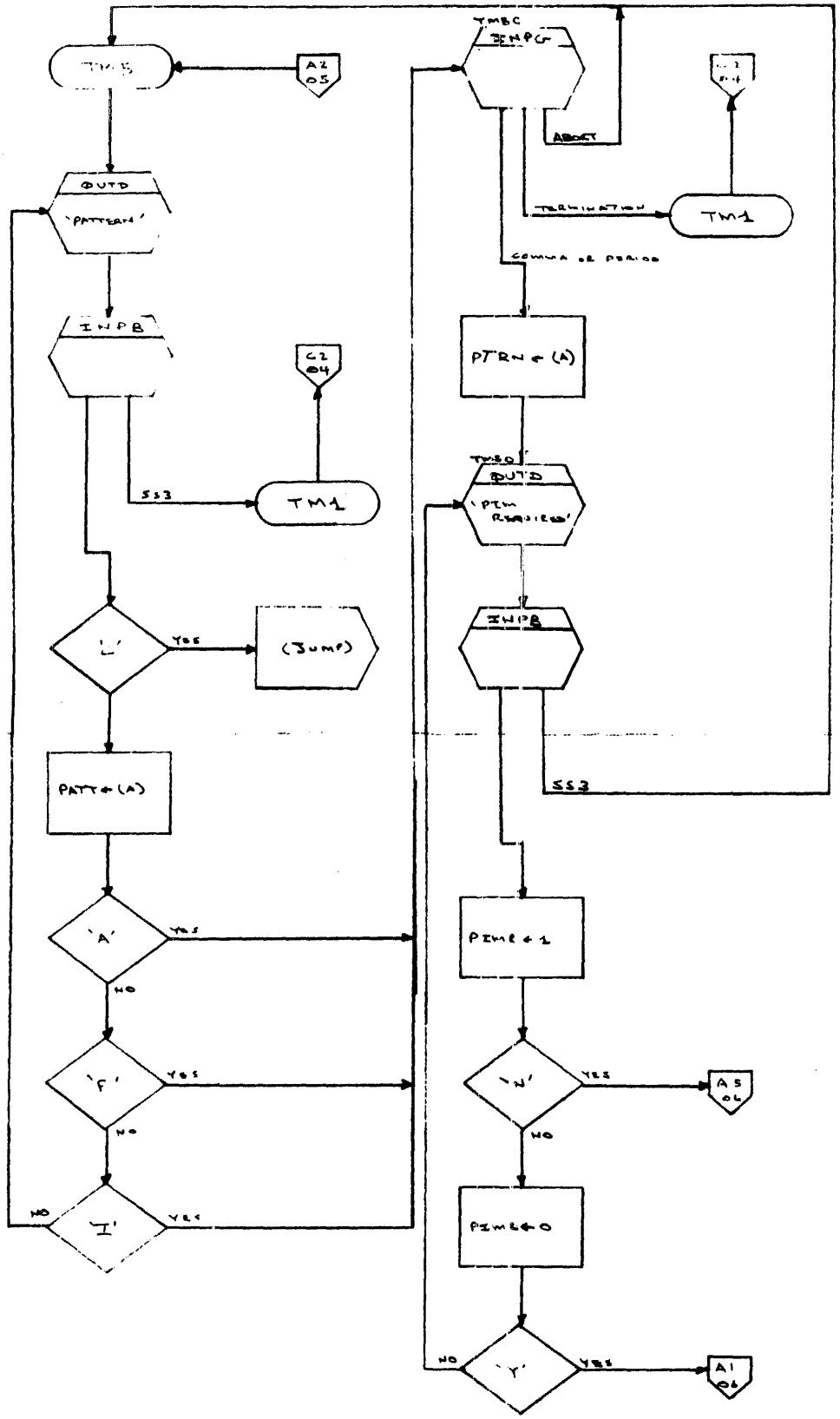
varian data machines a varian subsidiary	CODE IDENT. NO.		89A0228	REV. A
	PREPARED BY	APPROVED BY	SHEET 39 OF 70	

90A0240-000A

PROGRAMMER	PROGRAM NO.	DATE	PAGE 05
CHART I.D.	CHART NAME	PROGRAM NAME	

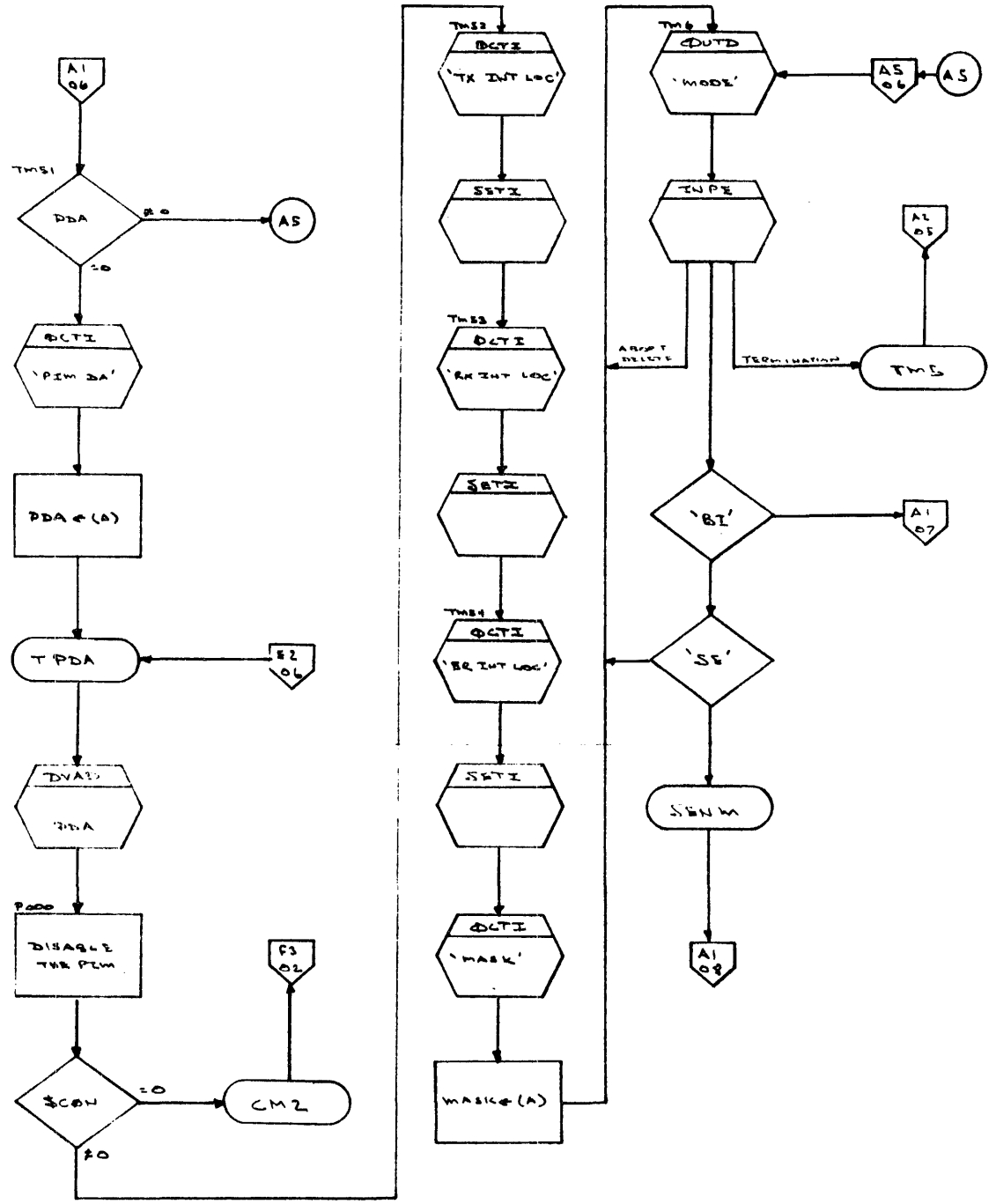


FOLD UNDER AT DOTTED LINE

FOLD UNDER AT DOTTED LINE

varian data machines a varian subsidiary	CODE IDENT. NO.	89A0228	REV. A
	PREPARED BY	APPROVED BY	SHEET 40 OF 70

PROGRAMMER	PROGRAM NO.	DATE	PAGE 06
CHART I.D.	CHART NAME	PROGRAM NAME	



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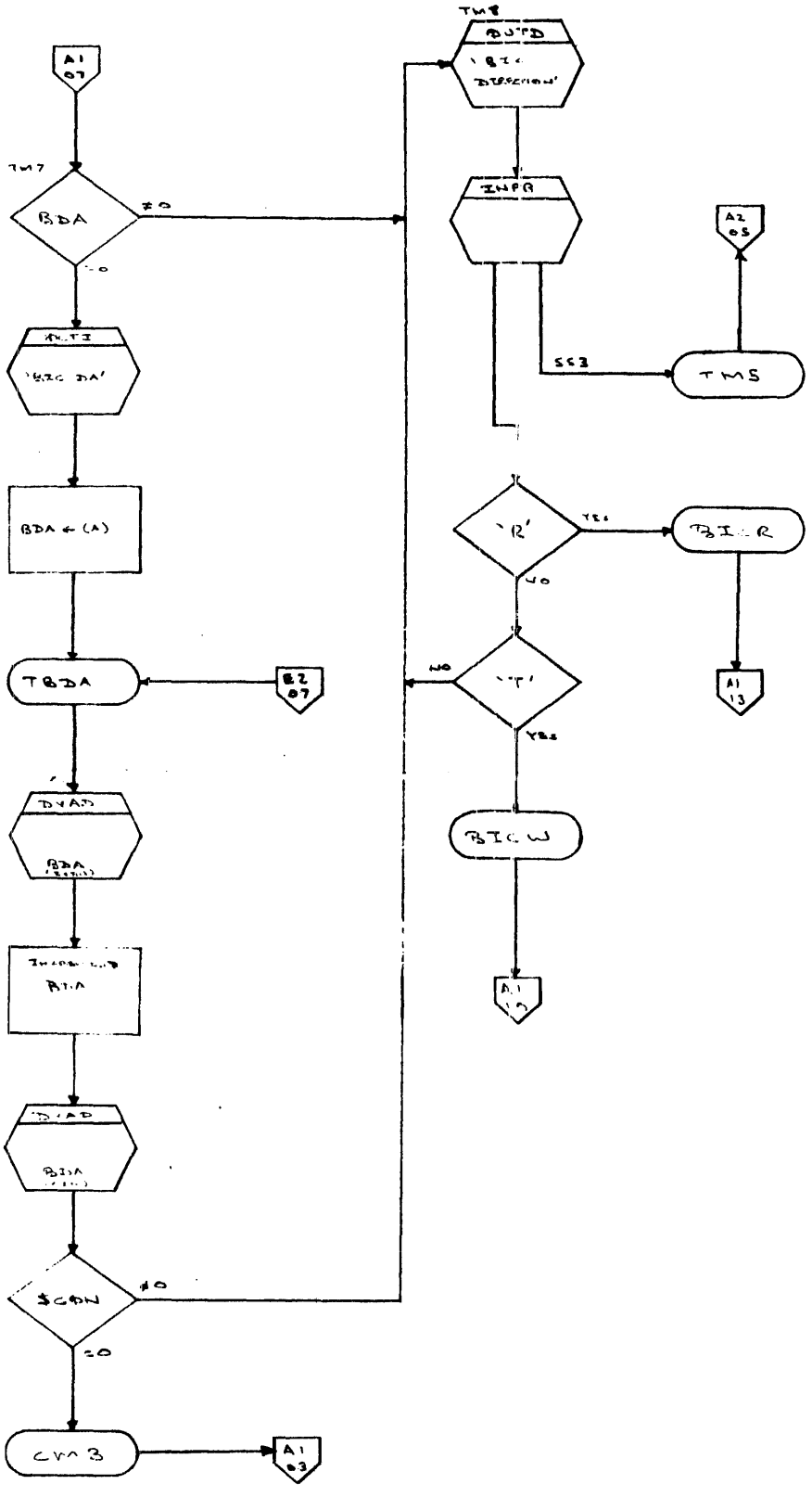
varian data machines a varian subsidiary	CODE IDENT. NO.		89A0228	REV. A
	PREPARED BY	APPROVED BY	SHEET 41 OF 70	



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PROGRAMMER	PROGRAM NO.	DATE	PAGE 09
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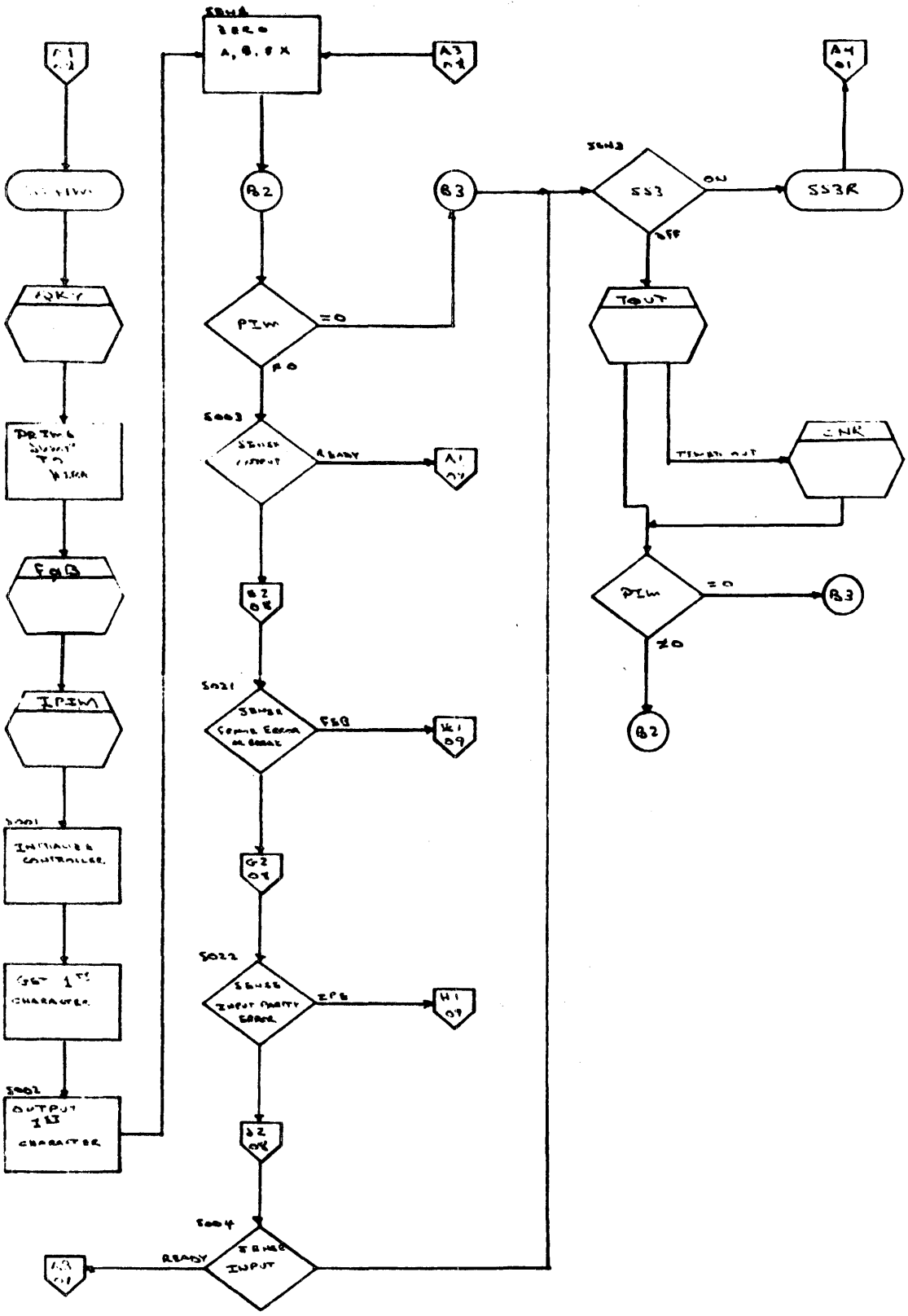

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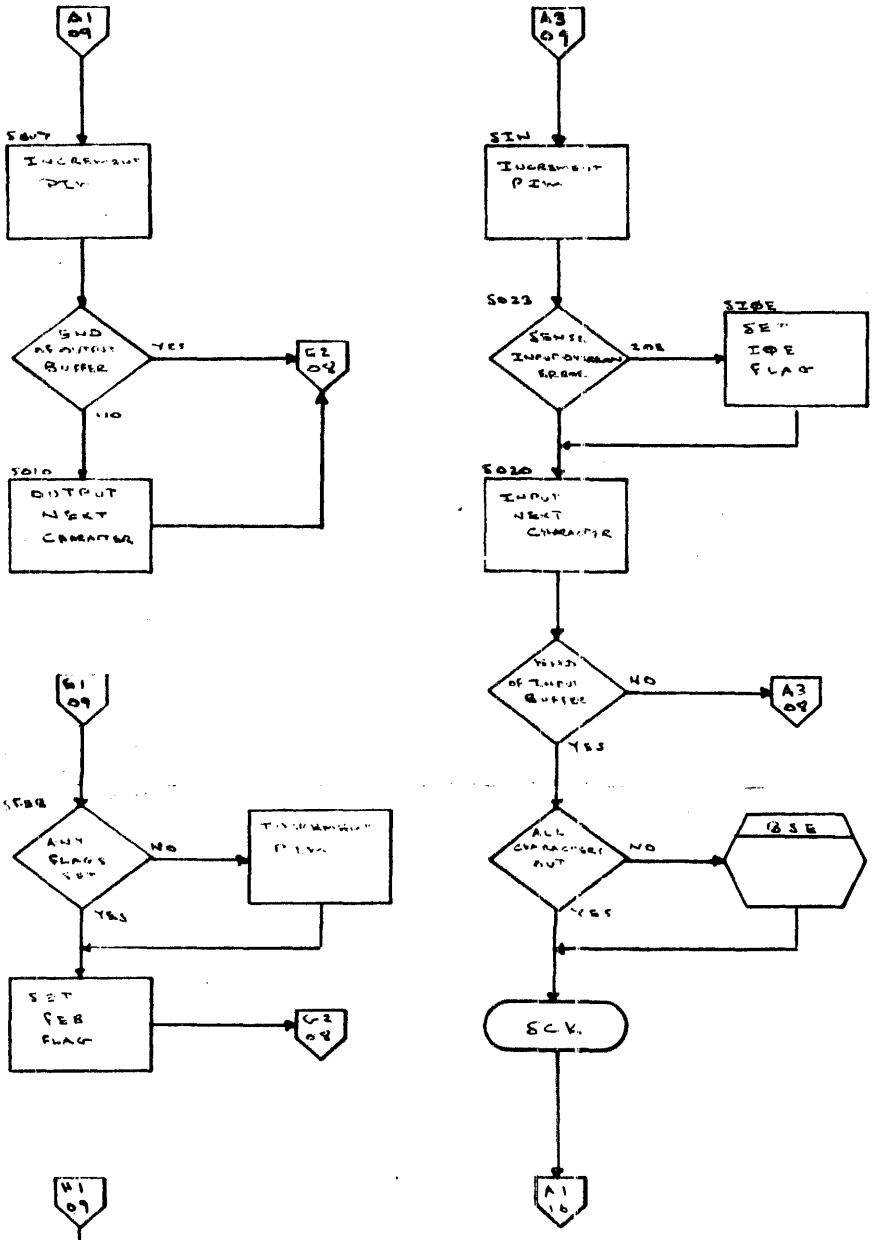
	PREPARED BY	APPROVED BY	SHEET 43 OF 70

PROGRAMMER	PROGRAM NO.	DATE	PAGE 04
CHART I.D.	CHART NAME	PROGRAM NAME	



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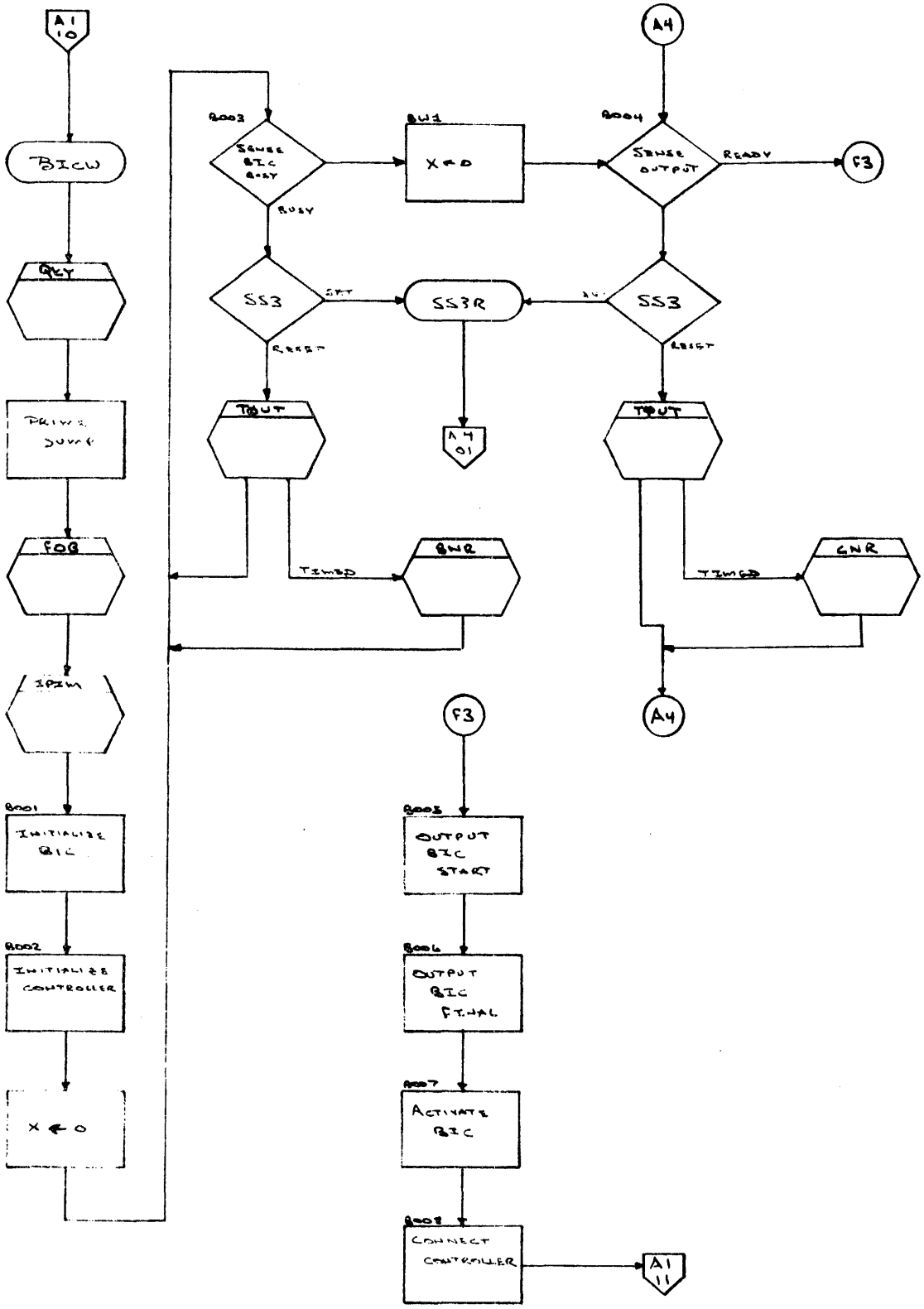
varian data machines a varian subsidiary	CODE IDENT. NO.	89A0228	REV. A
	PREPARED BY	APPROVED BY	SHEET 44 OF 70

PROGRAMMER	PROGRAM NO.	DATE	PAGE 10
CHART I.D.	CHART NAME	PROGRAM NAME	



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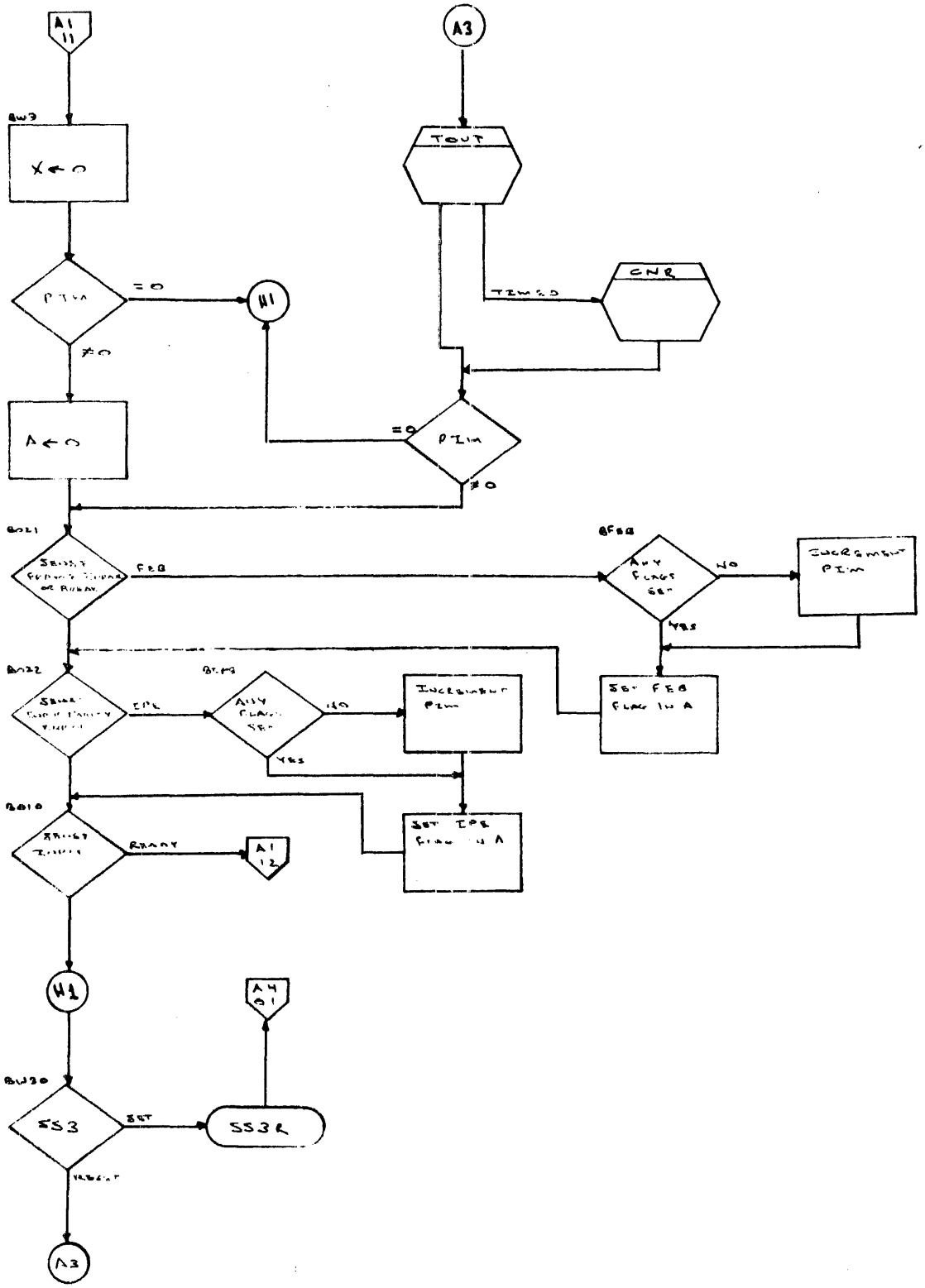
	PREPARED BY	APPROVED BY	SHEET 45 OF 70

90A0349-000A

PROGRAMMER	PROGRAM NO.	DATE	PAGE 11
CHART I.D.	CHART NAME	PROGRAM NAME	



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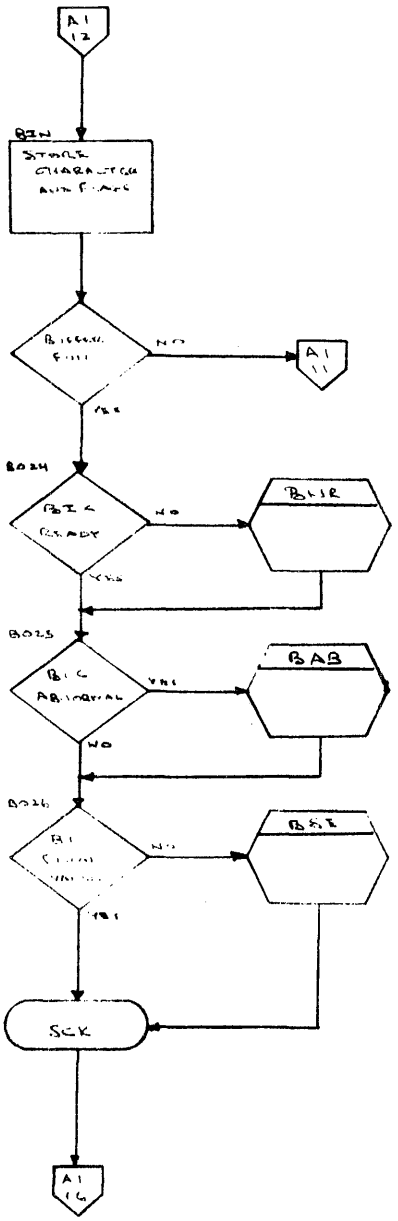
	PREPARED BY	APPROVED BY	SHEET 46 OF 70	

PROGRAMMER	PROGRAM NO.	DATE	PAGE 12
CHART I.D.	CHART NAME	PROGRAM NAME	



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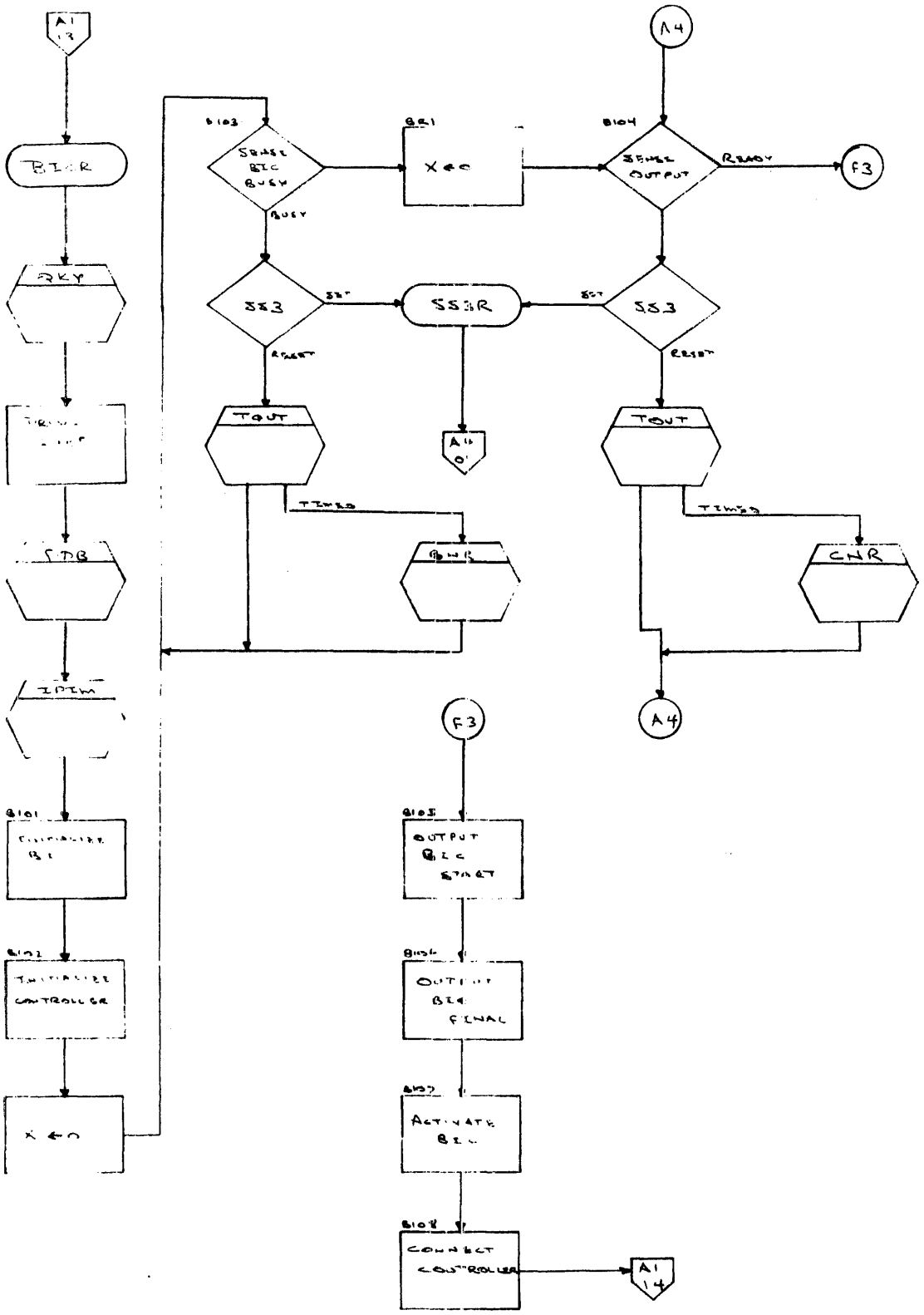
	PREPARED BY	APPROVED BY	SHEET 47 OF 70

98A0349-000A

PROGRAMMER	PROGRAM NO.	DATE	PAGE 1-.
CHART I.D.	CHART NAME	PROGRAM NAME	



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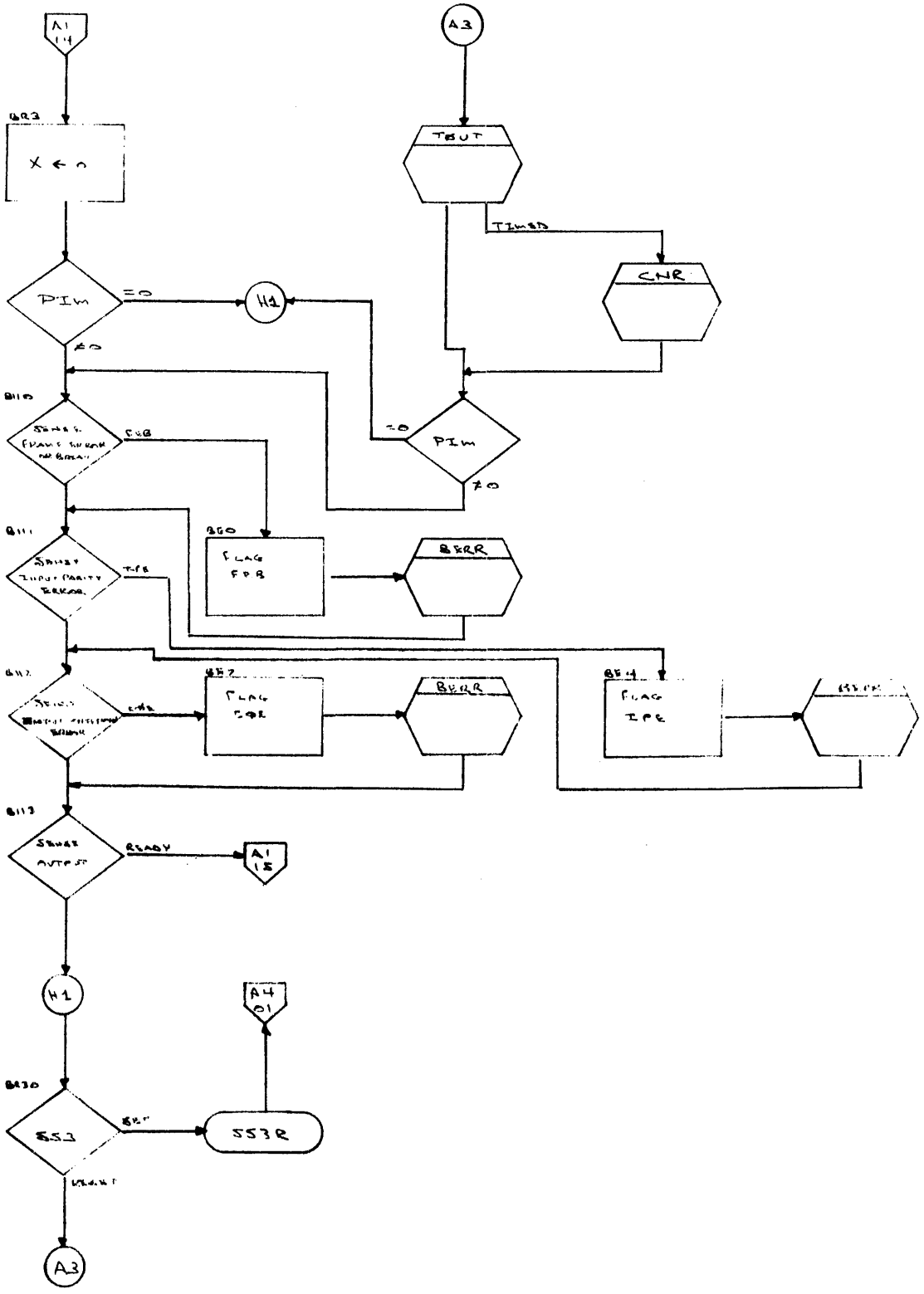
	CODE IDENT. NO.	89A0228	REV. A
varian data machines a varian subsidiary	PREPARED BY	APPROVED BY	SHEET 48 OF 70



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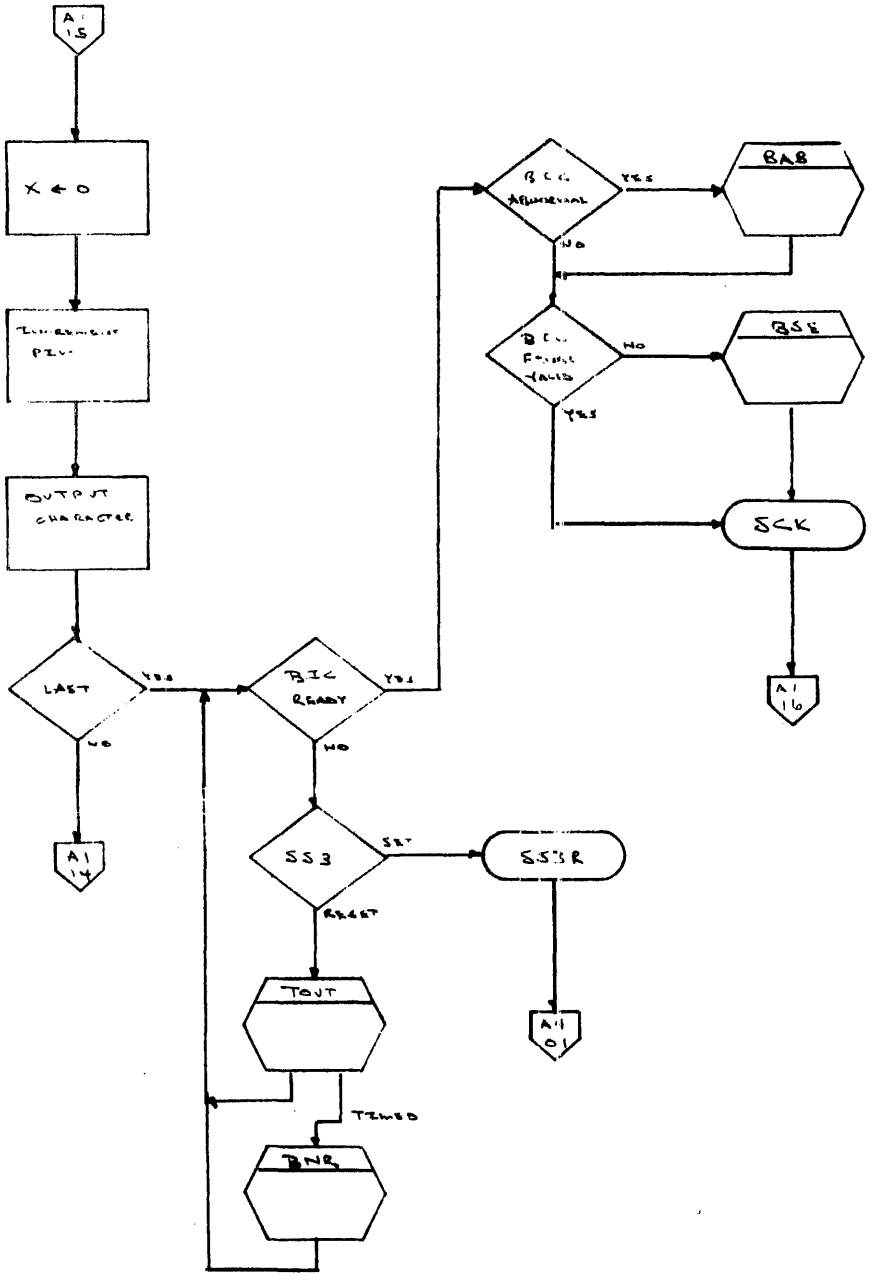
PROGRAMMER	PROGRAM NO.	DATE	PAGE 15
CHART I.D.	CHART NAME	PROGRAM NAME	



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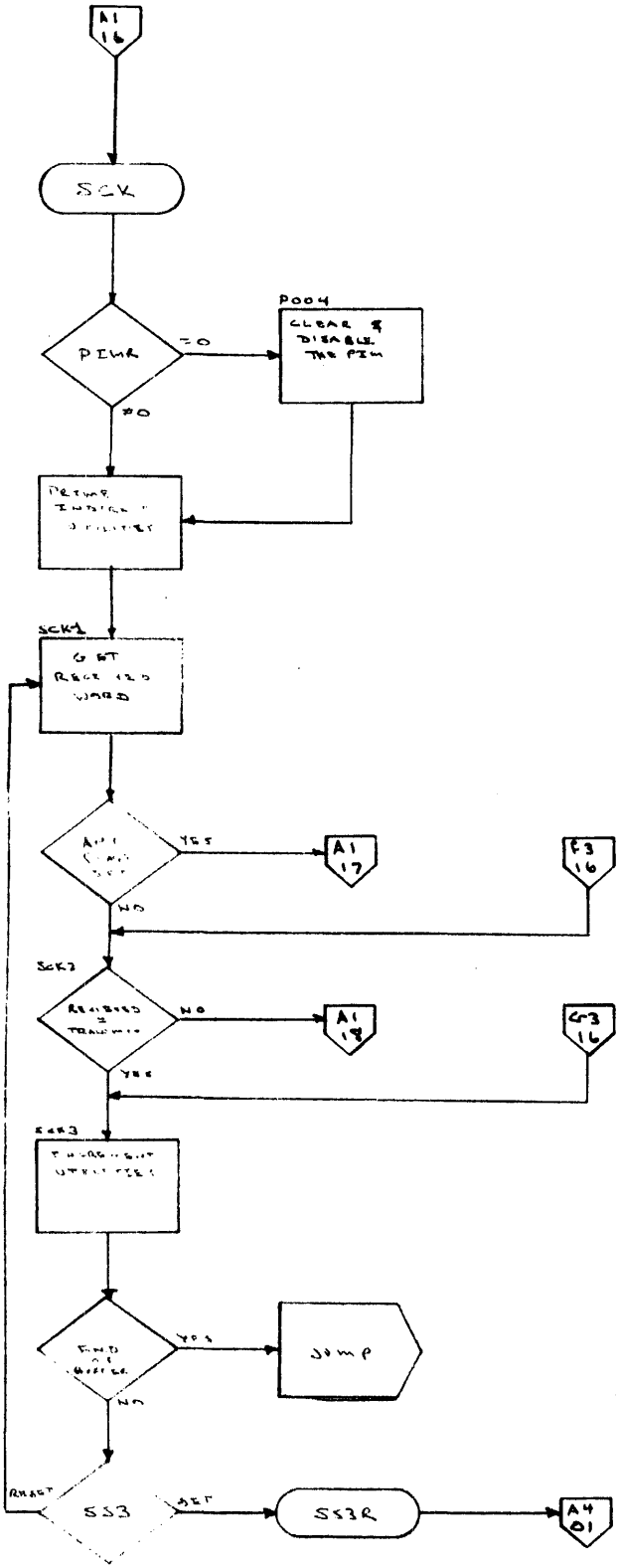
varian data machines a varian subsidiary	CODE IDENT. NO.	89A0228	REV. A
	PREPARED BY	APPROVED BY	SHEET 50 OF 70

89A0240-000A

PROGRAMMER	PROGRAM NO.	DATE	PAGE 16
CHART I.D.	CHART NAME	PROGRAM NAME	



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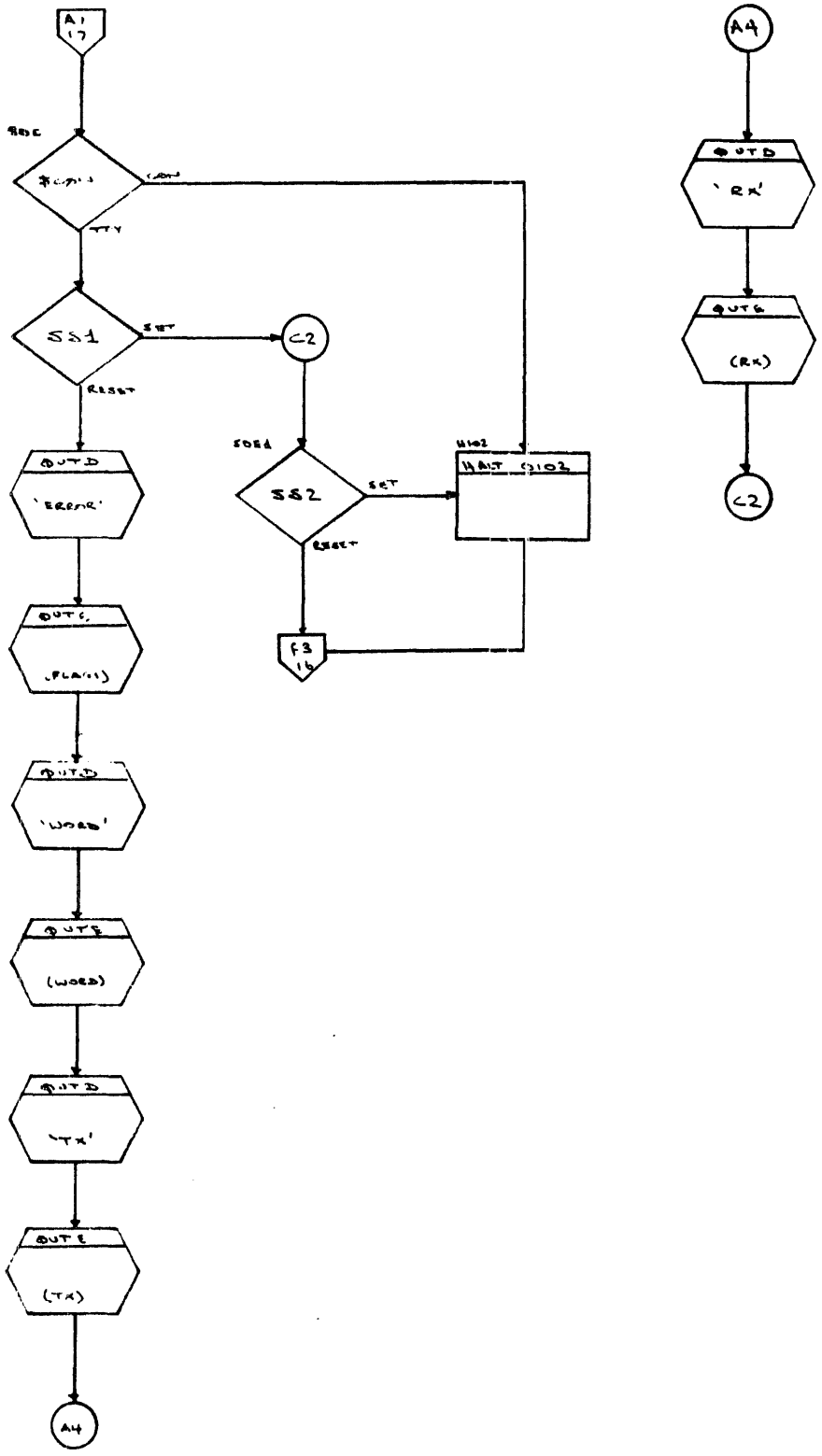
varian data machines a varian subsidiary	CODE IDENT. NO.	89A0228	REV. A
	PREPARED BY	APPROVED BY	SHEET 51 OF 70

PROGRAMMER	PROGRAM NO.	DATE	PAGE 17
CHART I.D.	CHART NAME	PROGRAM NAME	



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	PREPARED BY	APPROVED BY	SHEET 52 OF 70

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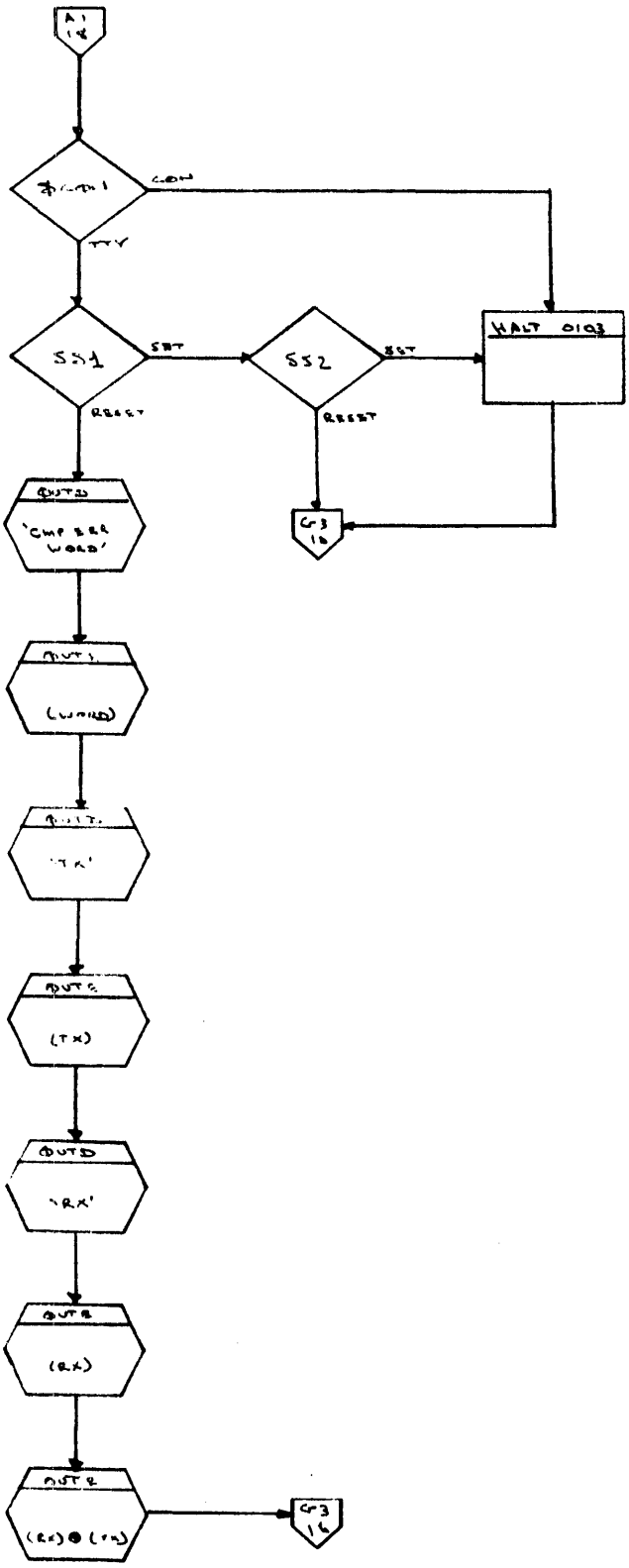
PROGRAMMER	PROGRAM NO.	DATE	PAGE 18
CHART I.D.	CHART NAME	PROGRAM NAME	



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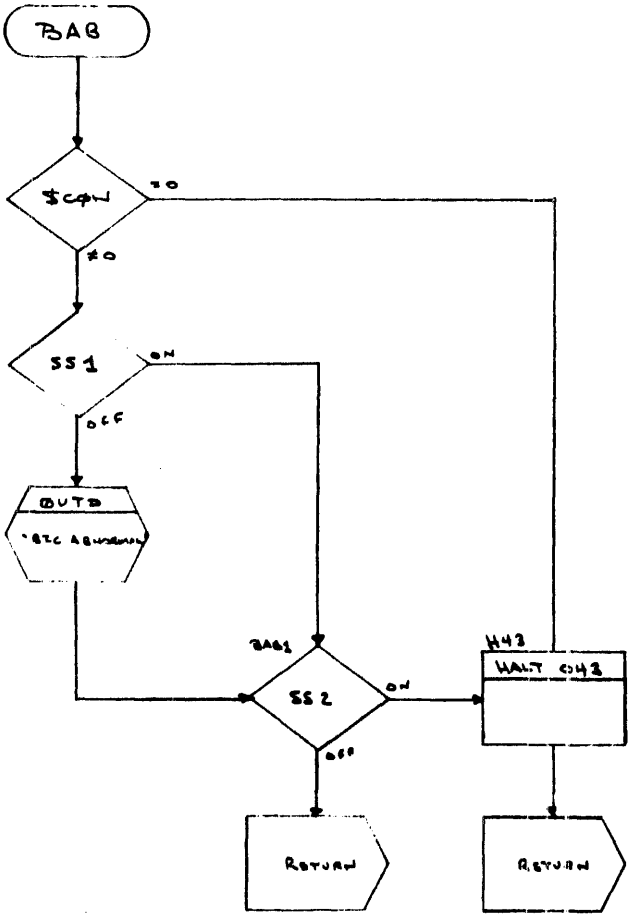
varian data machines a varian subsidiary	CODE IDENT. NO.	89A0228	REV. A
	PREPARED BY	APPROVED BY	SHEET 53 OF 70

PROGRAMMER	PROGRAM NO.	DATE	PAGE 19
CHART I.D.	CHART NAME	PROGRAM NAME	



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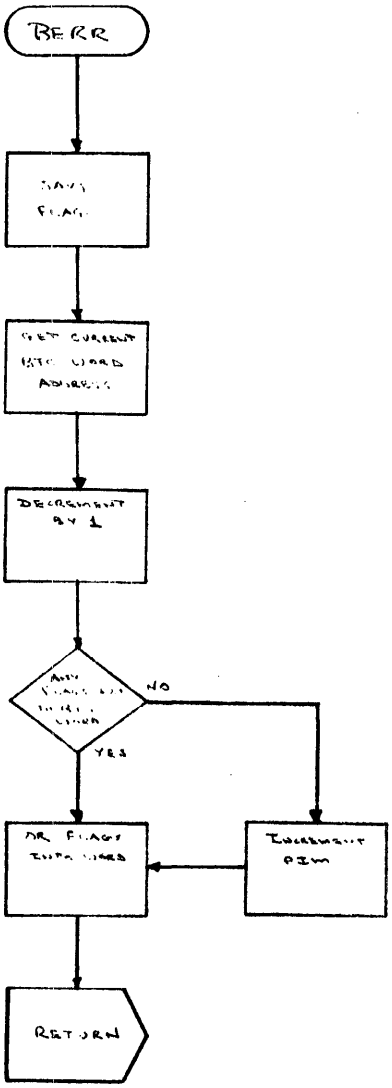

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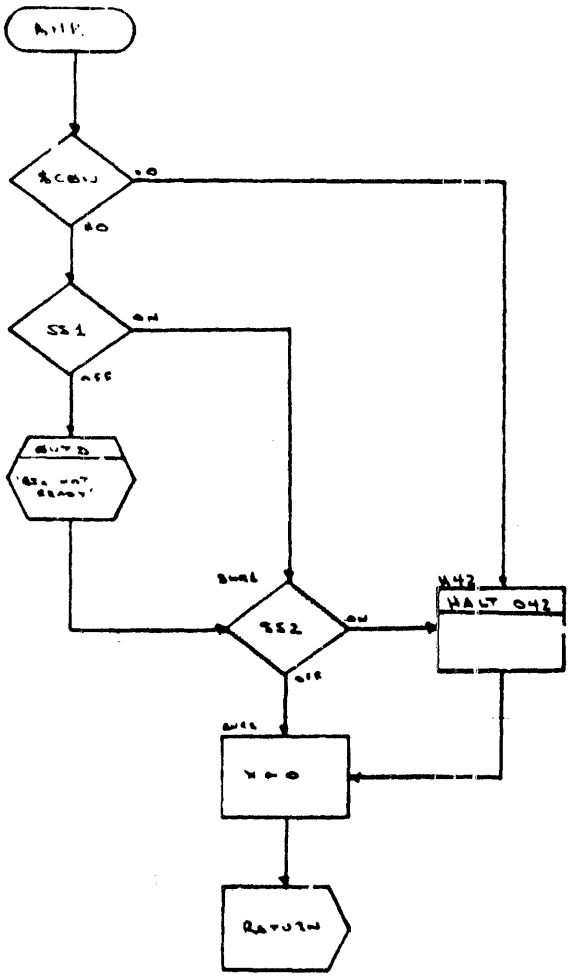
PROGRAMMER	PROGRAM NO.	DATE	PAGE 21
CHART I.D.	CHART NAME	PROGRAM NAME	



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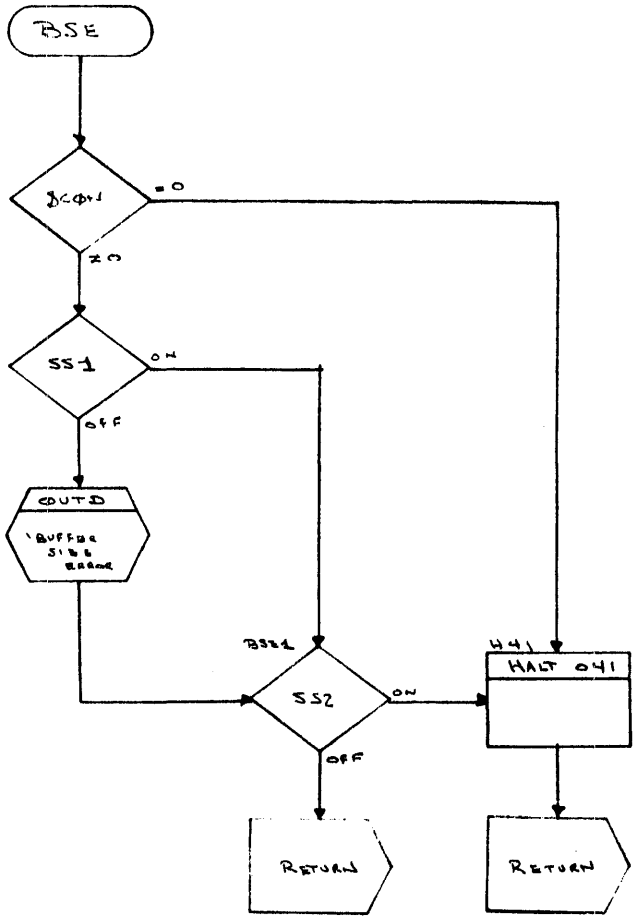
verian data machines a verian subsidiary	CODE IDENT. NO.	89A0228	REV. A
PREPARED BY	APPROVED BY	SHEET 56 OF 70	

PROGRAMMER	PROGRAM NO.	DATE	PAGE 22
CHART I.D.	CHART NAME	PROGRAM NAME	



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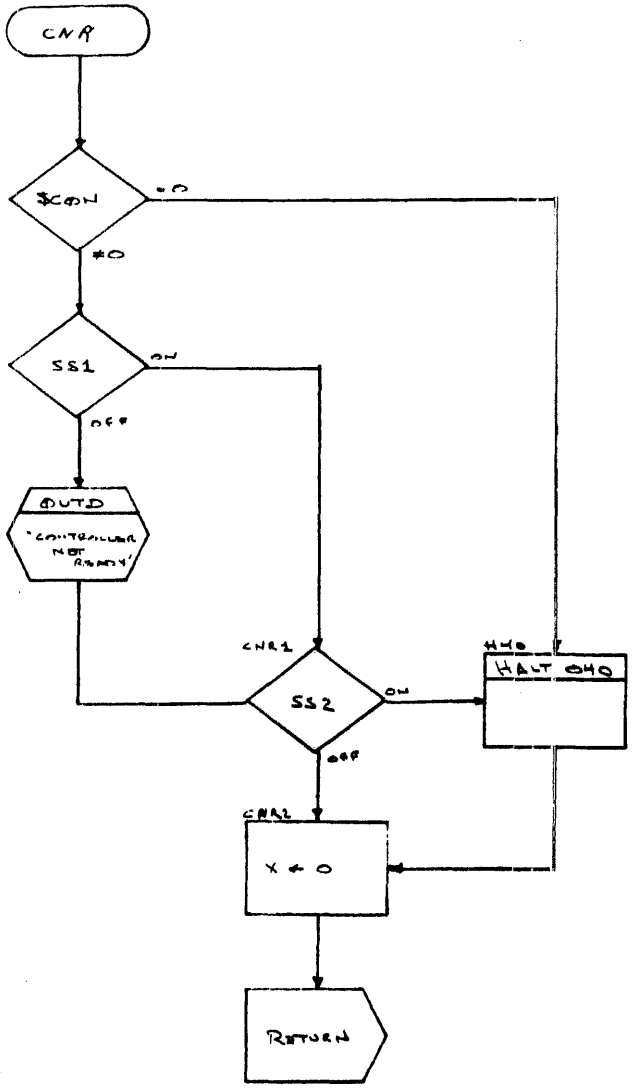
varian data machines a varian subsidiary	CODE IDENT. NO.	89A0228	REV. A
	PREPARED BY	APPROVED BY	SHEET 57 OF 70

89A0240-000A

PROGRAMMER	PROGRAM NO.	DATE	PAGE 23
CHART I. D.	CHART NAME	PROGRAM NAME	



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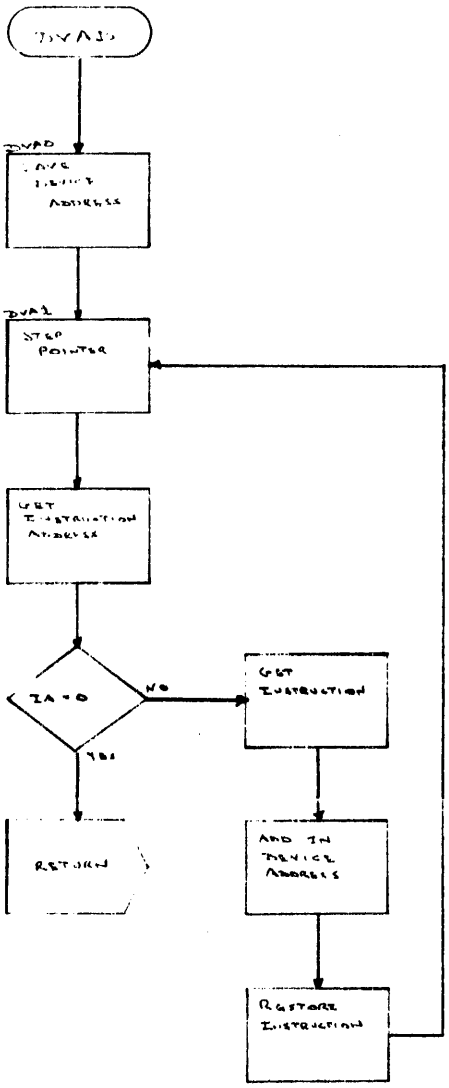
varian data machines a varian subsidiary	CODE IDENT. NO.	89A0228	REV. A
	PREPARED BY	APPROVED BY	SHEET 58 OF 70

PROGRAMMER	PROGRAM NO.	DATE	PAGE 24
CHART I.D.	CHART NAME	PROGRAM NAME	



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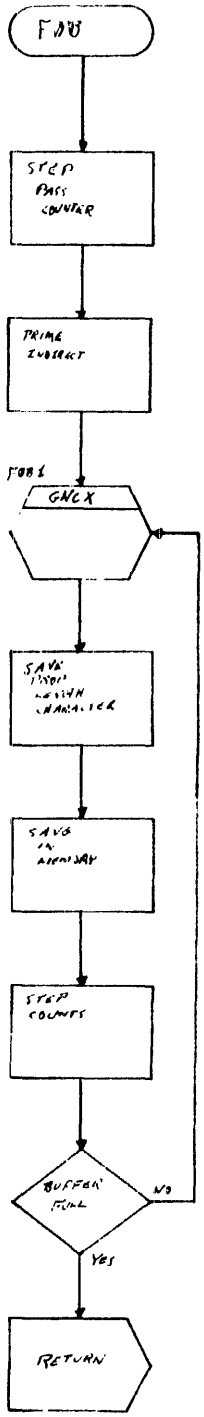
varian data machines a varian subsidiary	CODE IDENT. NO.	89A0228	REV. A
	PREPARED BY	APPROVED BY	SHEET 54 OF 70

PROGRAMMER	PROGRAM NO.	DATE	PAGE 25
CHART I. D.	CHART NAME	PROGRAM NAME	



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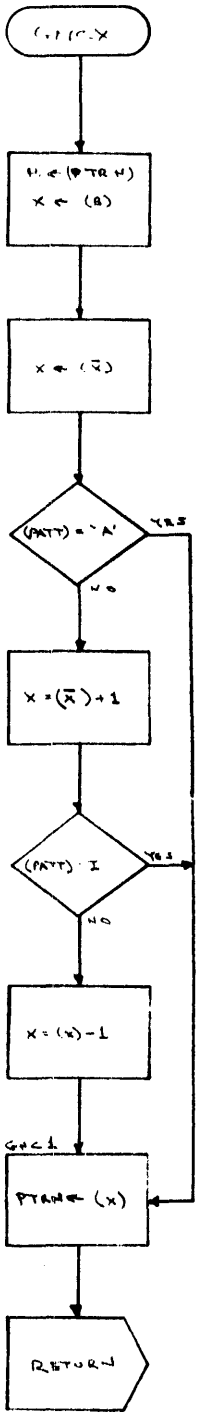
varian data machines a varian subsidiary	CODE IDENT. NO.	89A0228	REV. A
	PREPARED BY	APPROVED BY	SHEET 60 OF 70

PROGRAMMER	PROGRAM NO.	DATE	PAGE 26
CHART I.D.	CHART NAME	PROGRAM NAME	



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varian data machines
a varian subsidiary

CODE IDENT. NO.		89A0228	REV. A
PREPARED BY	APPROVED BY	SHEET 61 OF 70	

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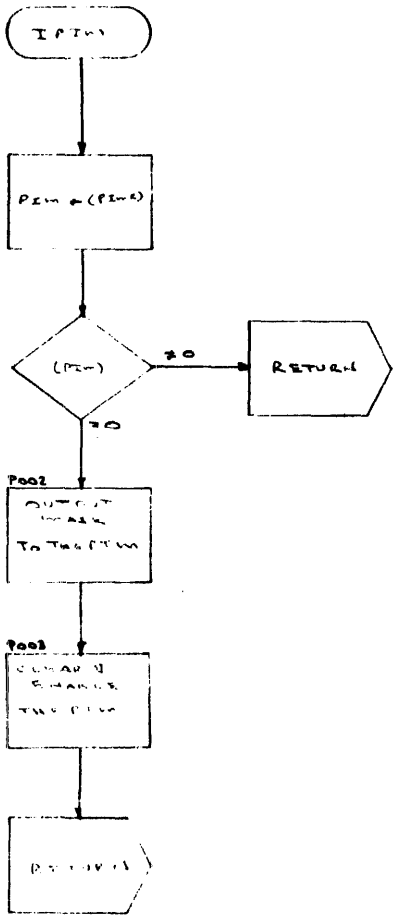

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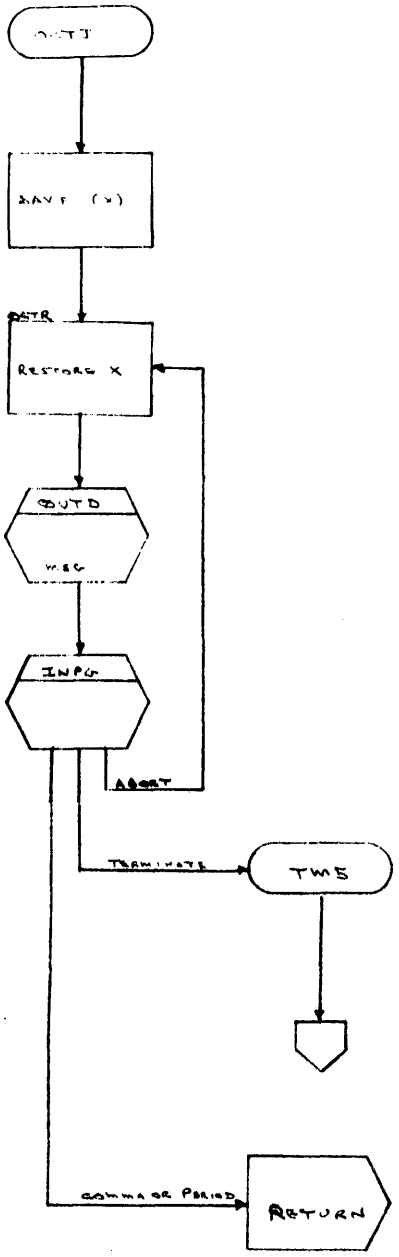
CHART I.D.	CHART NAME	PROGRAM NAME	



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varian data machines
a varian subsidiary

CODE IDENT. NO.		89A0228	REV. A
PREPARED BY	APPROVED BY	SHEET 63 OF 70	

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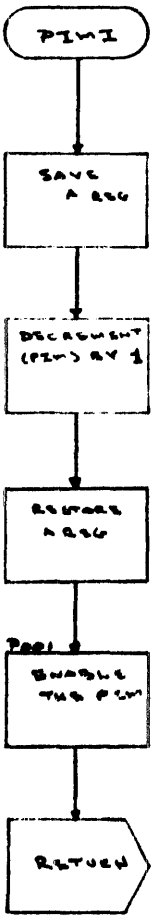
PROGRAMMER	PROGRAM NO.	DATE	PAGE 29
CHART I.D.	CHART NAME	PROGRAM NAME	



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PREPARED BY	APPROVED BY	SHEET 64 OF 70	

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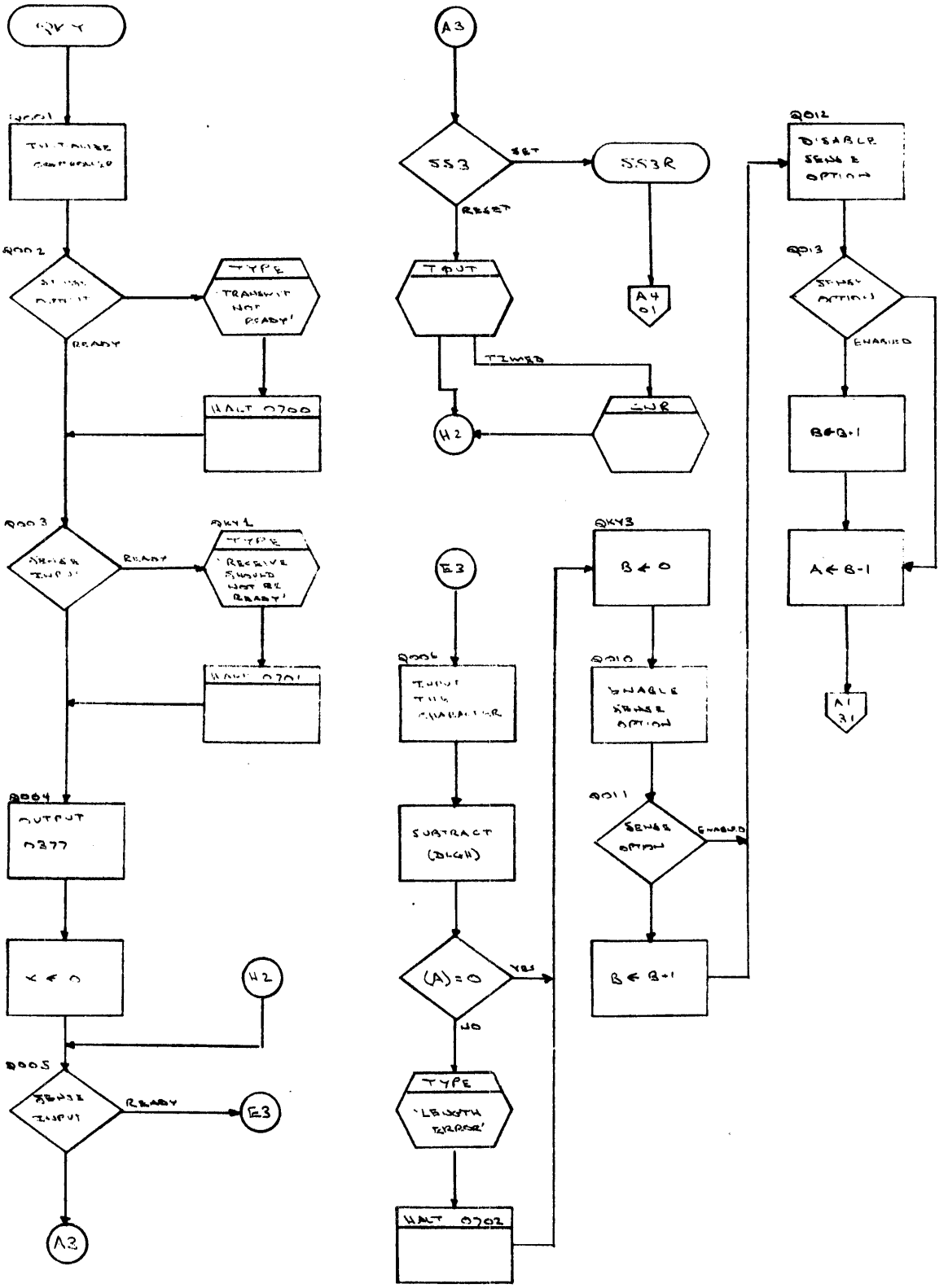

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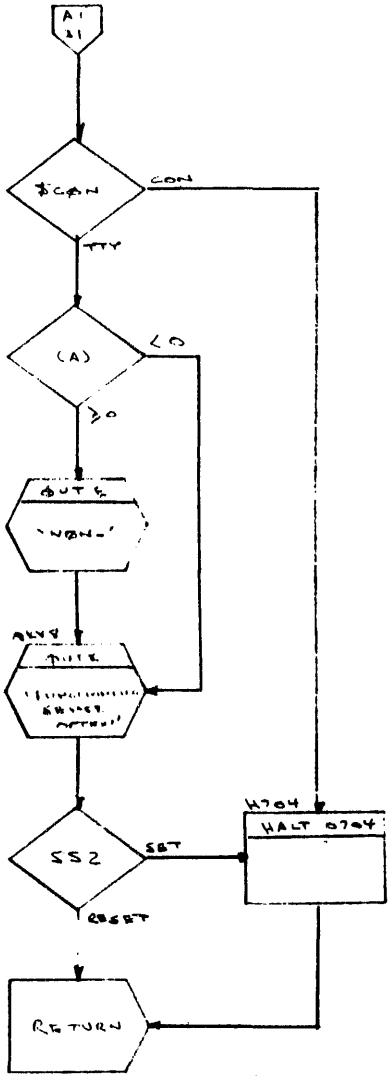

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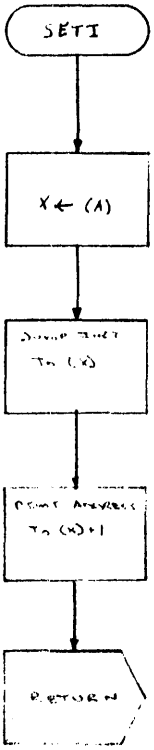
PROGRAMMER	PROGRAM NO.	DATE	PAGE 32
CHART I.D.	CHART NAME	PROGRAM NAME	



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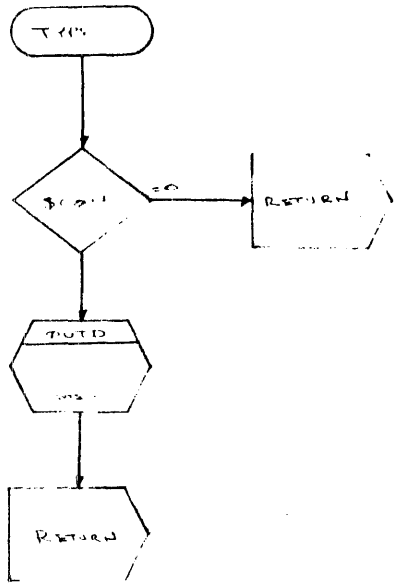
varian data machines
a varian subsidiary

CODE IDENT. NO.	89A0223	REV. A
PREPARED BY	APPROVED BY	SHEET 67 OF 70

PROGRAMMER	PROGRAM NO.	DATE	PAGE 33
CHART I.D.	CHART NAME	PROGRAM NAME	



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varian data machines
a varian subsidiary

CODE IDENT. NO.		89A0228	REV. A
PREPARED BY	APPROVED BY	SHEET 68 OF 110	

SECTION 4
TEST SPECIFICATIONS

4.1 OBJECTIVES

The purpose of this section is to describe to what extent the program has been validated in terms of variations in applicable hardware, configurations and other external input parameters. Using the teletype mode of operation, actual hardcopy of each test variance is presented. This will provide an aid in evaluating future claimed discrepancies observed in the program.

4.2 CONFIGURATIONS

This program has been exercised on the following hardware configuration:

1) 620/i - 4K memory

4.3 DETAILED DESCRIPTIONS

The following hard copy printout is provided to validate the responses received for each respective input:

```
        UNIVERSAL ASYNCHRONOUS SERIAL CONTROLLER TEST

        UASC DA          2.
        DATA LENGTH      8
        PATTERN          F377.
        PIM REQUIRED     N
        MODE             SE
        FUNCTIONING SENSE OPTION

        000025 PASSES
        PATTERN          A252.
        PIM REQUIRED     Y
        PIM DA           40.
        TX INT LOC       100.

        RX INT LOC       102.
        ER INT LOC       104.
        MASK             370.
        MODE             SE
        FUNCTIONING SENSE OPTION
```

```
000013 PASSES
PATTERN          IO.
PIM REQUIRED     Y
MODE             BI
BIC DA           20.
BIC DIRECTION    T
FUNCTIONING SENSE OPTION

000027 PASSES
PATTERN          C
000016 PASSES
PATTERN          FO.
PIM REQUIRED     N
MODE             BI
BIC DIRECTION    R
FUNCTIONING SENSE OPTION

000022 PASSES

PATTERN

UASC DA
```

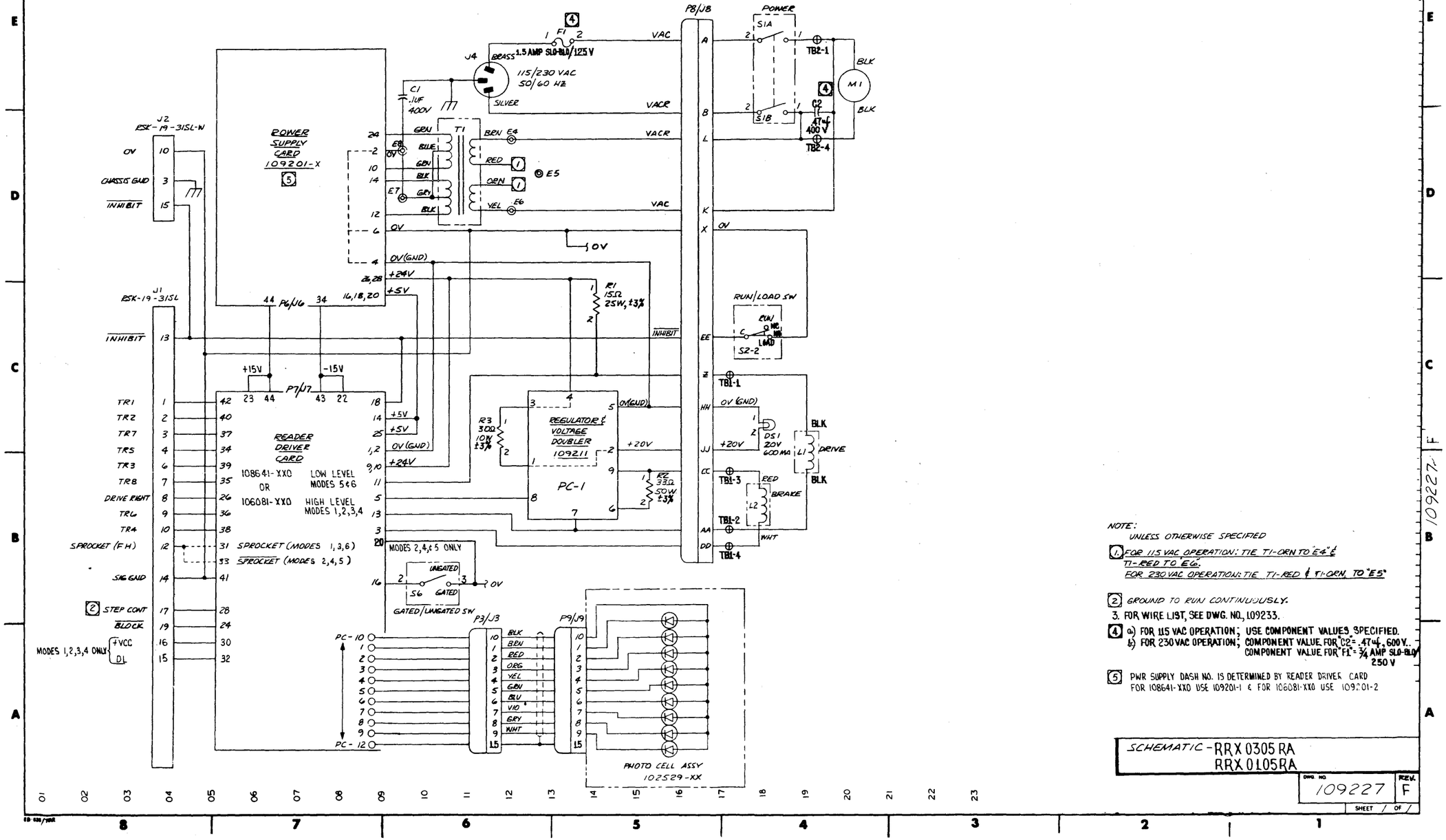


Figure 8-1. Overall Schematic, RR-0105/305RA.

Figure 8-2. Schematic, Reader/Driver Card II.

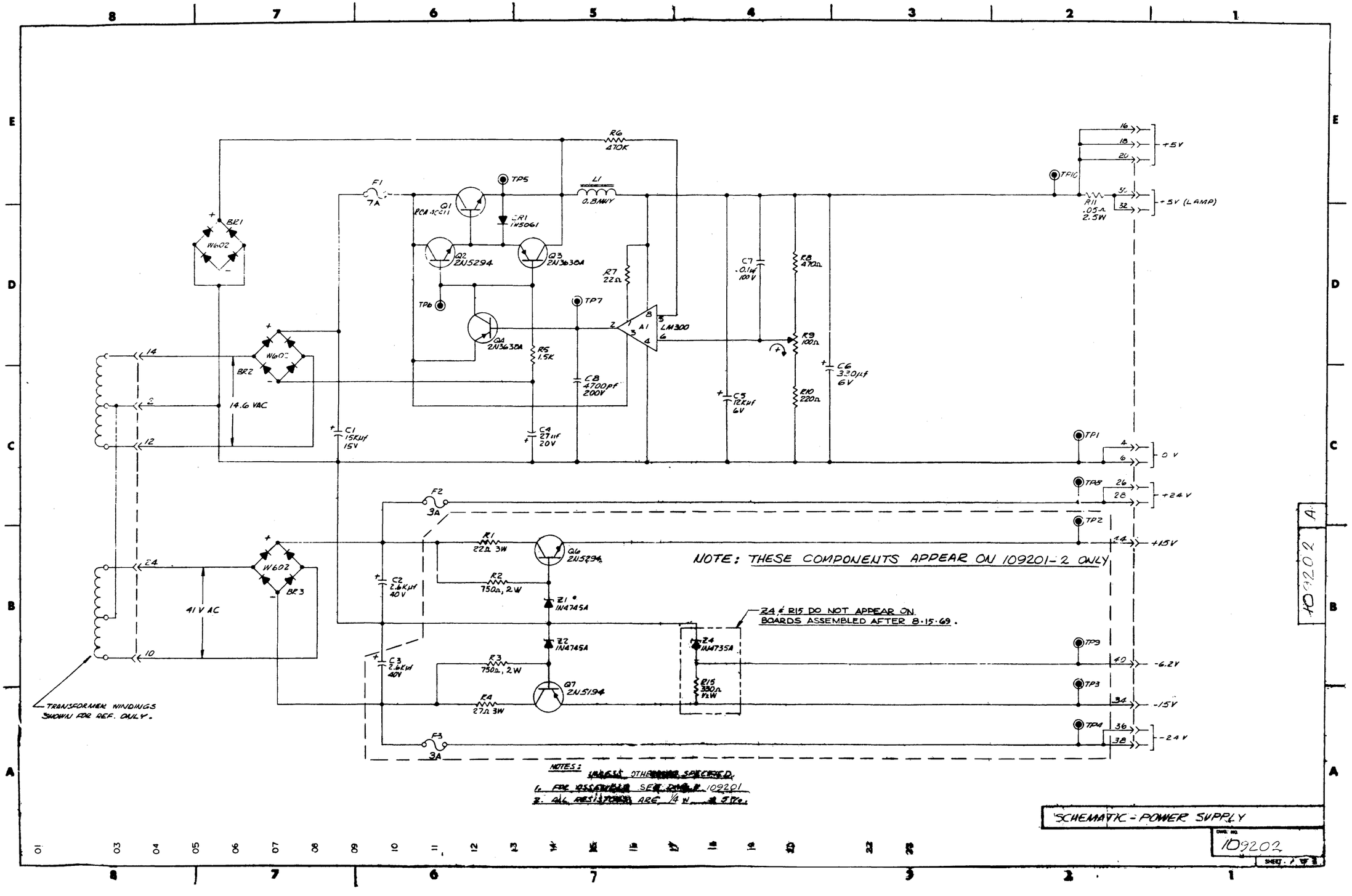
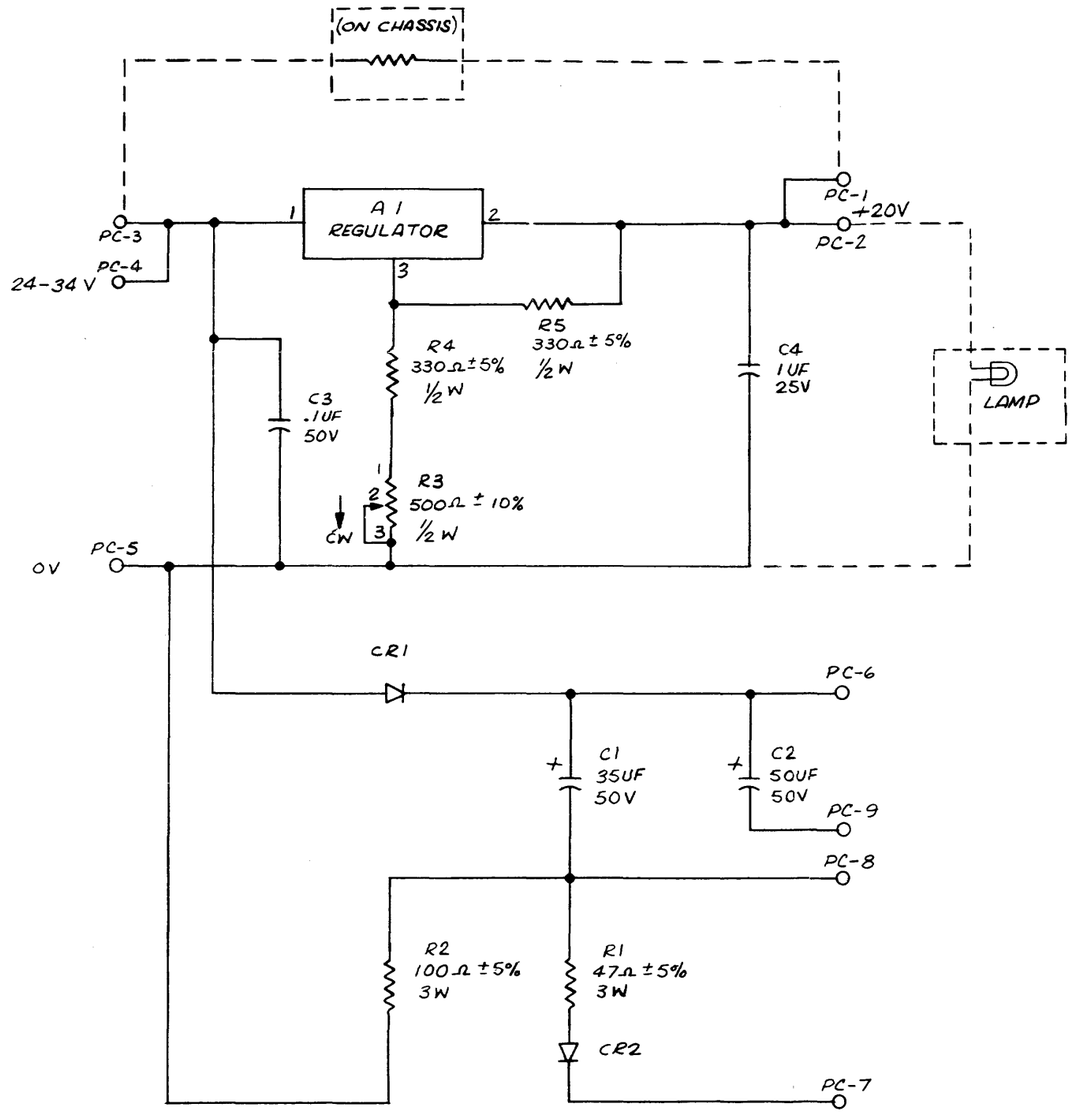


Figure 8-3. Schematic, Power Supply Card.



NOTE: UNLESS OTHERWISE SPECIFIED

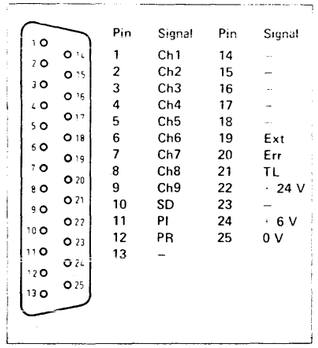
1. REF ASSY DWG NO. 109211
2. CR1 & CR2 ARE 704000-107 (IN5059)
3. A1 IS 704520-109 (LM309K)

TITLE	SCHEMATIC - REGULATOR AND VOLTAGE DOUBLER
	RR/RRS-0305
CODE IDENT. NO.	SIZE C — DWG. NO. 109212A
SCALE ——	WT. — SHEET 1 OF 1

109212 A

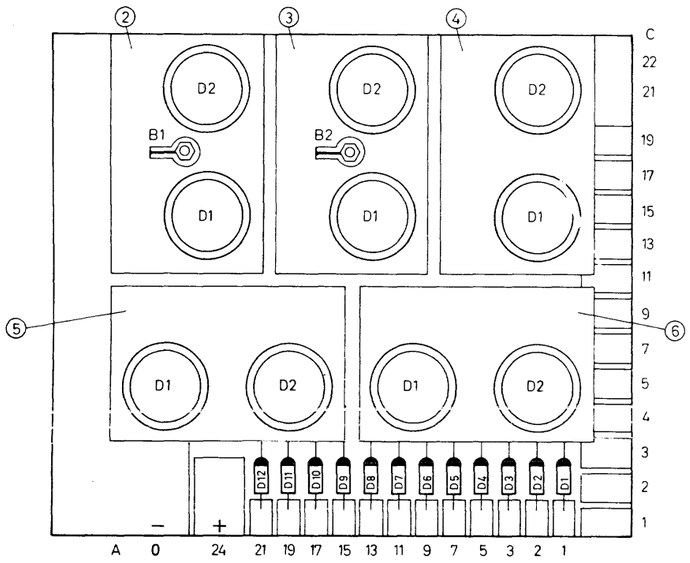
Figure 8-4. Schematic, Regulator and Voltage Doubler Card.

Signal connector P1

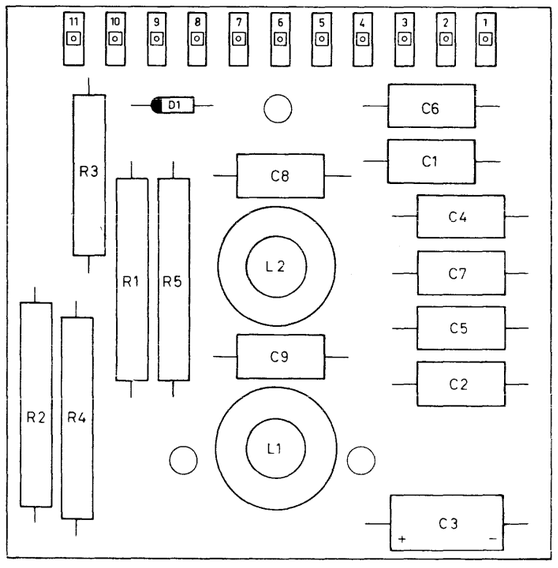


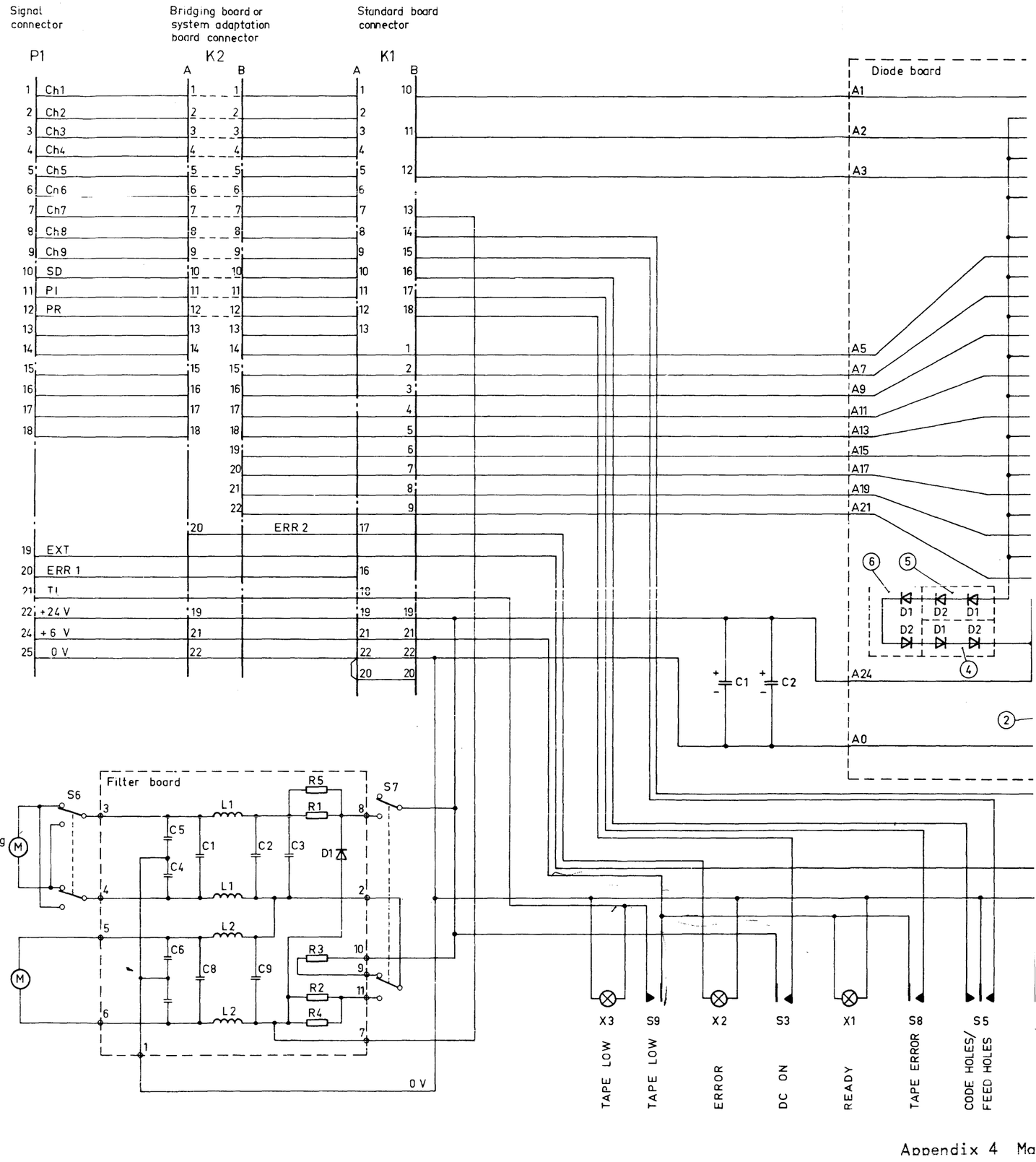
Pin	Signal	Pin	Signal
1	Ch1	14	–
2	Ch2	15	–
3	Ch3	16	–
4	Ch4	17	–
5	Ch5	18	–
6	Ch6	19	Ext
7	Ch7	20	Err
8	Ch8	21	TL
9	Ch9	22	+ 24 V
10	SD	23	–
11	PI	24	+ 6 V
12	PR	25	0 V
13	–		

Diode board

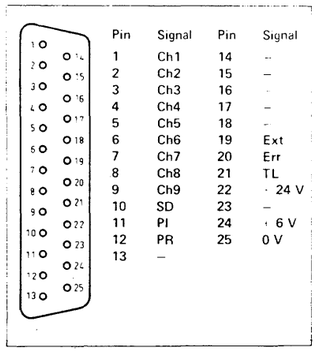


Filter circuit board

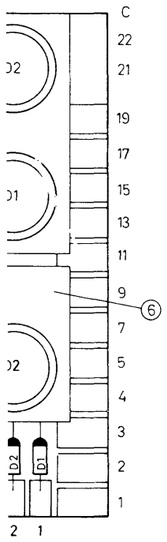


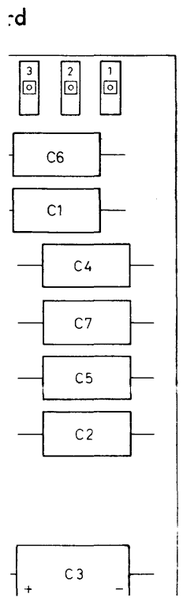


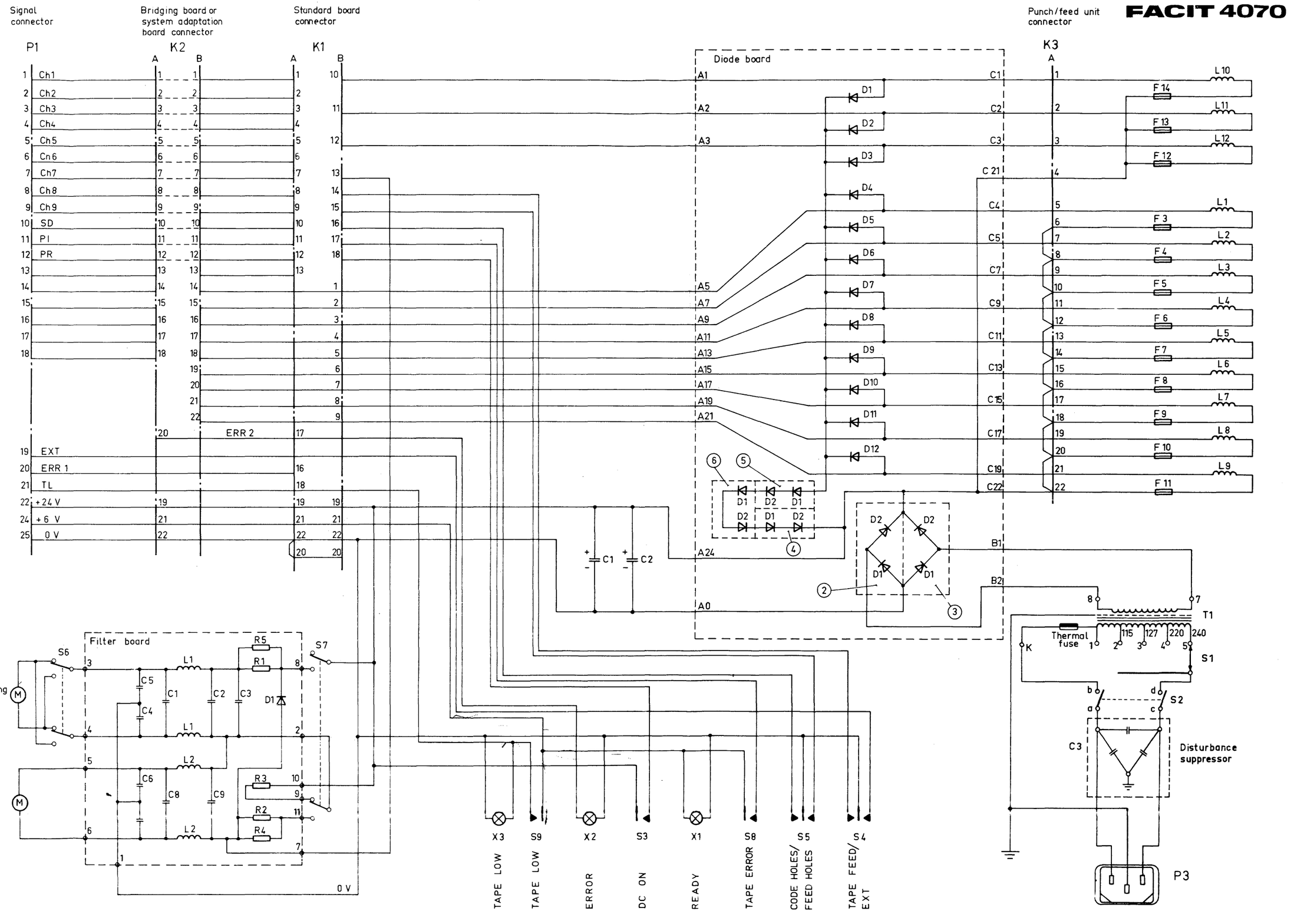
Signal connector P1



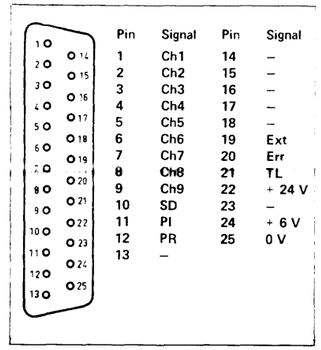
Pin	Signal	Pin	Signal
1	Ch1	14	–
2	Ch2	15	–
3	Ch3	16	–
4	Ch4	17	–
5	Ch5	18	–
6	Ch6	19	Ext
7	Ch7	20	Err
8	Ch8	21	TL
9	Ch9	22	+ 24 V
10	SD	23	–
11	PI	24	+ 6 V
12	PR	25	0 V
13	–		







Signal connector P1



Pin	Signal	Pin	Signal
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2	Ch2	15	–
3	Ch3	16	–
4	Ch4	17	–
5	Ch5	18	–
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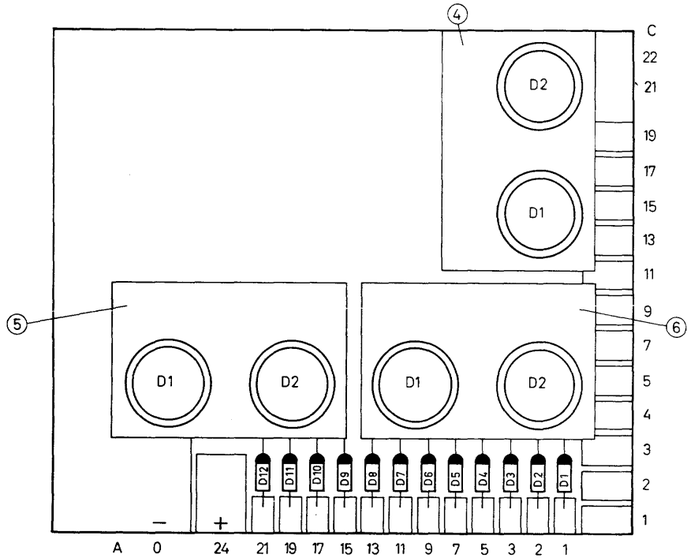
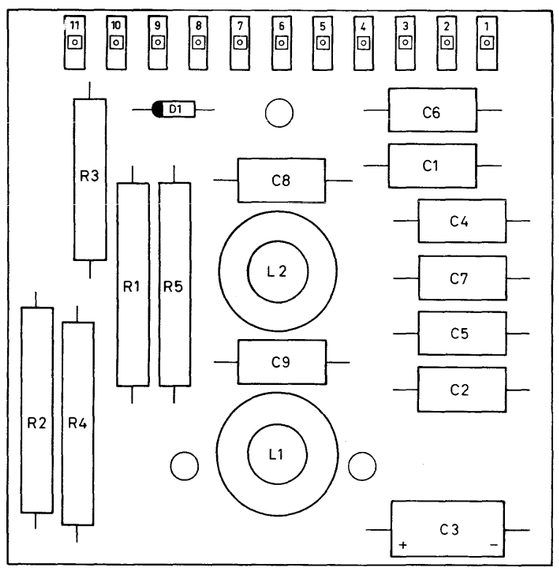
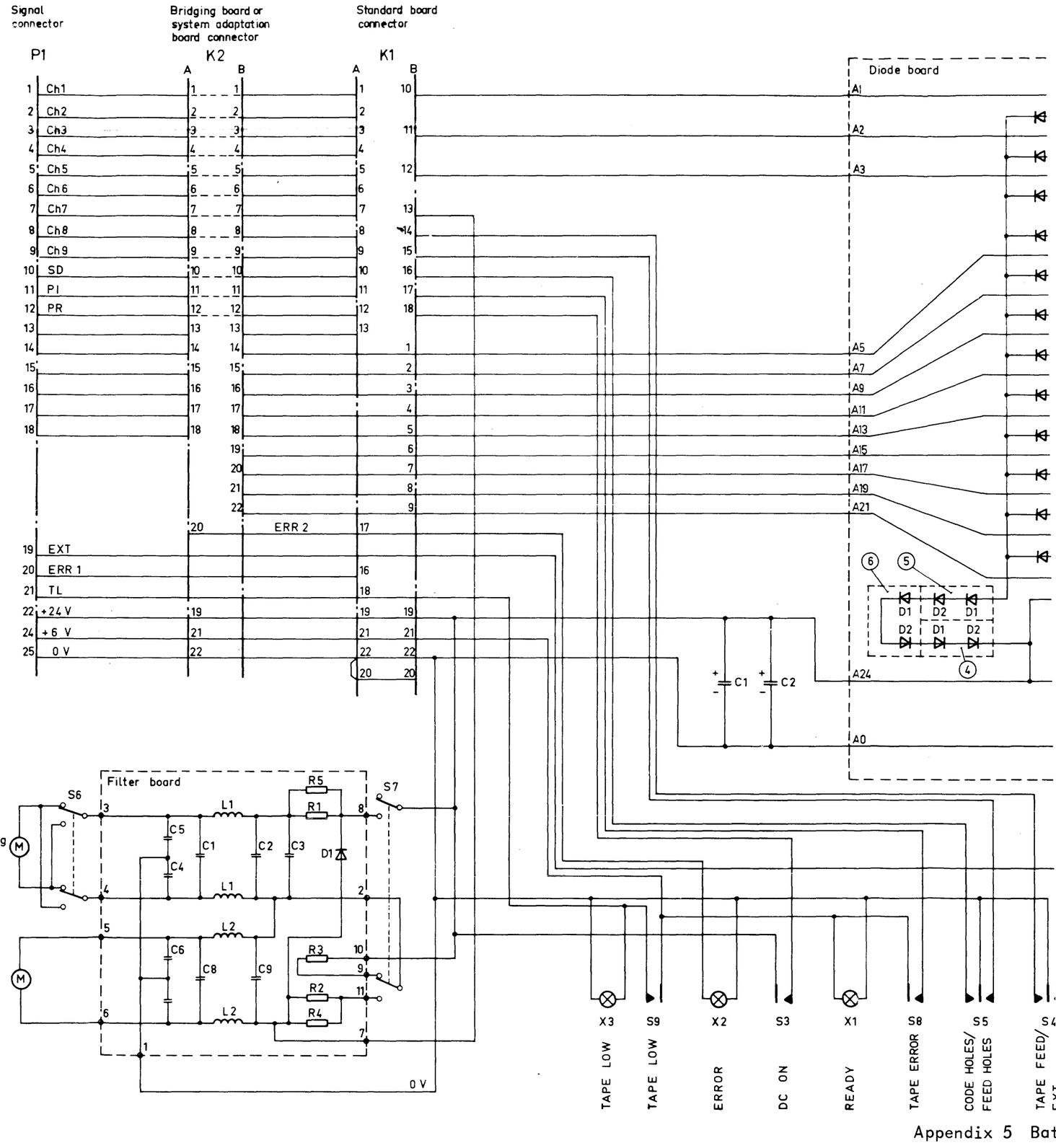
7	Ch7	20	Err
8	Ch8	21	TL
9	Ch9	22	+ 24 V
10	SD	23	–
11	PI	24	+ 6 V
12	PR	25	0 V
13	–		

Diode board



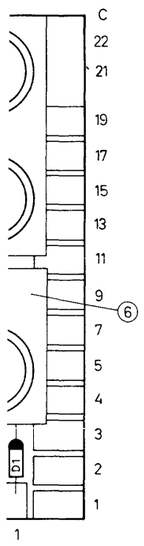
Filter circuit board



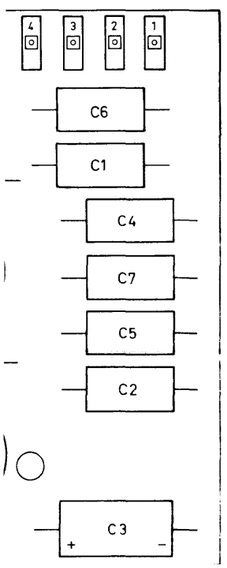


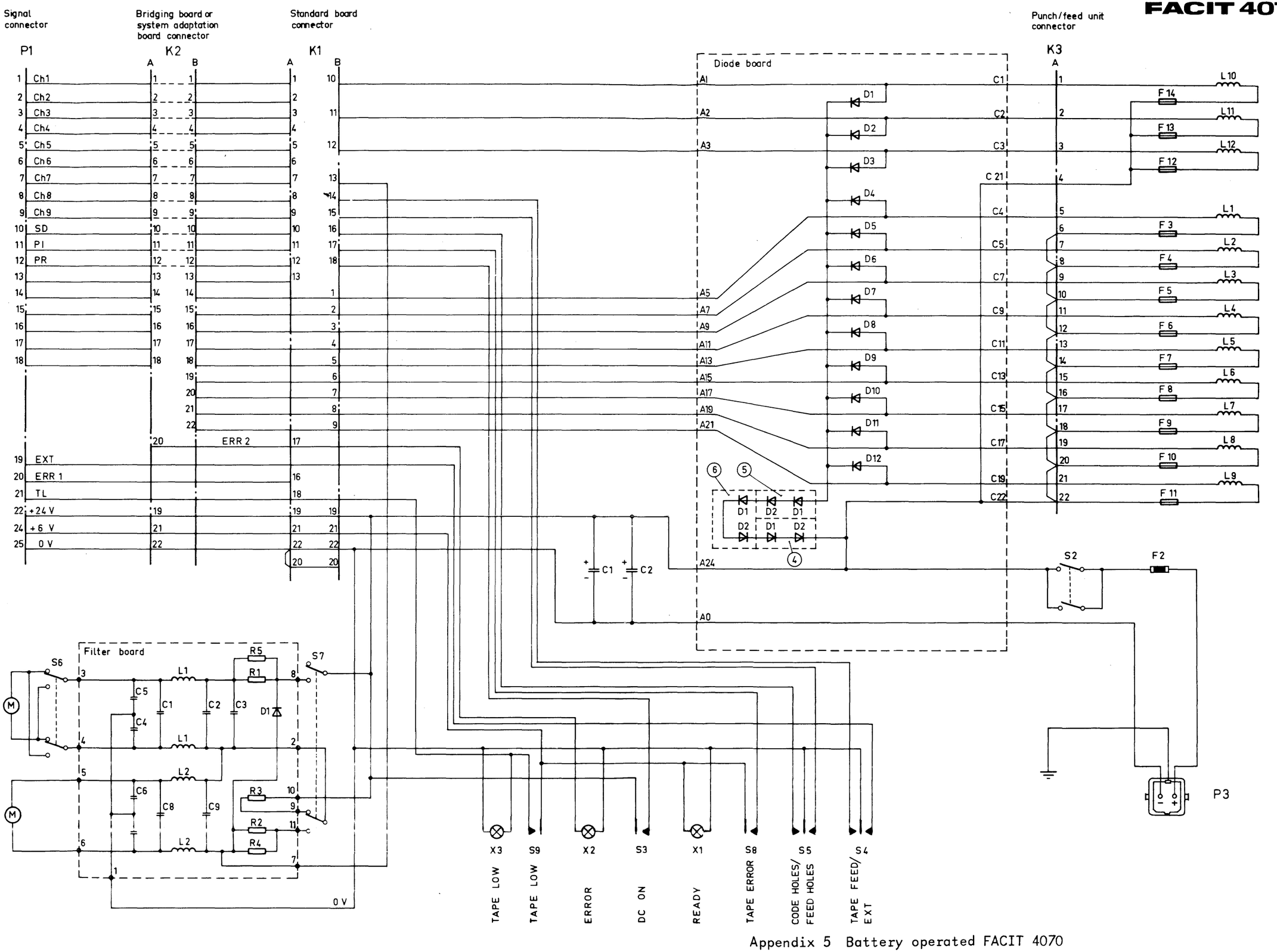
ıl connector P1

Pin	Signal	Pin	Signal
1	Ch1	14	–
2	Ch2	15	–
3	Ch3	16	–
4	Ch4	17	–
5	Ch5	18	–
6	Ch6	19	Ext
7	Ch7	20	Err
8	Ch8	21	TL
9	Ch9	22	+ 24 V
10	SD	23	–
11	PI	24	+ 6 V
12	PR	25	0 V
13	–		



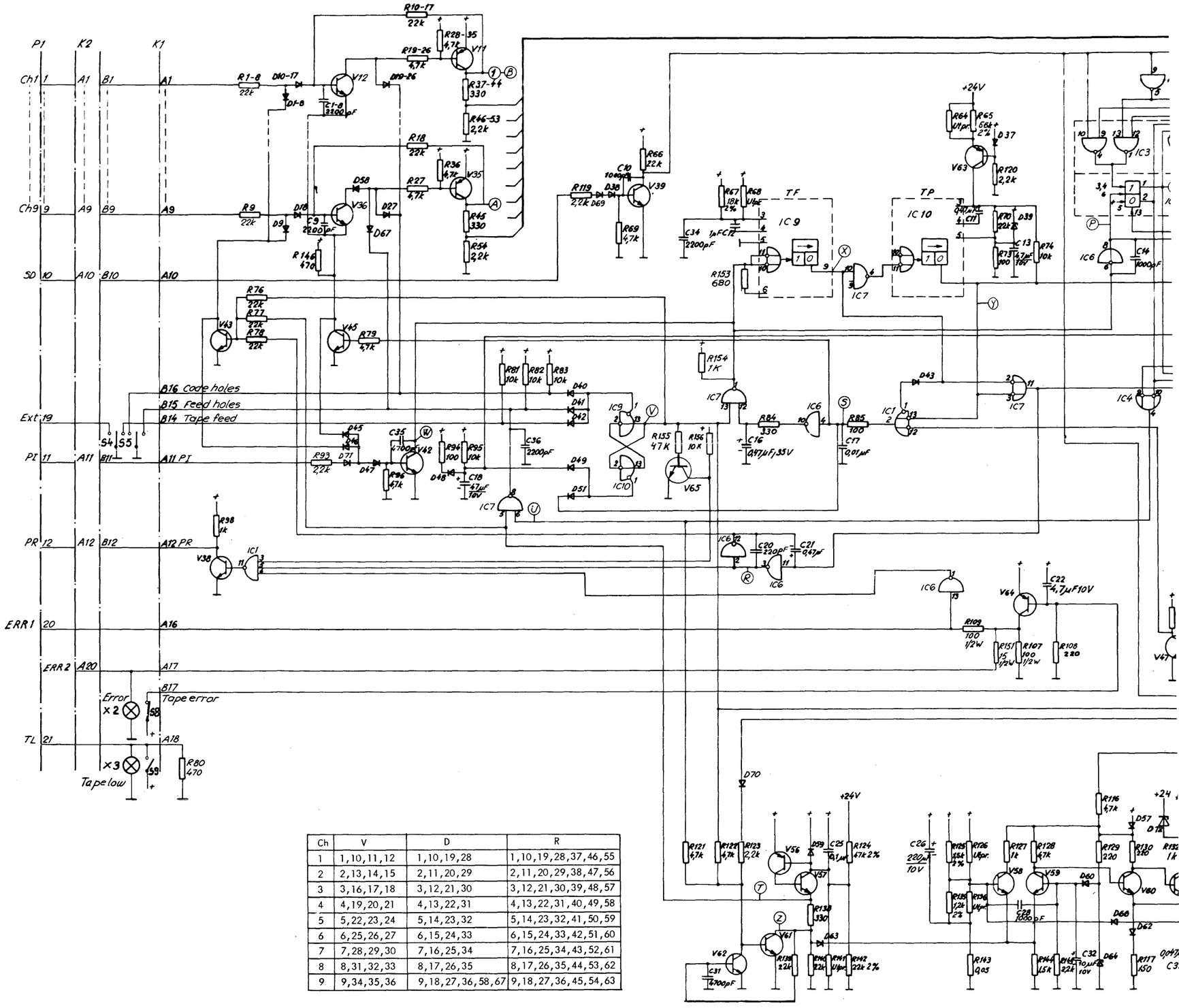
t board



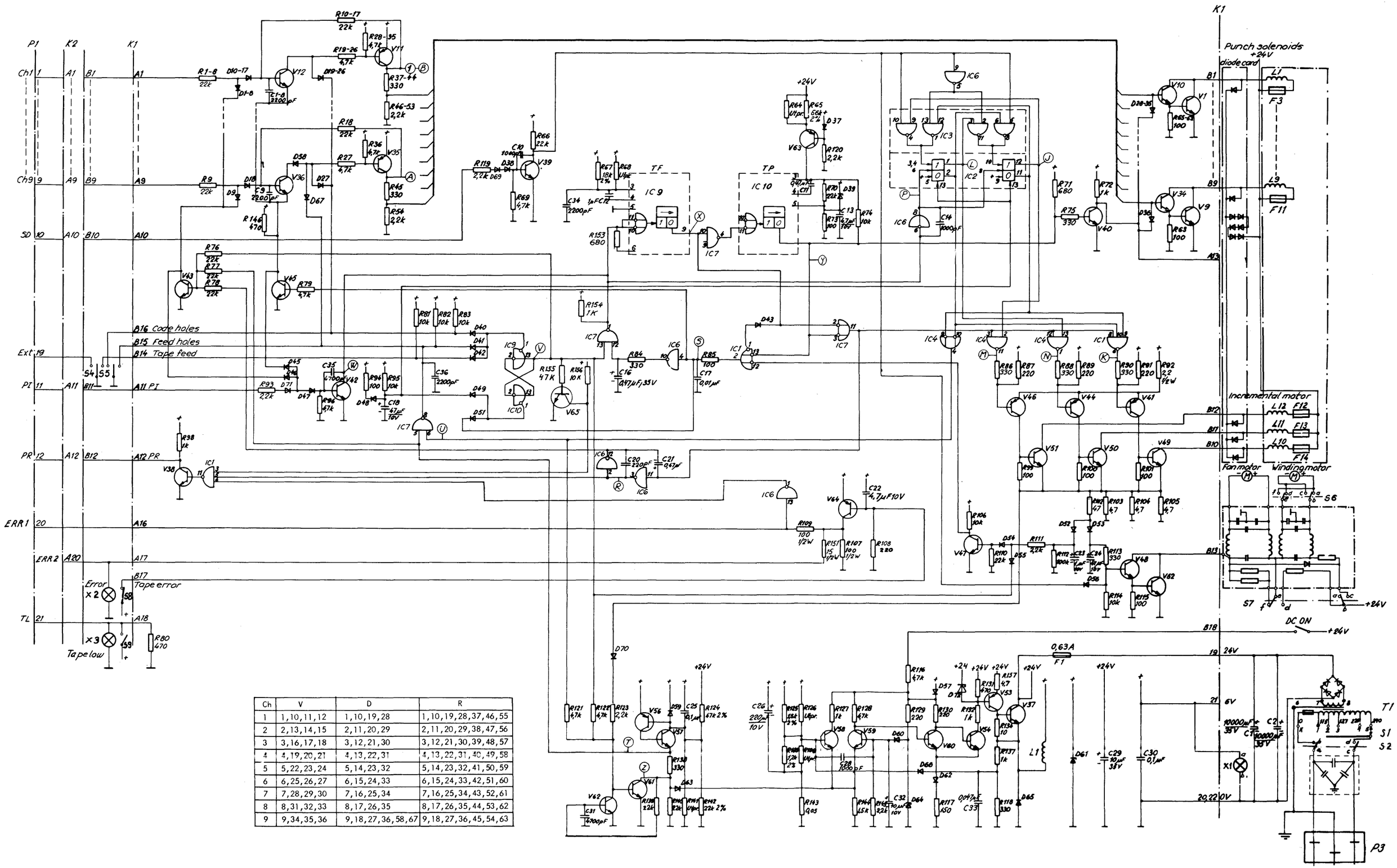


Appendix 5 Battery operated FACIT 4070

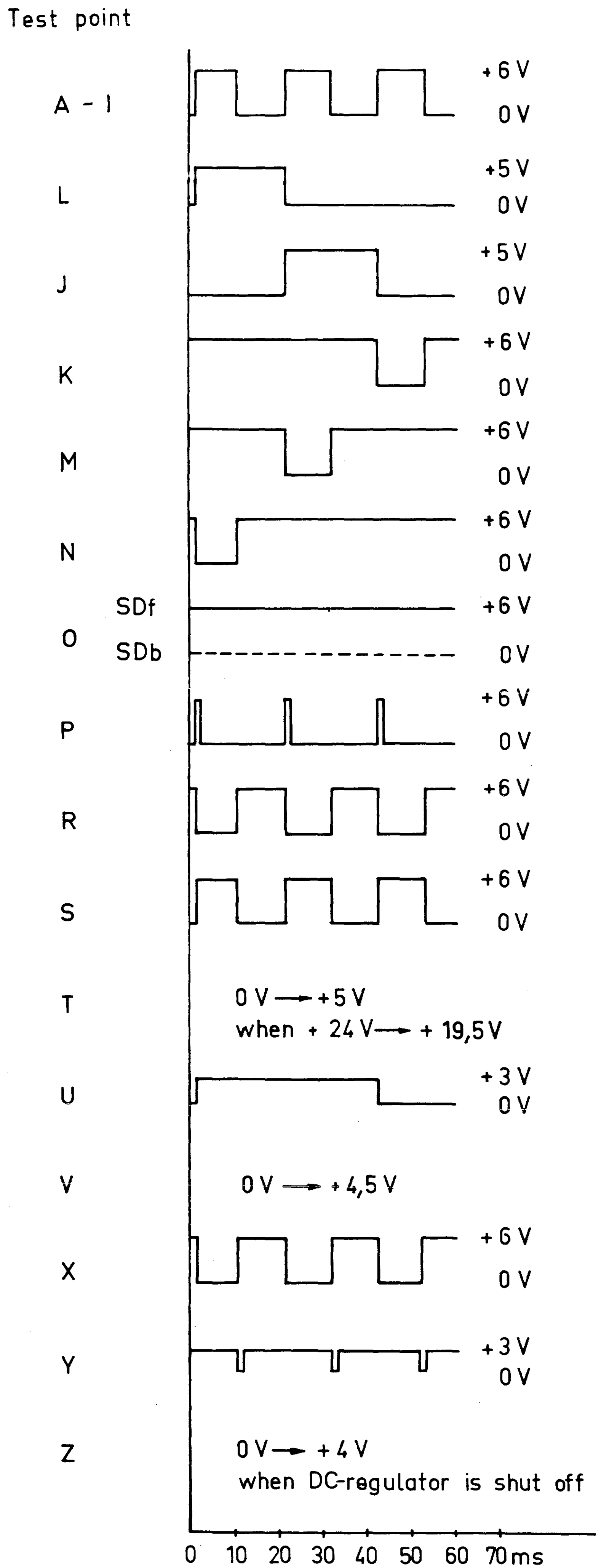
C	D	R	V
		10–17	
		28–35	
		19–26	11
	10–17, 19–26	1–8, 37–44	12
1–8	1–8		
			10
	28–35	46–53, 64, 65	1
		55–62	
	37	18	
		66	63
10		36, 120	
	58	27	35
	38, 69	119, 67, 68	39
11	18, 27, 39	9, 45, 70–72	36
9, 34, 12	9, 67	69	34
13, 14	36	73–75	40, 9
		146, 54, 63	
		153	
		76	
		77	
		78, 79	43, 45
		154	
	43	81–83, 154	
	40		
	41		
	42	84, 85	
	45	86–92	
35, 36, 16, 17	46	94, 95, 155, 156	
	71, 47, 49	93	42
	48	96	65, 46, 44, 41
18			
	51		
		98	51, 50, 49
20, 21			
		99–101	
			38
22			
		102–105	64
	52, 53	106	
		109	
	54	151, 107, 108, 111	47
23, 24	55	110, 112, 113	
			48
	56		
			52
		114, 115	
		80	
	70		
		116	
	57, 72	131, 157	
			53
25, 26	59	121–130, 132	56, 37
1, 2		134	57–60, 54
29, 30	61	135–137	
28		138	
	66		
	62, 63		61
32, 33	64, 65	139–145, 117, 118	62
31			

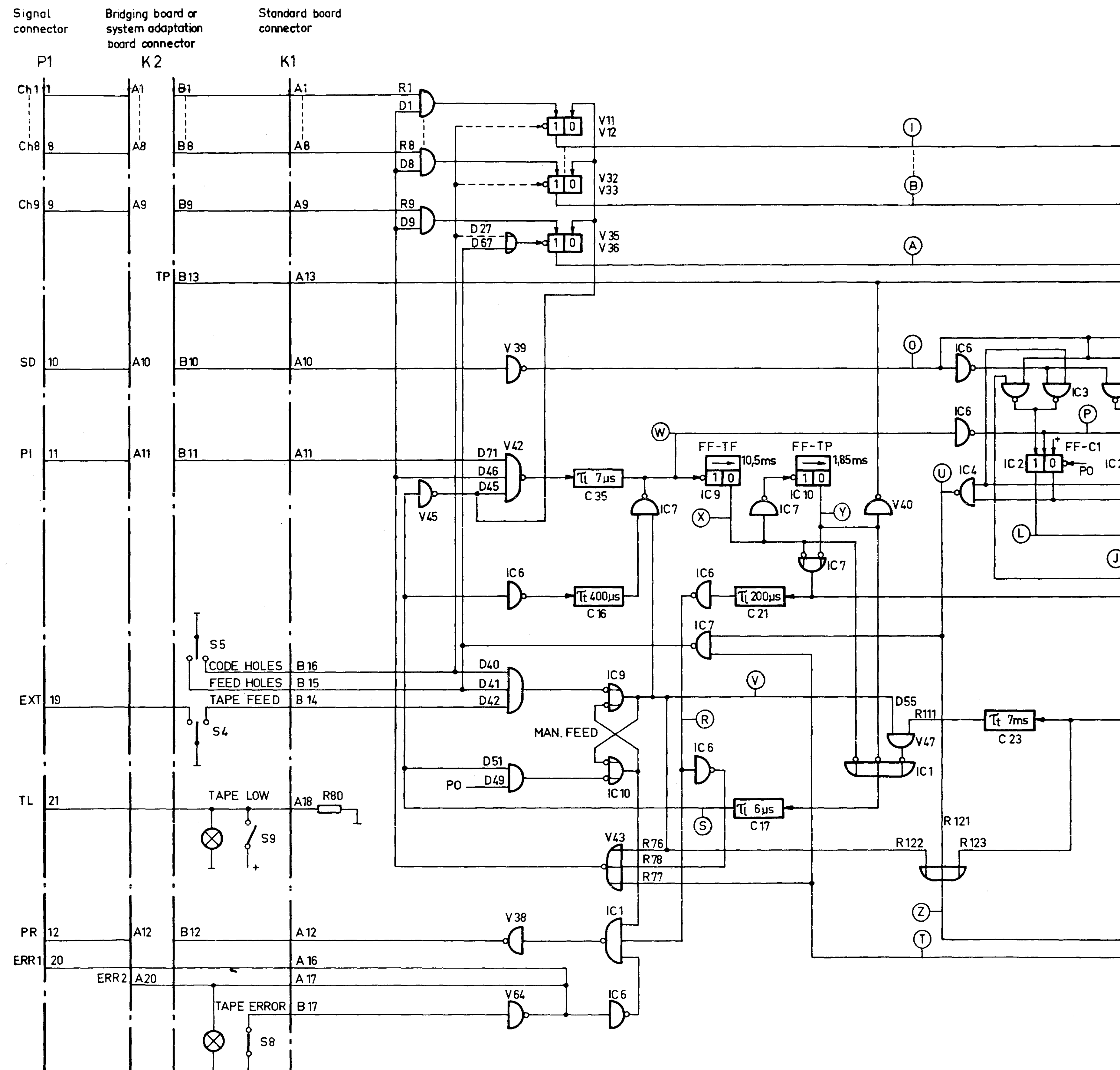


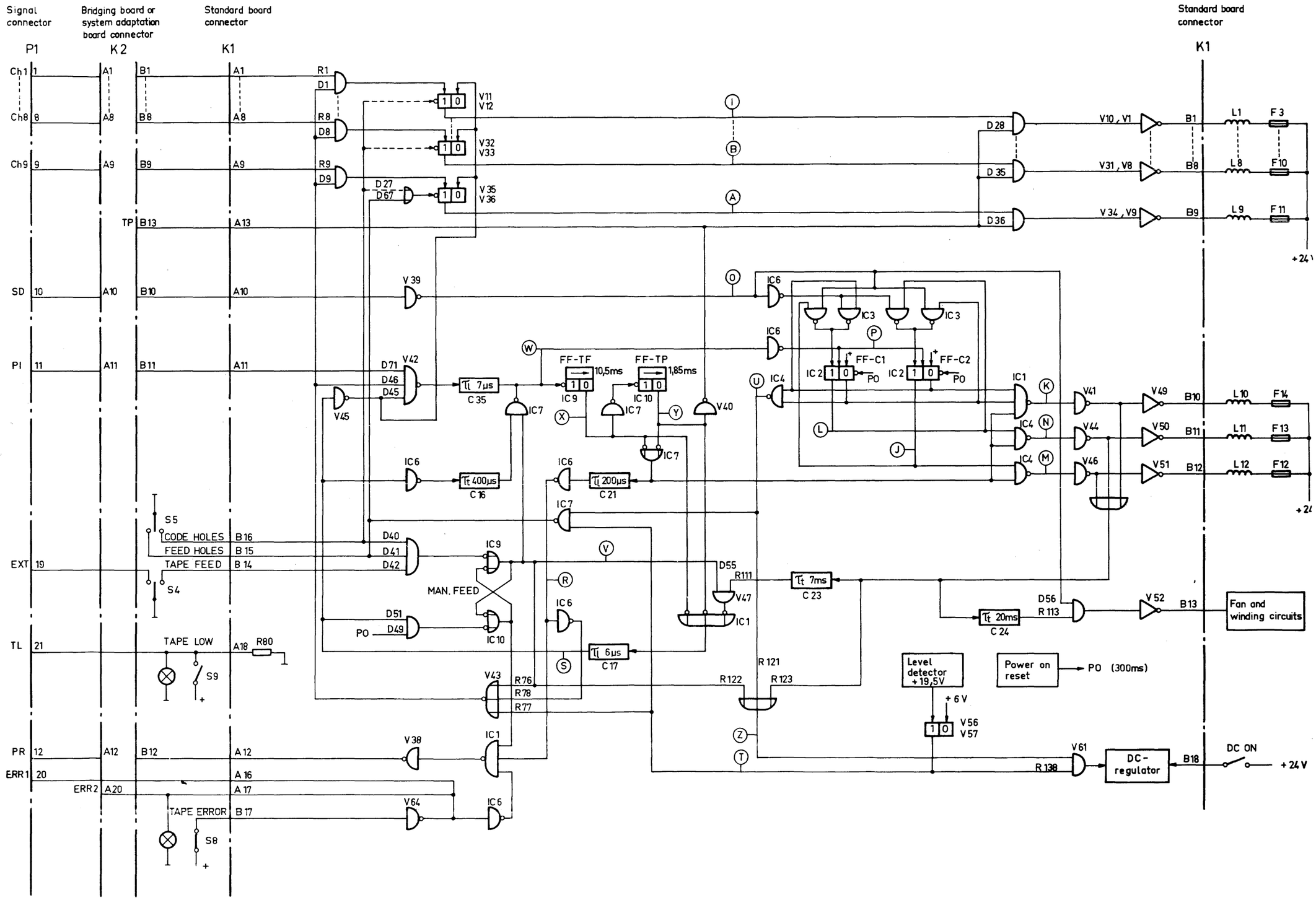
Ch	V	D	R
1	1,10,11,12	1,10,19,28	1,10,19,28,37,46,55
2	2,13,14,15	2,11,20,29	2,11,20,29,38,47,56
3	3,16,17,18	3,12,21,30	3,12,21,30,39,48,57
4	4,19,20,21	4,13,22,31	4,13,22,31,40,49,58
5	5,22,23,24	5,14,23,32	5,14,23,32,41,50,59
6	6,25,26,27	6,15,24,33	6,15,24,33,42,51,60
7	7,28,29,30	7,16,25,34	7,16,25,34,43,52,61
8	8,31,32,33	8,17,26,35	8,17,26,35,44,53,62
9	9,34,35,36	9,18,27,36,58,67	9,18,27,36,45,54,63



Ch	V	D	R
1	1,10,11,12	1,10,19,28	1,10,19,28,37,46,55
2	2,13,14,15	2,11,20,29	2,11,20,29,38,47,56
3	3,16,17,18	3,12,21,30	3,12,21,30,39,48,57
4	4,19,20,21	4,13,22,31	4,13,22,31,40,49,58
5	5,22,23,24	5,14,23,32	5,14,23,32,41,50,59
6	6,25,26,27	6,15,24,33	6,15,24,33,42,51,60
7	7,28,29,30	7,16,25,34	7,16,25,34,43,52,61
8	8,31,32,33	8,17,26,35	8,17,26,35,44,53,62
9	9,34,35,36	9,18,27,36,58,67	9,18,27,36,45,54,63


Test point
A - I
L
J
K
M
N
O
SDf
SDb
P
R
S
T
U
V
X
Y
Z
+6 V
0 V
+5 V
+3 V
0 V ⟶ +5 V
when + 24 V ⟶ + 19,5 V
0 V ⟶ + 4,5 V
0 V ⟶ + 4 V
when DC-regulator is shut off
0 10 20 30 40 50 60 70 ms


Signal connector
Bridging board or system adaptation board connector
Standard board connector
P1
K2
K1
Ch1
Ch8
Ch9
SD
PI
EXT
TL
PR
ERR1
ERR2
TP
S5
S4
S9
S8
CODE HOLES
FEED HOLES
TAPE FEED
TAPE LOW
TAPE ERROR
R80
MAN. FEED
FF-TF
FF-TP
FF-C1
10,5ms
1,85ms
Tt 7µs
C 35
Tt 400µs
C 16
Tt 200µs
C 21
Tt 6µs
C 17
Tt 7ms
C 23
V11
V12
V32
V33
V35
V36
V39
V42
V45
V40
V47
V43
V38
V64
IC1
IC2
IC3
IC4
IC6
IC7
IC9
IC10
D1
D8
D9
D27
D67
D71
D46
D45
D40
D41
D42
D51
D49
D55
PO
R1
R8
R9
R76
R78
R77
R111
R121
R122
R123



Appendix 2 Logical diagram - 4070

DWG NO 98A0792

REVISIONS

SYM	DESCRIPTION	APPROVED	DATE
A	PRODUCTION RELEASE EN [illegible]7	[signature]	3/15/72
B	REVISED PER EN 80715	[illegible]	5/22-72

DR C. Towner	1-24-72	
CHK [signature] JPS270	2/27/72	
DSGN —	—	
ENGR [signature]	1-24-72	
APPD [signature]	3/15/72	
APPD [signature]	3/[illegible]/72	

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2722 michelson drive [illegible] California 92664

TITLE

ENGINEERING DESCRIPTION
PARALLEL 8/16 BIT PAPER TAPE CONTROLLER
MODEL 620-55 or 620-51A

CODE IDENT NO.	SIZE	DWG NO.	REV
21101	A	98A0792	B

SCALE —

SHEET 1 OF 38

96A0153-0006

ENGINEERING DATA FORM

OPTION	8/16 Bit Parallel Controller
MODEL	See Below
NO. OF LOGIC CARDS REQ'D.	1
NO. OF CARD SLOTS REQ'D.	1
LOCATION OF SLOTS (NUMBERING)	Any
CONNECTORS REQ'D. (EXCLUDING I/O)	2
KEYING	None
ST'D. DEVICE ADDRESS	Variable (0 to 77)
WIRELIST NUMBER	None
MANUAL PUBLICATIONS NUMBER	This document
PERIPHERAL EQUIPT. REQ'D	See Below
MFG'R.	
MODEL	
GEN'L. SPECS	

NOTES:

The following paper tape devices may be operated through this controller.

Remex Reader	Model #620-51A
Facit Punch and Remex Reader	Model #620-55

Drawings:

620-51A Assembly Drawing	01P1219
620-55 Assembly Drawing	01P1206
→ Controller Assembly	44P0568
Logic Diagrams	91C0369
Facit Punch Cable Drawing	53B0557
Remex Reader Cable Drawing	53B0602
Facit Punch Procurement Spec.	35A0071
Rack Mount Facit Punch Procurement Spec.	35A0077
Remex Reader Procurement Spec.	35A0082
TEST PROGRAM	92A0107-023

varian data machines
a varian subsidiary
2722 michelson drive
irvine/california/92664

CODE IDENT. NO		98A0792	REV
21101			
PREPARED BY	APPR.	SHT. OF 38	

INDEX

FIGURES

TABLES

SECTION 1
GENERAL DESCRIPTION

1.1 Introduction

The VDM Parallel 8/16 Bit Controller is a special peripheral controller designed to interface between the VDM 620 series computers and a variety of 8 bit input or output peripherals. Data may be transferred in either sense mode or by means of the Buffer Interlace Controller (BIC). In the output mode, 8 or 16 bit data words may be transferred. In the input mode, only 8 bit words may be transferred.

1.2 Functional Description

Ref. Logic Diagrams 9IC0369
620 Computer Manual

1.2.1 Device Address

The device address may be any address from 0 to 77_8. The address is decoded from EB00 through EB05 and signal IUAX-1 (Computer Interrupt Acknowledge). These E-Bus signals are made available on the wire wrap connectors on the back plane. This allows the full device address to be hand wired on the back plane connector. (See para. 3.4).

1.2.2 External Control

The mechanization of the EXC commands is as follows: The device address, EB11+ and Function Ready Pulse (FRYX+) form FUNAD. Lines EB06 through EB08 are applied to a binary to 1 of 8 line decode. The decoded outputs (DEC 0 thru 8) are further decoded by "ANDING" them with FUNAD, thus, forming EXC decodes EXC 0 thru 7.

1.2.3 Extended External Control

Extended external control is developed as in 1.2.2 except EB15+ is the gating term instead of EB11+.

FIGURE 1.1-FUNCTIONAL BLOCK DIAGRAM

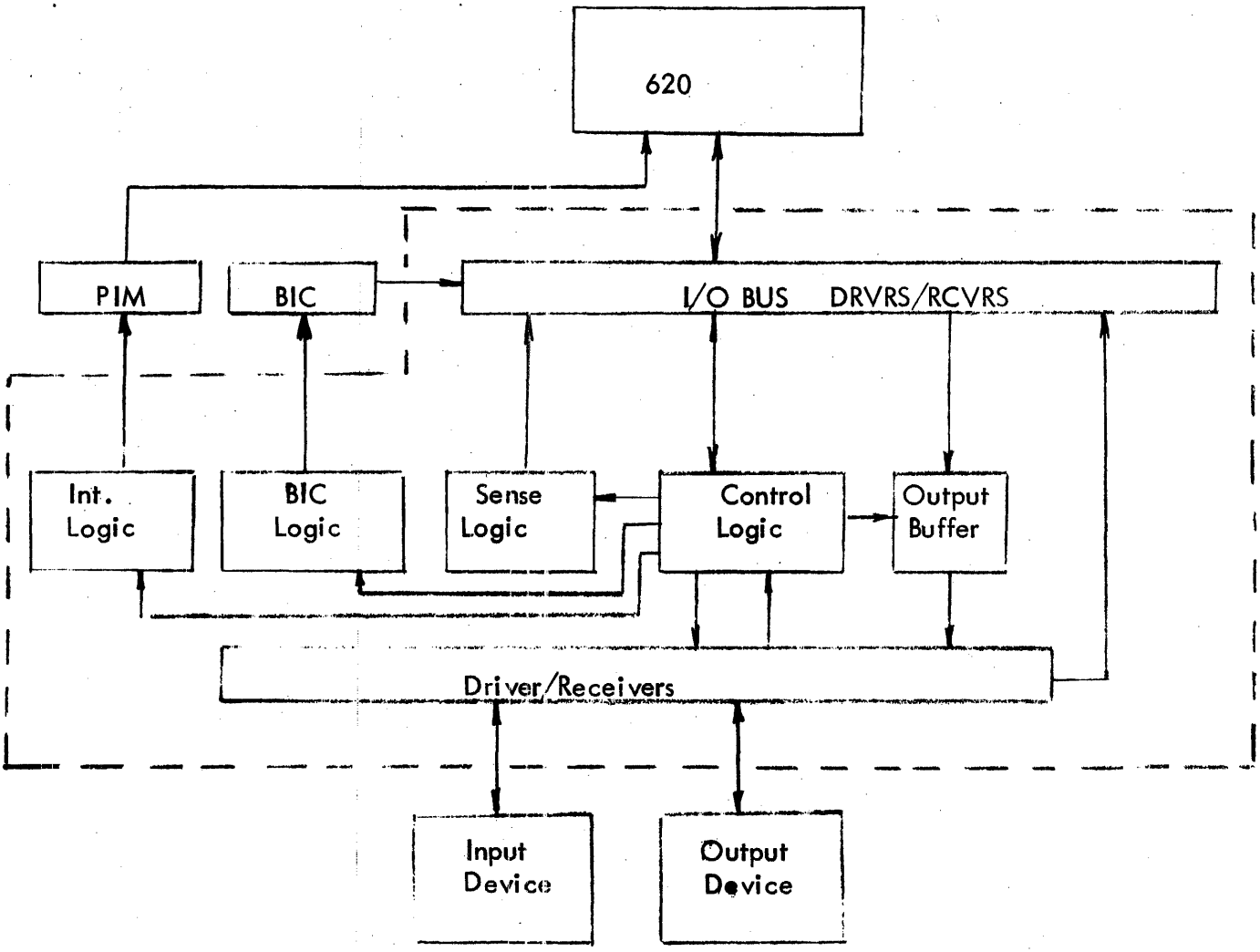
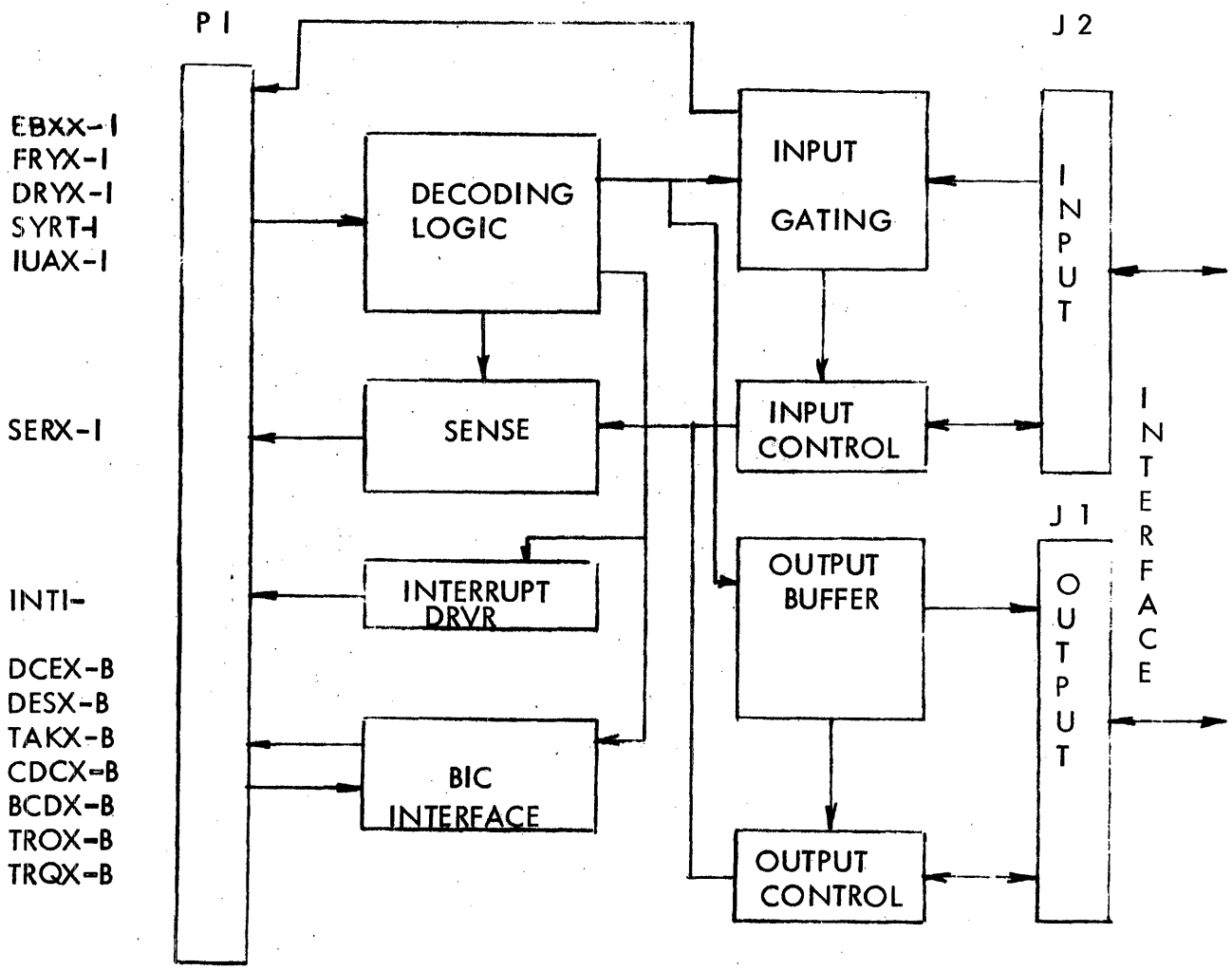


FIGURE 1.2 CONTROLLER BLOCK DIAGRAM



1.2.4 Data Transfer In (See Figure 1-3)

The data transfer in logic controls the transfer of the eight bit word from the peripheral device cable to the input (E) bus. Any of the data transfer in commands (IAR, IBR, IME, CIA, CIB) transfer the input data (DIXX+) to the E-Bus as follows:

The device address and EB13+ enabled flip flop DTIX. The trailing edge of FRYX+ clocks on the flip flop and the trailing edge of DRYX+ resets the flip flop. The output of the flip flop gates the input data onto the E-Bus. DTIX is also buffered and sent to the external device as STEP+. In the case of a Paper Tape Reader, this pulse will cause the tape to move to the next data holes. When this occurs, HRRY (Data Ready) is returned from the peripheral device and sets IRDY flip flop, signaling that next data word is ready.

1.2.5 Data Transfer Out

1.2.5.1 8 Bit Mode (See Figure 1-4)

The data transfer out logic controls the transfer of the data word to the peripheral device. Any of the data transfer out commands (OAR, OBR, OME) loads the output buffer as follows:

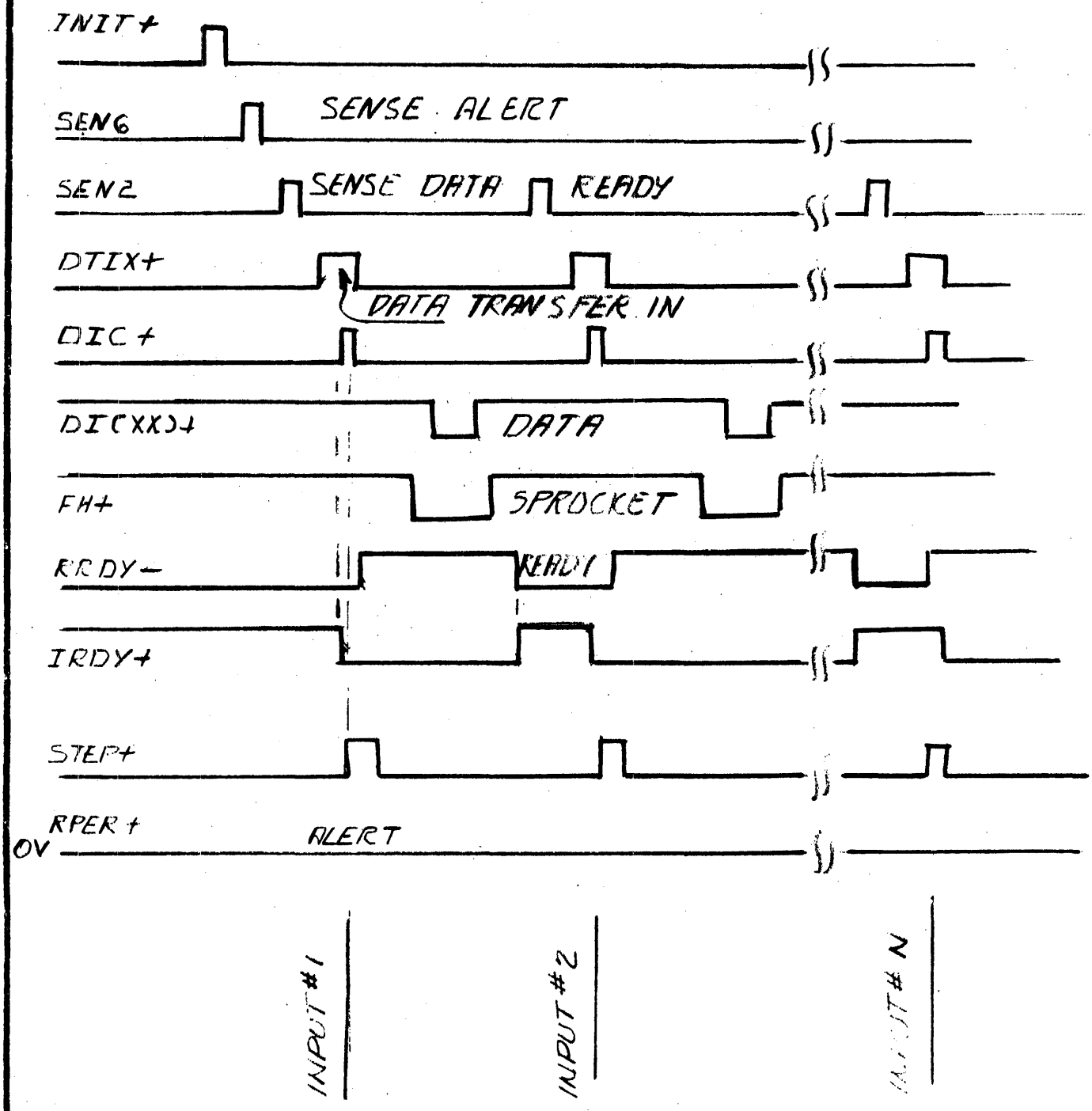
The device address and EB14+ enables the data transfer out flip flop DTOX. The trailing edge of FRYX+ clocks on the flip flop and the trailing edge of DRYX+ clocks off the flip flop.

Data (EB00+thru EB15+) is then clocked into the output buffer (OBXX+) by DOCA+. (Buffered DOC-).

DOC- (DTOX+ DRYX+) is utilized to fire one shot STRB+. This signal is buffered and sent to the peripheral device as DSTRB+, the data strobe. Gating of the least significant data bits to the interface cable is accomplished by the term SHI+ (not 16 bit mode).

The output buffer busy flip flop OBFLD+ is set by the trailing edge of DOC+, and reset by the trailing edge of the peripheral device busy pulse (RWDY-). Sensing of the OBFLD+ synchronizes data transfer with the peripheral device at its maximum rate.

FIGURE 1-3 DATA TRANSFER IN TIMING



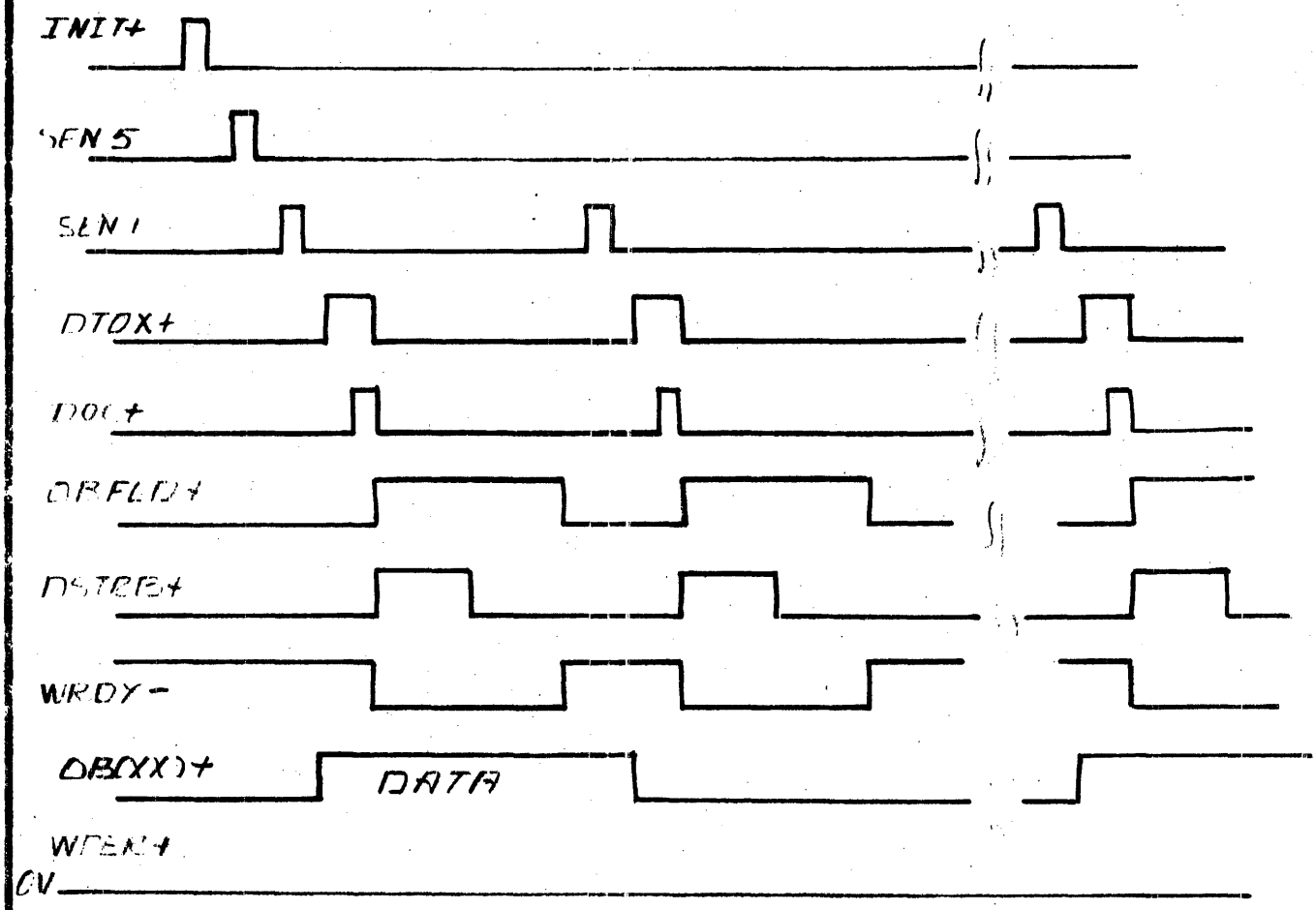


FIGURE 1·4 8 BIT DATA TRANSFER OUT TIMING

1.2.5.2 16 Bit Mode (See Figure 1-5)

Set up of the data transfer out flip flop and loading of the output buffer register is accomplished in the same way as in the 8 bit mode. Additional logic comes into play, however, to steer the two 8 bit bytes to the peripheral device.

EXC 3 is utilized to set the 16 bit mode flip flop. The output of the flip flop enables the clock for the STEER flip flop. The most significant bits (EB08 thru EB15) are transferred to the interface buffers in conjunction with the first byte strobe (DSTRB) developed by DOC+. The reset term (WRDY+) for OBFLD is inhibited by 16 BIT-, thus holding the controller in the busy state. Upon receipt of the trailing edge of the peripheral device busy pulse (LWRY), the STEER flip flop is set, which gates the least significant data bits (EB00 thru EB07+) to the interface buffers and develops the second interface strobe. Upon receipt of the trailing edge of the second peripheral device busy pulse, the steer flip flop is reset which resets the controller busy flip flop OBFLD+. A second 16 bit word may now be transferred to the controller.

1.2.6 Sense Response Logic

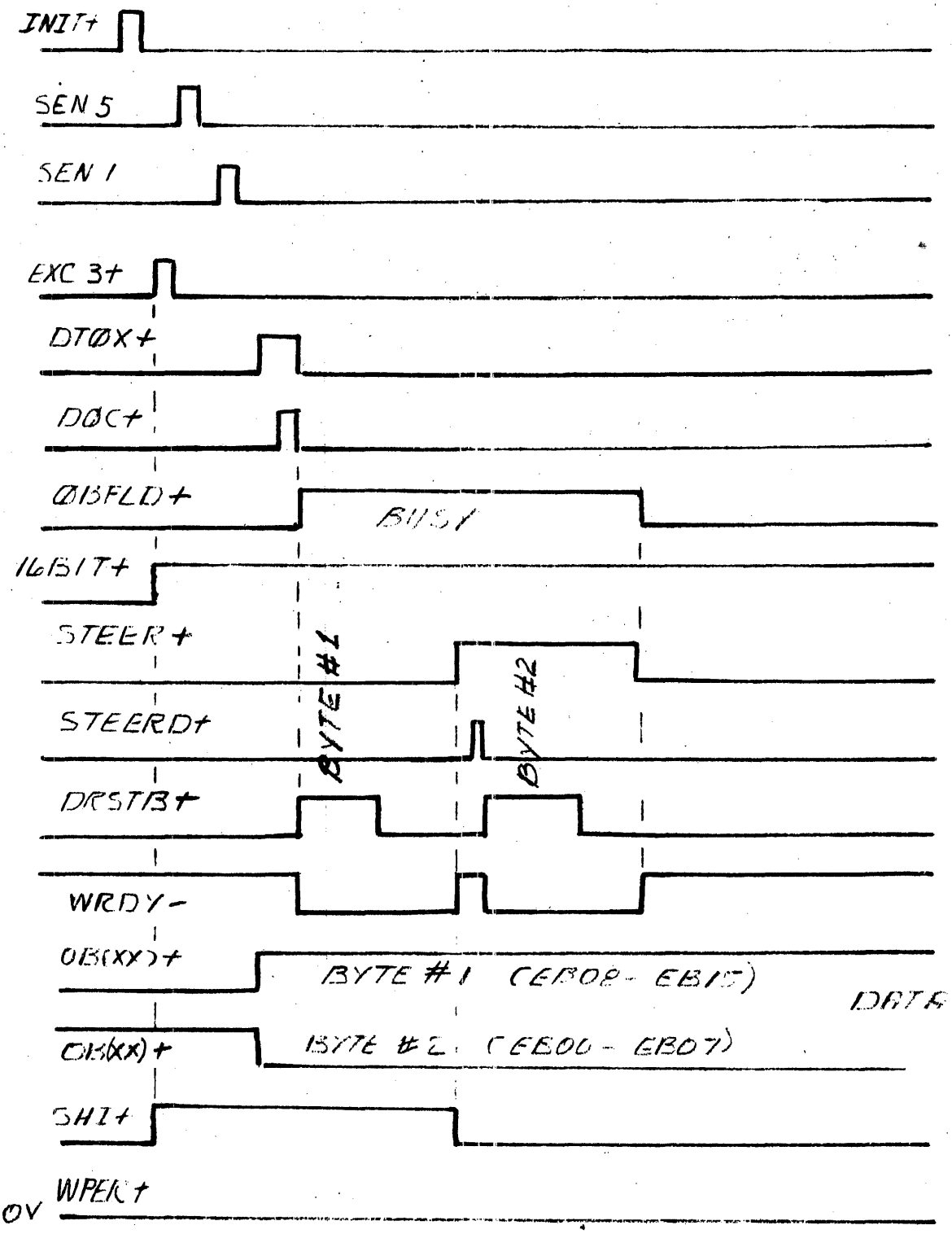
The sense commands check the peripheral device status and are mechanized as follows: Function decodes DEC(XX)+ are applied to individual collector OR'd gates which have as second inputs the various status lines. For example: The write peripheral device alert line, WPER+. In the case of the paper tape punch, if this line is true (high) at sense time, the device is in an alert (malfunction) state. This causes SERX-1, the sense line to the computer, to go true (low) indicating the alert condition.

Because this controller has been designed for more than one specific application, provision has been made within the logic to tie in either high or low active state status lines. If the high active state is used, then a ground jumper within the peripheral cable is required to disable the low active state input. This jumper will be flagged in Table 3.2 (pin assignment) of the pertinent engineering description.

1.2.7 BIC Control Logic

BIC transfer may be made in either input or output mode. Once the BIC is connected to the computer, it sends out DCEX-B which enables the set gate of flip flop CDCX. EXC connect BIC for either input or output will then set CDCX. CDCX-B is returned to the BIC indicating data transfer is now under control of BIC.

FIGURE 1-5 16 BIT DATA TRANSFER OUT TIMING



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			SH 12 OF 38	REV

When the peripheral device is ready (BRDY-) transfer request line TRQX-B is forced true (low). The BIC responds by forcing transfer acknowledge line TAKX-B true)low). The BIC enabled term BOCE-, in the case of an output transfer, goes true and enables data transfer out flip flop DTOX+ which initiates a data transfer out operation. In the case of a data transfer in operation, BICE- goes true and enables DTIX which initiates a data transfer in operation. This sequence of events occurs in synchronization with the peripheral device ready line until the BIC block transfer is complete. A BIC complete (DESX-B) pulse is received by the controller which resets flip flop CDCX.

If, at any time, a peripheral alert is received from the peripheral device during a BIC block transfer, signal BICAL- is pulled true (low). This generates BCDX-B which is returned to the BIC as a stop command. The BIC will then abort the transfer by returning DESX-B.

1.2.8 Interrupts

There are two interrupts available: Write Ready (WINT-) and Read Ready (RINT-). These interrupts are the differentiated trailing edges of OBFLD+ and IRDY+ flip flops, respectively.

1.2.9 Special Logic

1.2.9.1 Sprocket Recognition (Paper Tape Reader Input)

During a Paper Tape input operation, special logic has been incorporated to condition the ready line (RRDY+) so that IRDY+ will not be set if the paper tape reaches the end. (No stop code is present on the tape.) Sprocket pulse FH+ is differentiated. The resulting pulse sets flip flop SPROC+. This level is "ANDed" with RRDY+ and the result is utilized as the IRDY+ flip flop set clock. If no further sprockets pulses appear, RRDY+ is inhibited from setting IRDY.

1.2.9.2 DELETED

1.2.9.3 DELETED

TABLE 1-1 CONTROLLER MNEMONICS

MNEMONIC	DESCRIPTION	SOURCE
ADDR+	Decoded Device Address	
ASCII+	Flip Flop to allow 8 bit ASCII code to be sent to the DP2000 Series Printer.	
BCDX-B	BIC Device Disconnect	
BICAL-	BIC Abort from peripheral device.	
BICE-	BIC Input Enable Line to DTIX Flip Flop	
BOCE-	BIC Output Enable Line to DTOX Flip Flop	
BRDY-	Data Ready to BIC	
CDCX+	BIC Connected Flip Flop	
DA(XX)+	Decoded Device Address ANDed with interrupt acknowledge	
DCEX-B	BIC Device Connect	
DEC(X)-	EB6 through EB8 Decode	
DESX-B	BIC Disconnect	
DI(XX)+	Input Data from peripheral device	
DOC+	Reset term for DTOX Flip Flop	
DOCA+	Strobe for Output Buffer (Buffered DOC+)	
DRYX-I	Data Ready Pulse from CPU	
DSTRB+	Data Strobe to peripheral device	
DTIX+	Data Transfer In Flip Flop	
DTOX+	Data Transfer Out Flip Flop	
DWRDY+	Optional Write Ready Line for use when peripheral device does not supply one.	

TABLE 1-1

MNEMONIC	DESCRIPTION	SOURCE
FB(XX)+	E-Bus Bits 00 thru 15	
EXCB0-	Extended EXC Decode 0	
EXCB1-	Extended EXC Decode 1	
EXC(X)+	EXC Decodes 0 thru 7	
FH+	Sprocket Pulse from Peripheral Device	
FRYX-1	Function Ready Pulse from CPU	
FORMAT+	Format Flip Flop to transfer paper moving information to DP2000 Series Line Printer.	
FUNAD-	Function Command and Device Address	
INIT+	Initialize command.	
IØRDY+	Read or Write Ready	
IRDY+	Read Ready Flip Flop	
IUAX-1	Interrupt Acknowledge Pulse	
NØPCH-	Inhibit OBFLD+ flip flop if no output device connected.	
OBFLD+	Output Buffer Loaded Flip Flop	
OB(XX)+	Output Buffer Data Bits 00 thru 15	
OR(XX)A+	Output Bits 00 thru 15 at Interface Connector	
READ+	Read Mode Flip Flop	
RINT+	Read Ready Interrupt	
RPER+	Read Peripheral Alert	
RRDY+	Read Ready	

TABLE 1-1

MNEMONIC	DESCRIPTION	SOURCE
SERX-I	Sense Line to CPU	
SHI+	Strobe for bits 00 thry 07 to interface connector	
SHI-	Strobe for bits 08 thru 15 to interface connector	
SPROC+	Sprocket flip flop	
STEER+	Steer flip flop steers logic to second output data byte.	
STEP+	Step Pulse to external device to bring in new data.	
SYRT-I	Manual system reset from CPU.	
TAKX-B	BIC Transfer Pulse	
TRØX-B	Transfer Out Pulse	
TRQX-B	Transfer Request Pulse	
WINT-	Write Ready Interrupt	
WPER+	Write Peripheral Alert	
WRDY+	Write Ready Pulse	
ZØNSEL+	Zone Select Flip Flop (Option)	
16 BIT+	16 Bit Mode Flip Flop	

1.3 Controller Specifications

This section contains the principle specifications for the controller.

CHARACTERISTICS	DESCRIPTION
Control Capability	Any peripheral device whose requirements are eight data lines in or out with coincident strobe. The peripheral device must supply two more lines. A peripheral alert line and peripheral ready line. Both an input and an output device may be controlled on a time sharing basis. All lines must be TTL compatible.
I/O Capability	Seven External Control Commands (EXC); two Extended External Control Commands (EXCB), six Sense Commands (SEN), three Data Transfer Out Commands (OAR, OBR, OME), five Data Transfer In Commands (INA, INB, IME, CIA, CIB).
Logic Levels	
Negative Logic	Logic 1 = 0 to 0.5Vdc. Logic 0 = +2.4 to +5.0Vdc.
Positive Logic	Logic 1 = +2.4 to +5.0Vdc Logic 0 = 0 to +0.5Vdc
System Programming	Permits operating the system on an interrupt basis or by programmed sense response loops. BIC capability is also available. In the output mode, The CPU may transfer 8 or 16 bit (two 8 bit bytes) words. In the input mode, only 8 bit words may be transferred.
Size	Packaged on a single circuit card measuring 12.7 inches by 7.7 inches.
Power Requirements	+5 Volts DC @ 1 AMP
Operational Environment	0 to 50°C, 0 to 90°R.H. (without condensation)

1.4 Paper Tape System - General Specifications

1.4.1 Facit Punch Model 4070

Punch speed:	Max 75 rows per second at nominal voltage and frequency
Row spacing:	2.54 mm (0.1")
Tape feed:	Incremental, externally controlled
Feed accuracy:	Complies with ISO standard Adjacent rows, 3% 10 rows, 1% 50 rows, 0.5%
Punch hole configuration:	5-8 track ISO standard 6-track typesetting
Tape widths:	5-track 17.46 ±0.05 mm (.687" ± .002") 6-track 22.23 ±0.05mm (.875" ± .002") 7-track 22.23 ± 0.05mm (.875" ± .002") 8-track 25.4 ±0.05mm (1.000" ± .002")
Tape thickness:	Punch is adjusted for 0.1mm tape on delivery, but can be reset for tapes ranging from 0.08 mm to approximately 0.12mm in thickness.
Type of tape:	Paper, mylar or plastic tape complying with ISO standard
Tape reel hub:	Accepts 51 - 52 mm (2") cores
Outside diameter of tape reel:	Up to 200 mm (8")
Dimensions:	Length 515mm (20.3") Width 205mm (8.1") Height 210mm (8.3")
Weight:	13 kg (29 lbs.)
Mains connection:	Mains voltage shall not be connected up to punch units - control units supply the punch units with voltage

Voltage:	220 V ± 10% single phase 50 Hz ± 2Hz 220 V ± 10% single phase 60Hz ± 2Hz 115 V ± 10% single phase 50 Hz ± 2Hz 115 V ± 10% single phase 60Hz ± 2Hz	Switch Adjustable
Power Consumption:	Approximately 90W	
Control Unit		
Ambient temperature:	0°C - +40°C	
Relative Humidity:	Max 85%	
Dimensions:	Length (incl. connectors) 600 mm (23.6") Width 262 mm (10.3") Height 170 mm (6.7")	

AC INPUT Voltage:	115 V, 127 V, 220 V and 240 V + 15% -10% -1phase AC, grounded mains voltage inlet
AC INPUT Frequency:	50 - 60 Hz ± 2 Hz
Power consumption:	Max 200W with punch motor connected at rated voltage
Voltage outlet for punch:	Grounded outlet for 1-phase AC Voltage, 220 V +15% Current, max 1.1A Frequency, same as mains frequency Output impedance, max 12 ohms
Input logic levels:	
Start pulse	Logical 1, +4V to +25V
Punch motor start	Logical 0, +2 V to -25V
Data signals	Input impedance min 1.5 kohm, max 200 pf

Start pulse:	Start, logical 1 Not start, logical 0 Pulse duration, 0.1 - 3ms Rise time, max 10us
Data signal:	8 parallel lines. A DC voltage or a pulse with a duration of at least 0.1 ms arrives simultaneously with the start pulse. Hole, logical 1 Not hole, logical 0
Output logic levels: Ready signal	Negative logic Punch ready for start pulse and data signals Logical 1, nominal +5 V (can range from +4.3 V to +5.1 V) max 2 mA Punch not ready Logical 0, 0 V to +0.3 V max 20 mA Switching time, max 2us
Register:	The punch register stores one row (8 bits).

Internally programmed functions

Blank tape:	Lever on punch unit can be used to feed out tape punched only with feed hole.
Mark character:	Same lever can be used to feed out tape punched with a special mark character which can comprise any combination of holes specified by the customer. As standard, all-holes tape is punched out.

Connections and controls

The punch unit is connected to the control unit via a signal cable and power cable. The control unit shall be connected to mains having the voltage specified on its nameplate.

ON/OFF power switch:	This control unit switch turns on power throughout the system and lights an indicator lamp in the switch
Line Fuse:	3 A time-delay fuse is used in all control units.
Punch fuse:	0.5 A time-delay fuse. Rack model, 1 A time-delay fuse.

For further information, see the Instruction Book for the Facit 4070.

1.4.2 Remex Reader Model RRX1150BBX/650

Tape Movement	Bidirectional (Manual Operation Only)
Reading Speed	150 characters per second, ±10% in continuous mode and asynchronously at any speed up to 150 characters per second. See Section 5.4.5.
Tapes	Reads standard 8-track (1-inch) tapes with light transmissivity of 57% or less and thickness between 0.0027 and 0.0045 inch (oiled buff paper tape). Options for 6 channel typesetter available.
Input Power	115 VAC (RRX1150BBX/650/S000) or 230 VAC (RRX1150BBX/650/E000), ±10%, 47 to 420 Hz. single phase at 0.6 amp peak (115 VAC) or 0.3 amp (230 VAC). 100 VAC, 47 to 420 Hz option also available.
Temperature	Operating: 0°C to +55°C, free air. Non-operating: -55°C to +85°C.
Weight:	RR-1150BBX: 12 lbs. RRF1150BBX: 13 lbs.
Mounting Dimensions	RR-1150BBX/650: 5-1/4" high, 19" wide, 6" behind 1/4" panel, 2-1/2" in front of panel. RRF1150BBX/650: 7" high, 19" wide, 6" behind 1/4" panel, 2-1/2" in front of panel.
Drive Control (Remex Mode 6)	Stop: +2.4 V +5.0 (2K to +5V) or open circuit Drive: 0 V +0.4 @ 5ma.
Data Output (Remex Mode 5)	Hole: +2.4 V +5.0 @ 0.2 ma (2.2K resistor to +5V dc) No hole: 0 V +0.4 @ 16 ma. (sink) Data envelops sprocket by at least 100 usec on both rising and falling edges.
Slew Mode Operation	250 cps nominally

SECTION 2
PROGRAMMING

2.1 PAPER TAPE SYSTEM PROGRAMMING REQUIREMENTS

The paper tape system may be programmed in a multi-peripheral environment by the external interrupt structure or individually selected by programmed response loops. Four EXC instructions control the operations with data transfers and sense interrogations affected by standard 620 programming methods. BIC capability is also available.

2.2 Description of Commands

There are a total of seventeen instructions reserved for use with the paper tape system. These include four external functions, eight transfers, and five sense. The reserved instructions are listed and described in the paragraphs that follow. It is assumed here that the paper tape system is assigned to device address 37.

2.2.1 External Control

EXC (N=0 or 1)	100N37	Write Connect (BIC)
EXC 3	100337	16 Bit Output Mode
EXC 4	100437	Initialize Controller
EXC (N=2 or 5)	100N37	Read Connect (BIC)

2.2.2 Sense

SEN 1	101137	Write Ready
SEN 2	101237	Read Ready
SEN 5	101537	Read and Write Ready
SEN 6	101637	Write Peripheral Alert
SEN 7	101737	Read Peripheral Alert

2.2.3 Data Transfer Out

OAR	103137	Output A Register
OBR	103237	Output B Register
OME	103037	Output from Memory

2.2.4 Data Transfer In

INA	102137	Input to A Register
INB	102237	Input to B Register
IME	102037	Input to Memory
CIA	102537	Clear and Input to A Register
CIB	102637	Clear and Input to B Register

2.3 Instruction Set Description

2.3.1 External Control Commands

BIC Write Connect (EXC 0 or 1)

This command connects the controller to a 620 BIC for output of data to the paper tape punch under DMA control. It should be issued after the BIC is initialized and loaded with the parameters of the DMA Transfer. DMA operation requires a BIC option.

BIC Read Connect (EXC 2 or 5)

This command connects the controller to a 620 BIC for input of data from the paper tape reader under DMA control. It should be issued after the BIC is initialized and loaded with the parameters of the DMA Transfer.

16 Bit Output Mode (EXC 3)

In the 16 bit mode, a 16 bit (2 bytes) data word may be sent to the controller. The controller will transmit this data to the punch in two 8 bit bytes. The first byte will correspond to CPU bits 08 through 15 and the second byte CPU bits 00 through 07. (See Figure 2-1.) The controller will hang up in a busy state during the full two byte transfer to the punch.

Initialize (EXC 4)

This command initializes the controller to the following state:

Write Ready
BIC disconnected
Eight Bit Mode

2.3.2 Sense Commands

Write Ready (SEN 1)

This instruction is answered affirmative when the paper tape punch is ready to accept a data character.

Read Ready (SEN 2)

This instruction is answered affirmative when the paper tape reader is available and a previous sprocket hole has been recognized.

Read/Write Ready (SEN 5)

This instruction is answered in the affirmative when the punch is ready to accept data and reader data is available.

Write Peripheral Alert (SEN 6)

This instruction is answered in the affirmative when there is a punch alert for the following conditions:

Punch Power not on
No paper tape

Read Peripheral Alert (SEN 7)

This instruction is answered in the affirmative when there is a reader alert for the following conditions:

Reader Power not on
Run load switch in load position

2.3.3 Data Transfer Out Commands

Any of the data transfer out commands (OAR, OBR, OME) loads the 16 bit output buffer register with E-Bus bits 00 through 15. If the controller is in the 8 bit mode (initialize), only E-Bus bits 00 through 07 will be transferred to the punch. If EXC 9 (16 bit mode) has been previously executed, then two bytes will be transferred to the punch. E-Bus bits 08 through 15 will be the first byte and E-Bus bits 00 through 07 will be the second byte.

2.3.4 Data Transfer In

Any of the data transfer in commands (INA, INB, IME, CIA, CIB) will input an 8 bit data word to the CPU E-Bus. See Figure 2.2 for data E-Bus relationships.

2.3.5 Interrupts

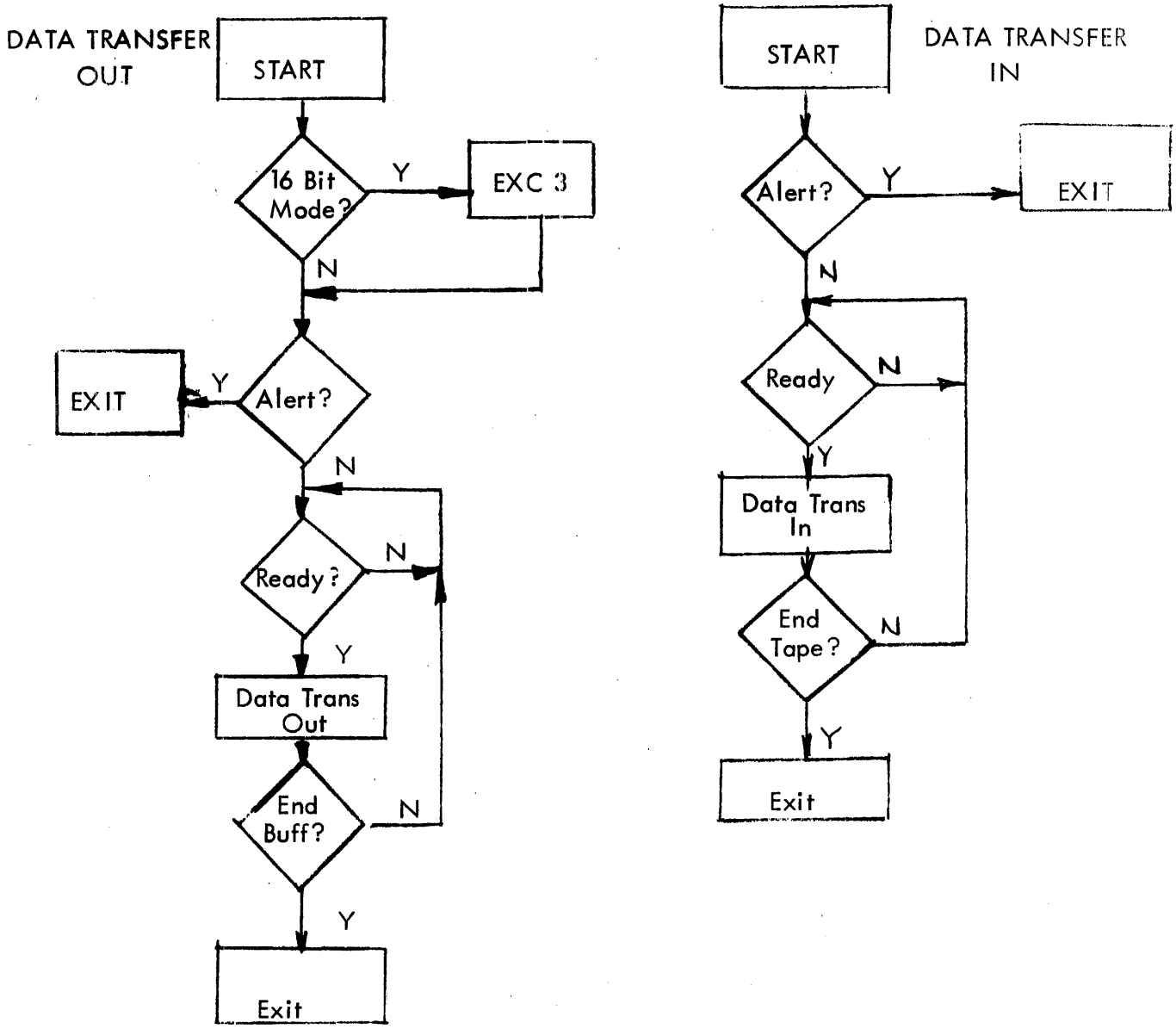
There are two interrupts available: Write Ready and Read Ready. These interrupts correspond to SENS 1 and SENS 2 respectively.

2.4. Typical Operations and Programs

Flow diagrams of typical operating sequences for reading tapes under programmed sense control are illustrated in figure 2.1.

FIGURE 2.1

DATA FLOW



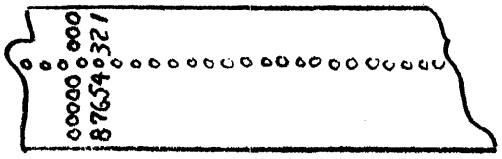
2.5 Data Format

The E-Bus to input or output bits relationship is shown in Figure 2A.2.

Figure 2A-2 - E-Bus to Data Relationship

Input or Output 8 Bit Mode

7	6	5	4	3	2	1	0	E-Bus
8	7	6	5	4	3	2	1	Hole



Output 16 Bit Mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	E-BUS
8	7	6	5	4	3	2	1	8	7	6	5	4	3	2	1	HOLE

First Byte Second Byte

2.6 Models Applicable Punch and/or Reader

The following paper tape models can be operated using this controller.

620-51A Paper Tape Reader (150 cps)

620-55 Paper Tape Reader (150 cps) Paper Tape Punch (75 cps)

The paper tape reader is defined in procurement specification 35A0082 and is the Remex 150 cps Reader Model RR(X)-150BBX/650.

The paper tape punch is defined in procurement specification 35A0071 OR 35A0077 and is the 75 cps model 4070.

SECTION 3
INSTALLATION

3.1 General

Installation of the Paper Tape System in the field is normally accomplished by Varian Data Machines Customer Service Engineers. Logic diagrams, assembly layout, and Eng. Description are provided at the time of purchase. The following installation data is provided for planning purposes.

3.2 Pre-Installation Requirements

Prior to the installation of the system, proper operation of the computer should be assured through use of the diagnostic test routines described in the 620 Maintenance Manual. An Expansion/Peripheral Controller Chassis must be installed in close proximity to the computer. The chassis is connected to the I/O bus by means of the I/O cable. The I/O BUS IS TERMINATED AT THE LAST EXPANSION CHASSIS

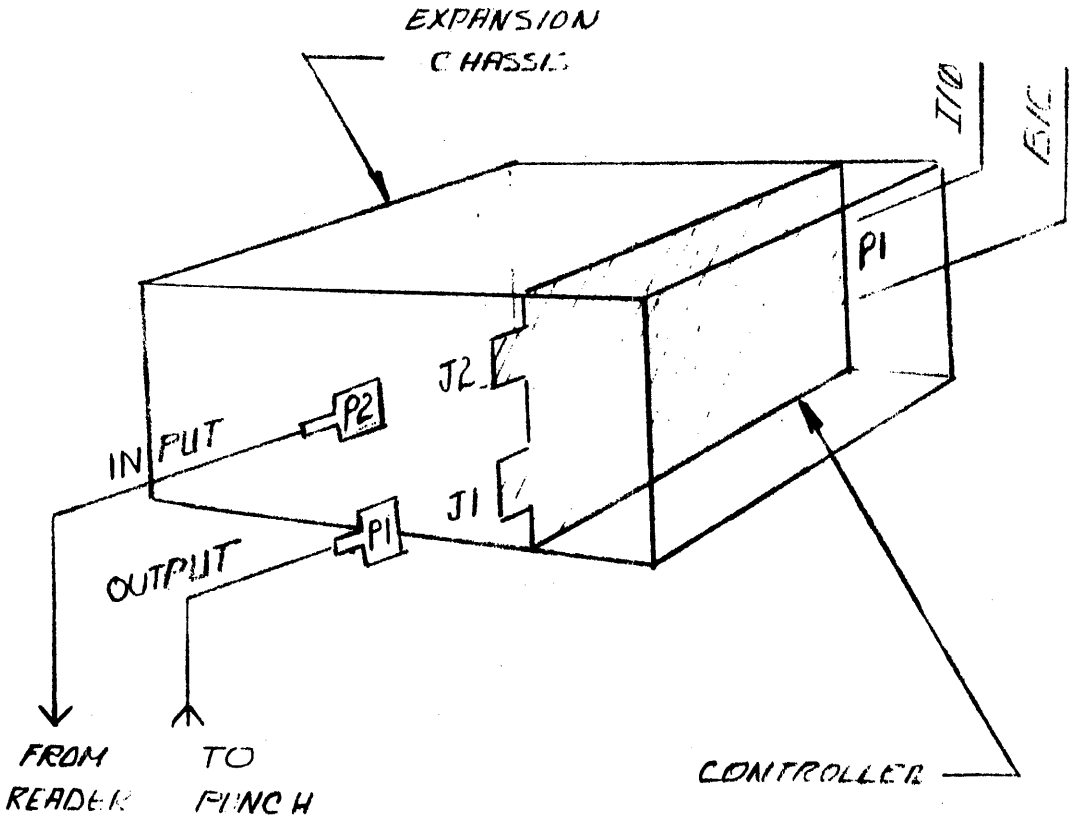


FIGURE 3-1 TYPICAL INSTALLATION

3.3 Wiring Requirements

3.3.1 Controller Back Plane Wiring

The controller requires one card slot space. It uses the standard back plane I/O bus and power wiring used with the expansion chassis (See table 3-1).

3.3.2 Peripheral Device Cabling

There is one cable connecting each peripheral device to the controller. The output cable is connected to controller edge connector J1 and the input cable is connected to controller edge connector J2. Pin assignments are shown in Table 3.2 and Table 3.3, respectively. See Figure 3-1 for typical installation.

TABLE 3-1 Controller Card, P1 Pin Assignments

PIN	MNEMONICS	PIN	MNEMONICS
1	GND	64	EB00+
2	EB00-I	65	EB00-
4	EB01-I	66	EB0I+
6	EB02-I	67	EB01+
8	EB03-I	68	EB01-
10	EB04-I	69	EB1I+
11	EB05-I	70	EB02+
12	EB06-I	71	EB02-
13	EB07-I	72	EB2I+
14	EB08-I	76	EB3I+
15	EB09-I	77	EB4I+
16	EB10-I	78	EB5I+
17	EB11-I	82	EB03+
18	EB12-I	83	EB03-
19	EB13-I	84	EB04+
20	EB14-I	85	EB04-
21	EB15-I	86	EB05-
27	FRYX-I	87	EB05+
29	DRYX-I	90	RINT-
31	SERX-I	96	WINT-
43	SYRT-I	100	GND
44	IUAX-I	118	+5V
48	GND	122	GND
49	TRQX-B		
50	TRØX-B		
52	BCDX-B		
54	CDCX-B		
56	DCEX-B		
58	TAKX-B		
60	DESX-B		

Table 3-2 J1 Pin Assignments

PIN	MNEMONIC	DESCRIPTION	SOURCE
1	DSTRB+	Strobe	Controller
2	Ret		
5	OR03+		
6	Ret		
7	OR02+		
8	Ret		
9	OR01+	Data	Controller
10	Ret		
11	OR00+		
12	Ret		
13	OR07+		
14	Ret		
15	OR06+		
16	Ret		
17	OR04+		
18	Ret		
19	OR05+		
20	Ret		
21	HWRY+	Ready	Device
22	Ret		
23	LWRY-	~~Ready~~	Device
24	Ret		
25	HWPER-	~~Alert~~	Device
26	Ret		
27	DSTRB-	~~Strobe~~	Controller
28	Ret		
29	LWPER+ *	Alert	Device
30	Ret		
32	NO PCH-	Device connected	Controller

* This line is grounded within the cable (Ref. Paragraph 1.2.6).

TABLE 3-3 J2 Pin Assignments

PIN	MNEMONIC	DESCRIPTION	SOURCE
1	Ret		
2	D100+		
3	Ret		
4	D103+	Data	Device
5	Ret		
6	D102+		
7	Ret		
8	D101+		
9	Ret		
10	STEP+	Send Data	Controller
11	Ret		
12	LRRY+	Data Ready	
13	Ret		
14	HRRY-	~~Data Ready~~	Device
15	Ret		
16	HRPER-	$\overline{\text{Alert}}$	Device
17	Ret		
18	FH+	Sprocket Pulse	Device
19	Ret		
20	STEP-	~~Send Data~~	Controller
22	LRPER+	Alert	Device
23	Ret		
35	D105+		
36	Ret		
37	D106+	Data	Device
38	Ret		
39	D104+		
40	Ret		
41	D107+		

3.4 Device Address

Any address from 0 to 77 may be wired in on the back plane. Table 3-4 lists the true and complement inputs and outputs of the I/O bus address bits. Table 3-5 lists wiring connections required for the least significant portion of the device address and Table 2-6 lists wiring connections required for the most significant portion of the device address. Device address of first paper tape system is normally 37_8.

TABLE 3-4 Device Address Input and Output Pins

TERM	PIN (P1)	TERM	PIN (P1)
EB00+	64	EB03+	82
EB00-	65	EB03-	83
EB0I+	66	EB3I+	76
EB01+	67	EB04+	84
EB01-	68	EB04-	85
EB1I+	69	EB4I+	77
EB02+	70	EB05+	86
EB02-	71	EB05-	87
EB2I+	72	EB5I+	78

TABLE 3-5 Device Address Jumpers (least significant address)

DEVICE ADDRESS	JUMPER PINS	DEVICE ADDRESS	JUMPER PINS
X0	65 to 66 68 to 69 71 to 72	X4	65 to 66 68 to 69 70 to 72
X1	64 to 66 68 to 69 71 to 72	X5	64 to 66 68 to 69 70 to 72
X2	65 to 66 67 to 69 71 to 72	X6	65 to 66 67 to 69 70 to 72
X3	64 to 68 67 to 69 71 to 72	X7	64 to 66 67 to 69 70 to 72

TABLE 3.6 Device Address Jumpers (most significant address)

DEVICE ADDRESS	JUMPER PINS	DEVICE ADDRESS	JUMPER PINS
0X	83 to 76 85 to 77 87 to 78	4X	83 to 76 85 to 77 86 to 78
1X	82 to 76 85 to 77 87 to 78	5X	82 to 76 85 to 77 86 to 78
2X	83 to 76 84 to 77 87 to 78	6X	83 to 76 84 to 77 86 to 78
3X	82 to 76 84 to 77 87 to 78	7X	82 to 76 84 to 77 86 to 78

3.5 Peripheral Device Installation and Operation

3.5.1 General

A complete description and operating instructions will be found in the peripheral device maintenance and operation manual that is delivered with the system.

SECTION 4
MAINTENANCE

4.1 General

This section defines the appropriate equipment, diagnostic routines, and required tests to insure the controller's proper performance. Maintenance requirements for the peripheral device are called out in the appropriate peripheral device instruction manual.

4.2 Maintenance of the Controller

The following are standard hardware and software devices for checkout. Addition and/or deletion of these devices may be made in the future, if necessary.

4.2.1 Test Equipment

The Tektronix 545 Oscilloscope or one of similar performance specification is required.

4.2.2 Tools

A standard extender board allows for easy access to the controller during test.

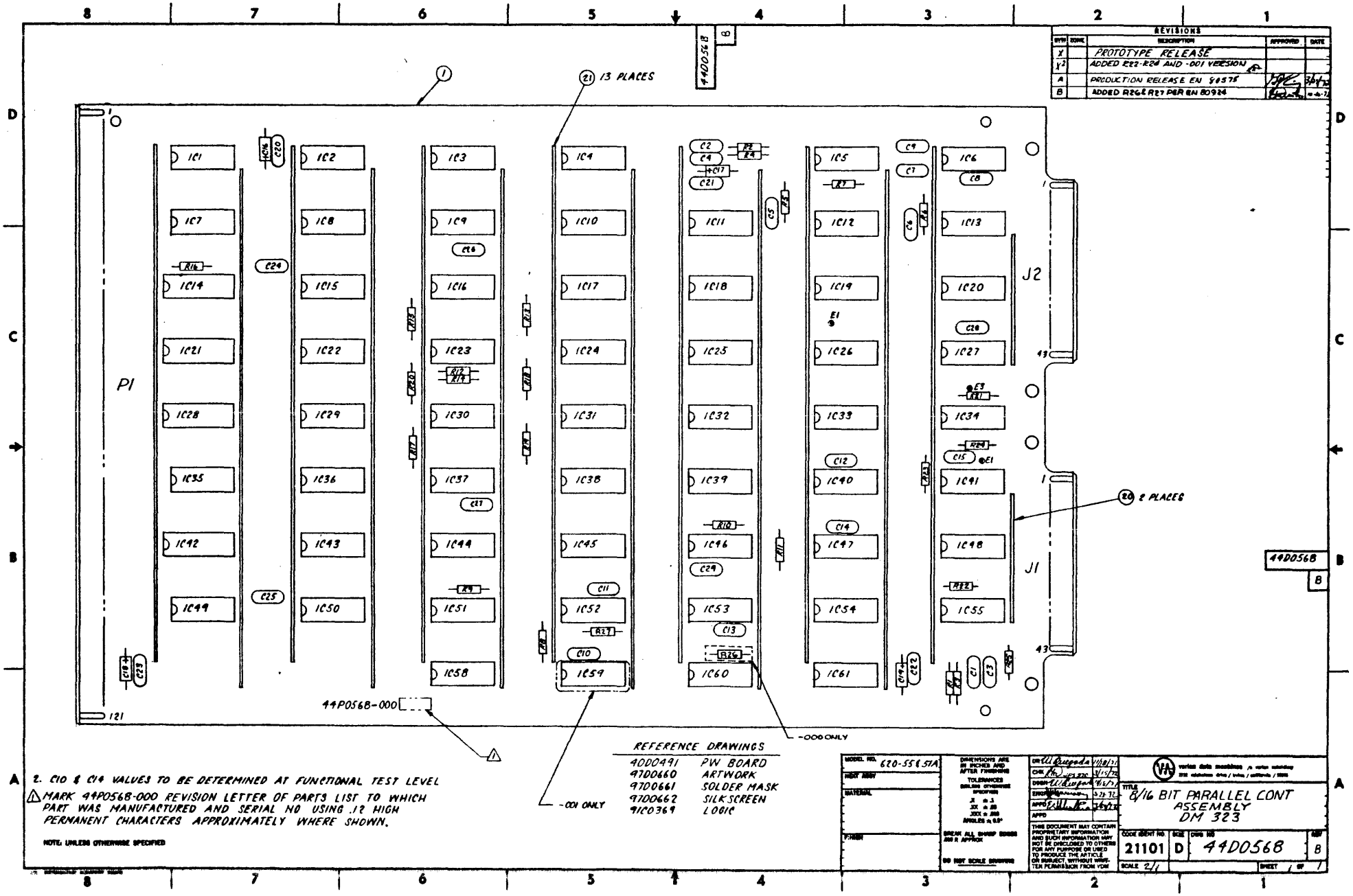
4.2.3 Software (Diagnostic)

Test utilized for diagnosis and trouble shooting of the controller and peripheral devices are as follows:

TEST PROGRAM 92A0107-023

4.3 Maintenance of the Peripheral Device

Maintenance procedures are completely defined in the peripheral device maintenance manual.



2. C10 & C14 VALUES TO BE DETERMINED AT FUNCTIONAL TEST LEVEL

⚠ MARK 44P056B-000 REVISION LETTER OF PARTS LIST TO WHICH PART WAS MANUFACTURED AND SERIAL NO USING .12 HIGH PERMANENT CHARACTERS APPROXIMATELY WHERE SHOWN.

NOTE: UNLESS OTHERWISE SPECIFIED

REFERENCE DRAWINGS

4000491	PW BOARD
9700660	ARTWORK
9700661	SOLDER MASK
9700662	SILKSCREEN
9100369	LOGIC

MODEL NO. 620-55&STA
NEXT ASSY
MATERIAL
FINISH

DIMENSIONS ARE IN INCHES AND AFTER FINISHING
TOLERANCES UNLESS OTHERWISE SPECIFIED
X ± .1
XX ± .05
XXX ± .010
ANGLES ± 0.5°
BREAK ALL SHARP EDGES .005 R APPROX
DO NOT SCALE DRAWING

DR W. Rugeda 1/18/72
CHK [illegible] 3/15/72
DESIGN W. Rugeda 4/5/72
ENGR [illegible] 3/24/72
APPD [illegible] 3/24/72
APPD

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TITLE 8/16 BIT PARALLEL CONT ASSEMBLY DM 323

CODE IDENT NO. 21101 | SIZE D | DWG NO. 44D056B | REV B

SCALE 2/1 SHEET 1 OF 1

NOTES: (UNLESS OTHERWISE SPECIFIED)

REVISIONS					
CODE	SYM	ZONE		APPROVED	DATE
--	A		PRODUCTION RELEASE EN 80575		8/24/72
--	B		RESISTOR VALUE NOTE WAS 570 OHMS 1259 NOTE WAS -002 ONLY EN. 80715		9/22/72
--	C	CW	ADDED RES. R26 & R27 AND REVISED PER EN 80924		10.16.72
--	D	CW	REVISED PER EN 81033		10.16.72
--	E	CW	REVISED PER EN 81088		10.16.72
--	-	B	REVISED CONN. P1, PIN 95 & 96 ON SHT 9 PER EN 83209		1/10/74

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
1C61	
R27	
C29	

REFERENCE DRAWINGS	
44D0568	ASSEMBLY
44P0568	PARTS LIST
97D0660	ARTWORK
97D0662	SILKSCREEN
97D0661	SOLDERMASK
90D0491	P.W. BOARD

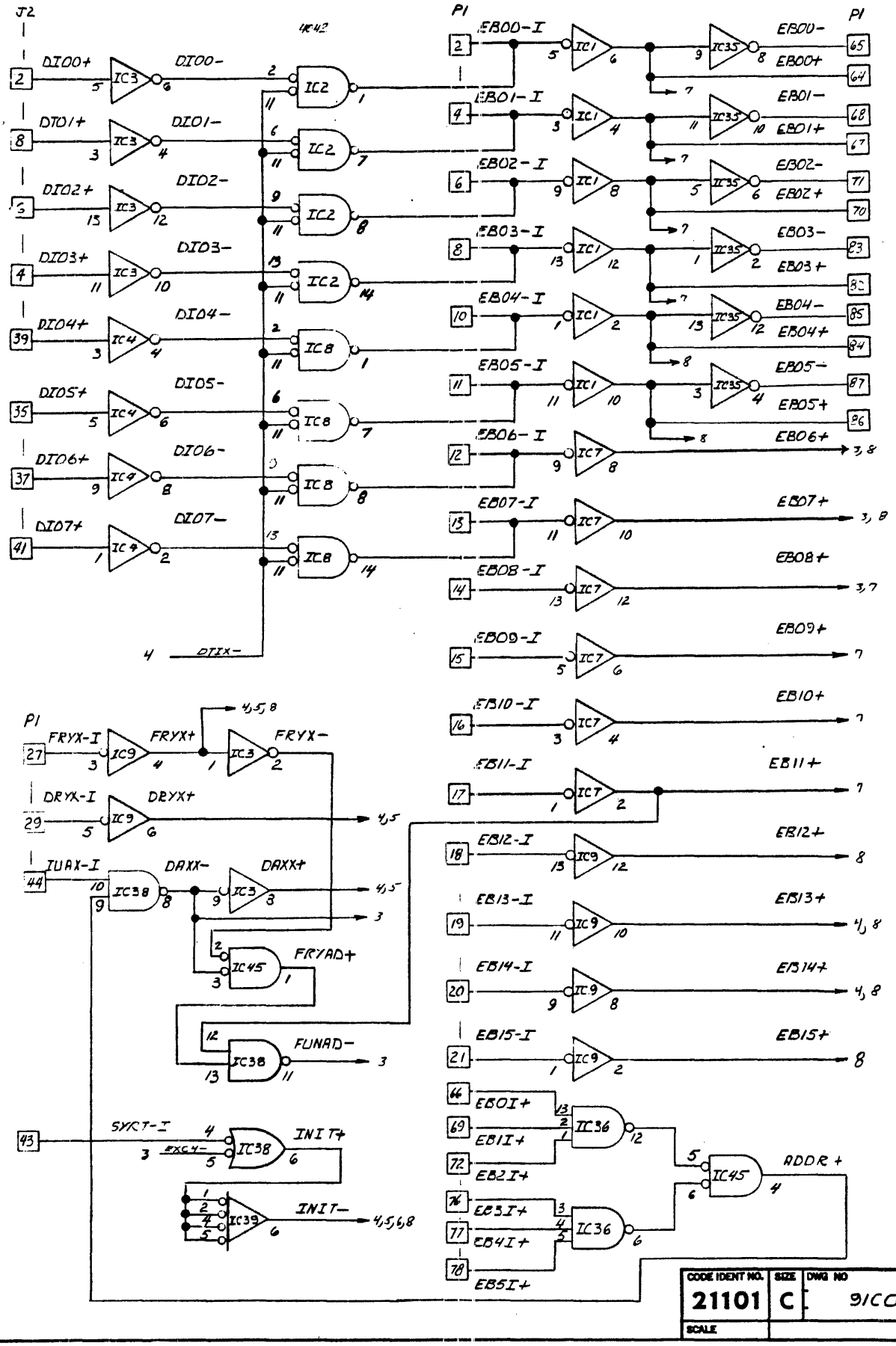
DR	—	—
CHK	[illegible]	3/19/72
DSGN	—	—
ENGR	[illegible]	11-24-71
APPD	[illegible]	8/24/72
APPD		

THIS DOCUMENT MAY CONTAIN PROPRIETARY INFORMATION AND SUCH INFORMATION MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE OR USED TO PRODUCE THE ARTICLE OR SUBJECT, WITHOUT WRITTEN PERMISSION FROM VDM

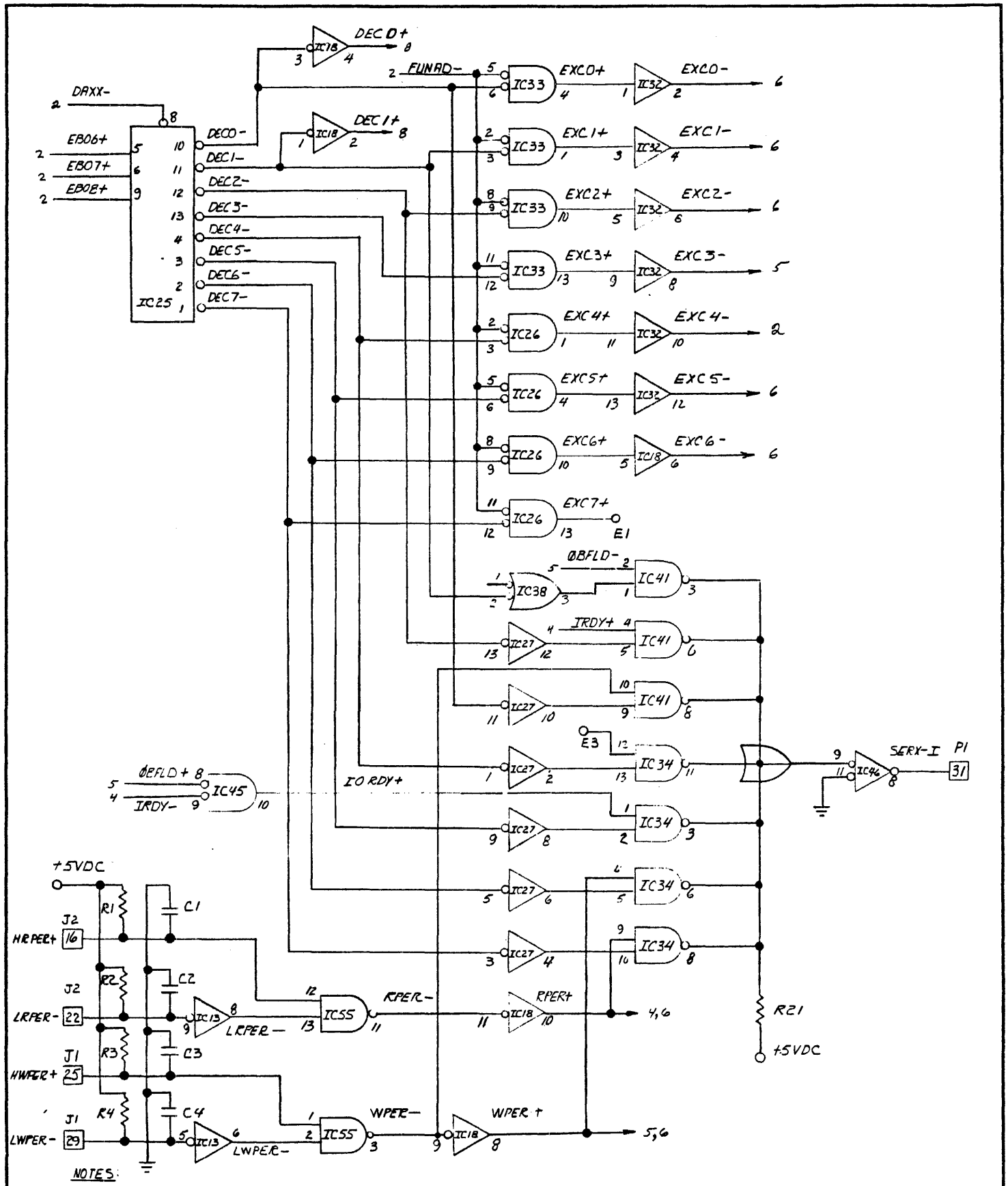
varian data machines /a varian subsidiary
2722 michelson drive / irvine / california / 92664

TITLE LOGIC DIAGRAMS
8/16 BIT PARALLEL CONTROLLER

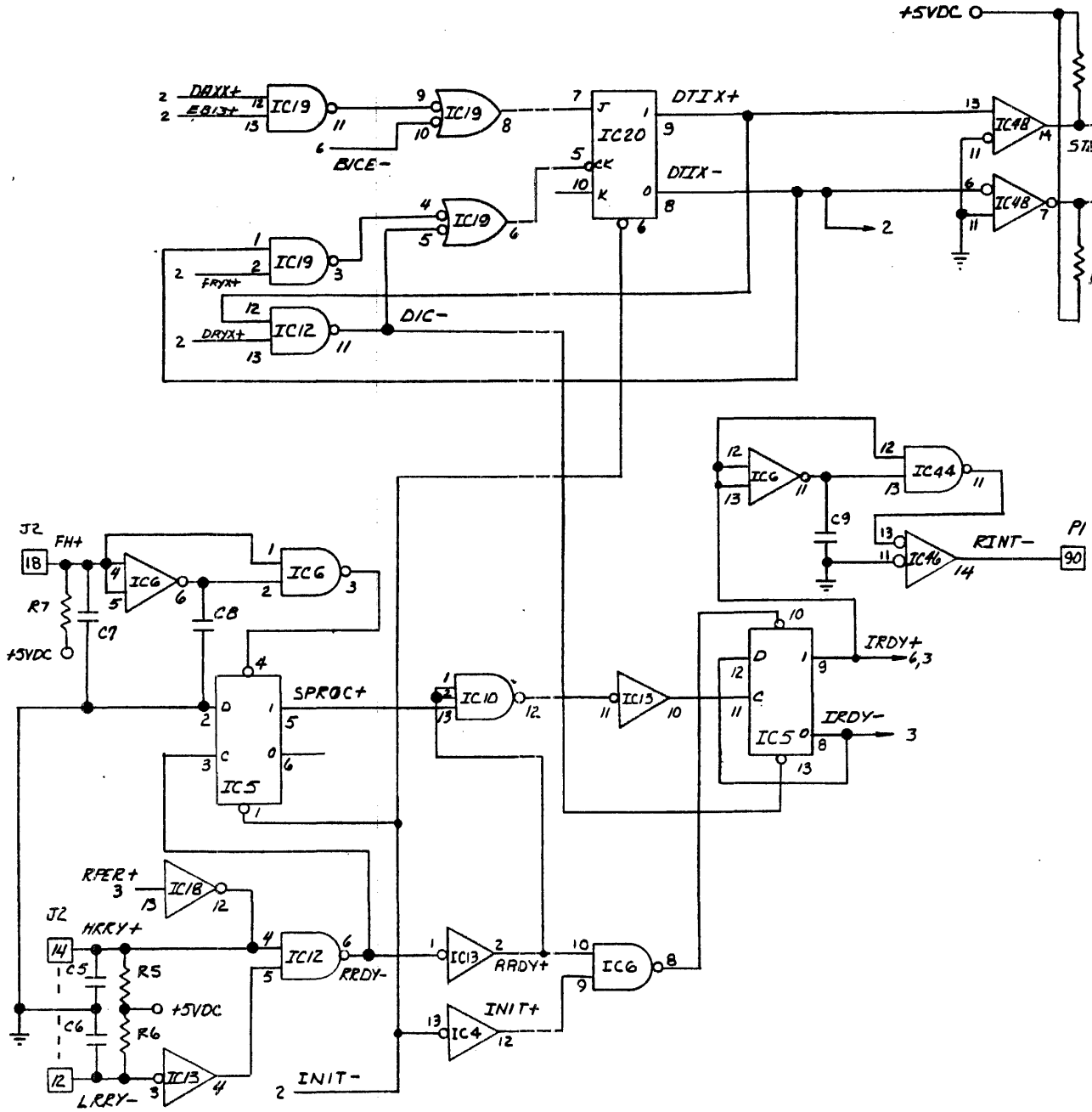
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0369	E
SCALE —	620-51A, 620-55	SHEET 1 OF 9	



CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0369	E
SCALE		SHEET 2 OF 9	



CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0369	E
SCALE		SHEET 3 OF 9	



NOTES

UNLESS OTHERWISE SPECIFIED ALL

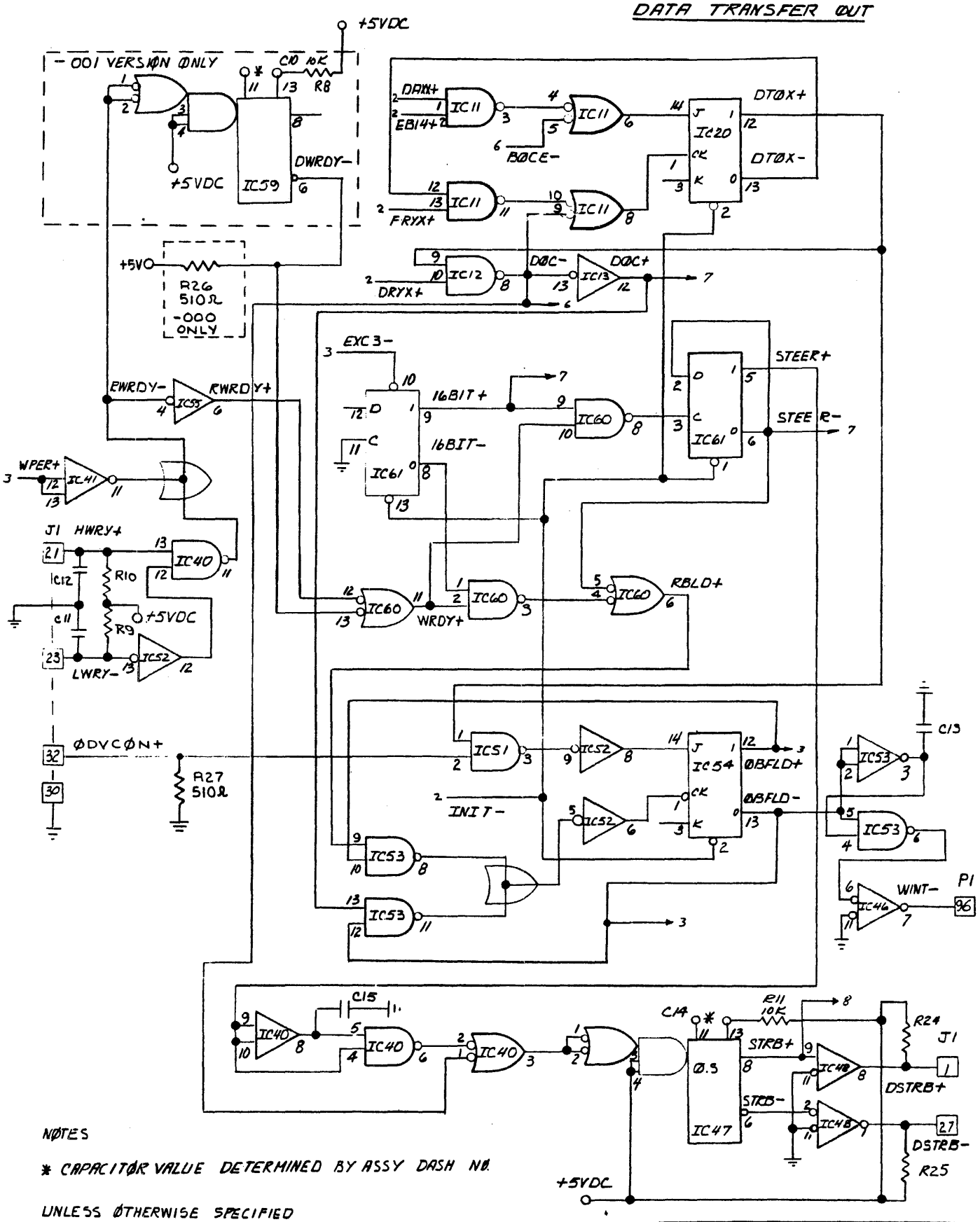
RESISTORS ARE 510 OHM 1/4 W

CAPACITORS ARE 680pf

DATA TRANSFER IN

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0369	E
SCALE		SHEET 4 OF 9	

DATA TRANSFER OUT



NØTES

* CAPACITØR VALUE DETERMINED BY ASSY DASH NØ.

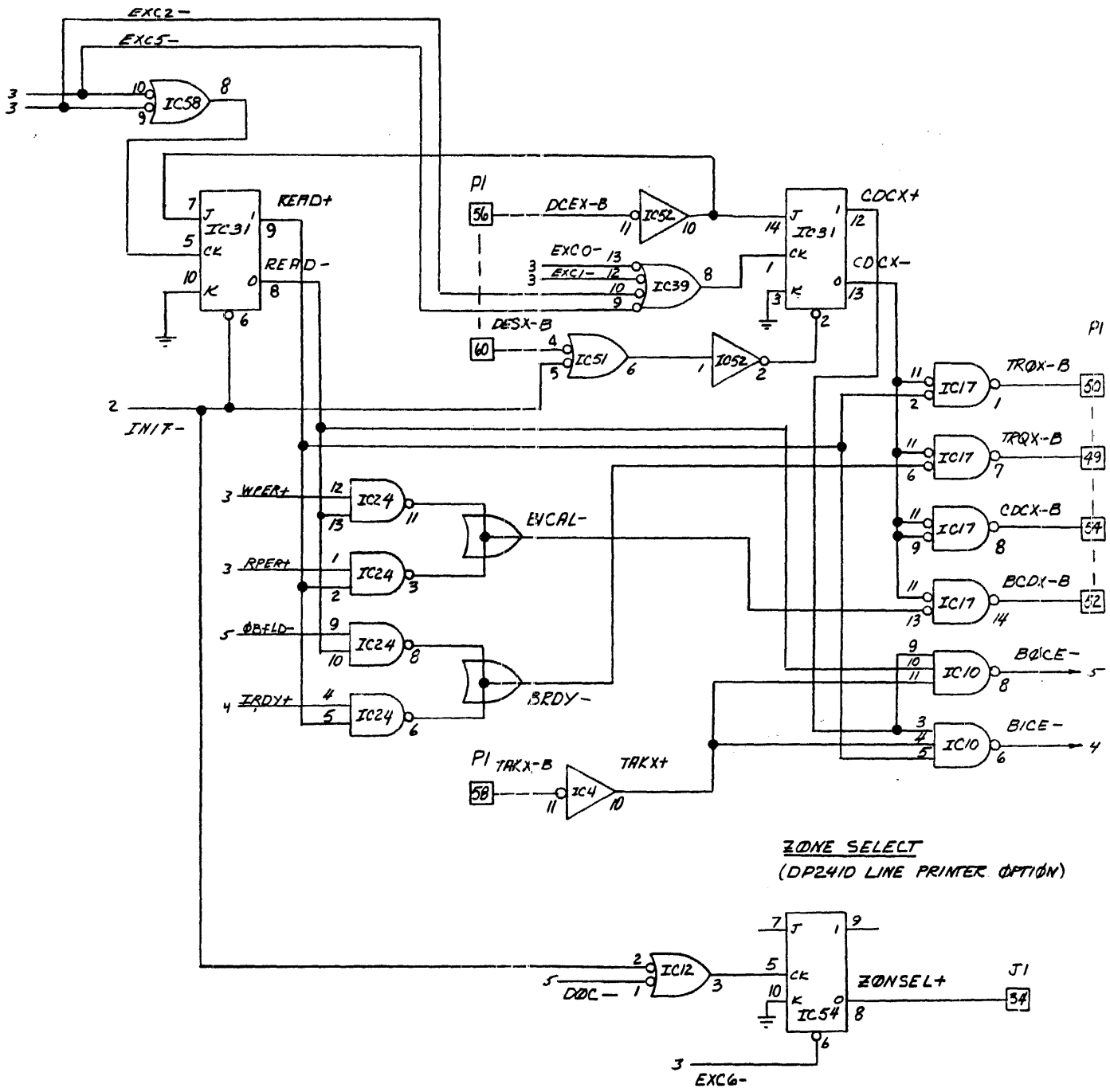
UNLESS ØTHERWISE SPECIFIED

CAPACITØR VALUES ARE 680 pf

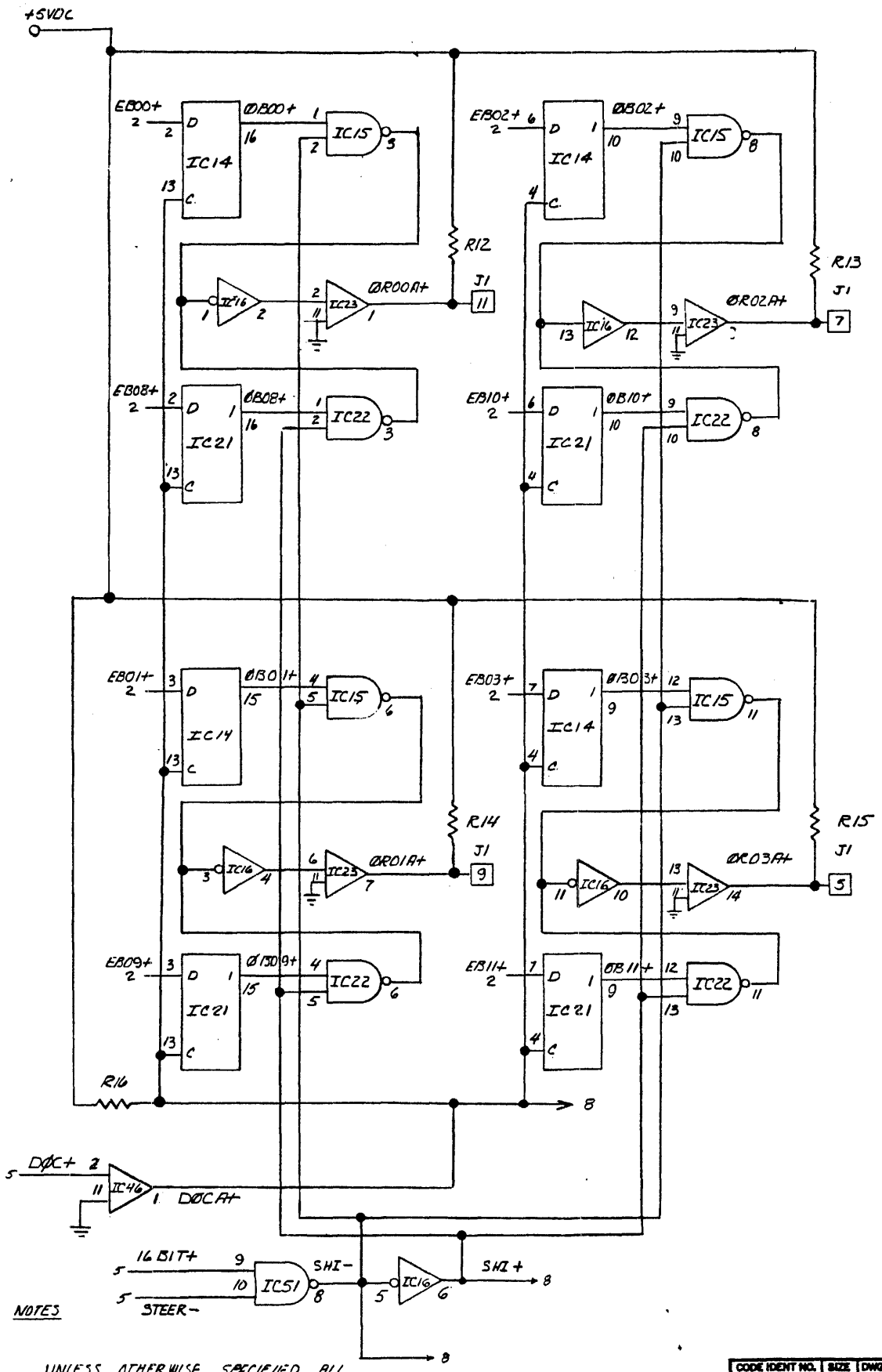
RESISTØR VALUES ARE 510 OHM 1/4 W

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0369	E
SCALE		SHEET 5 OF 9	

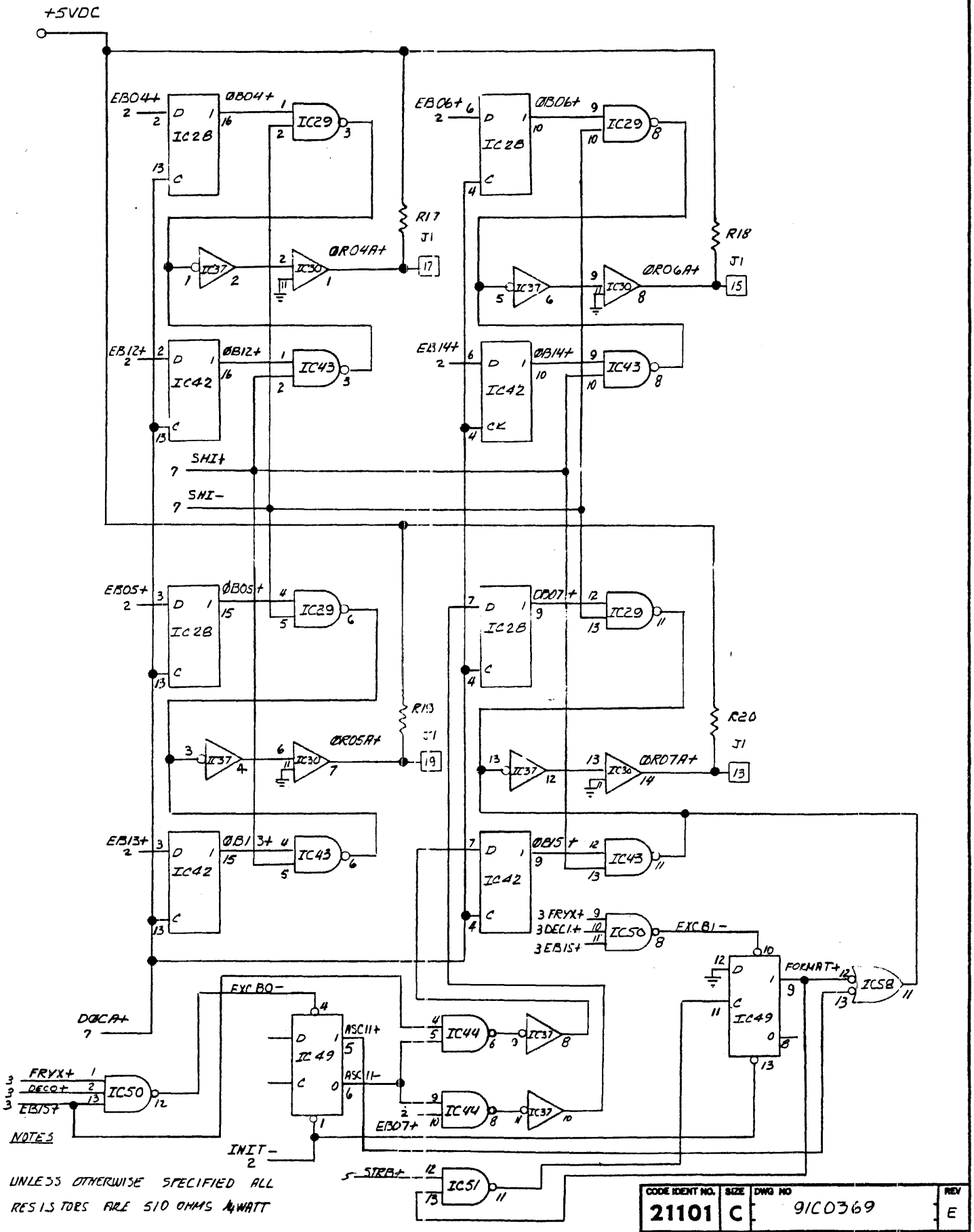
BIC CONTROL



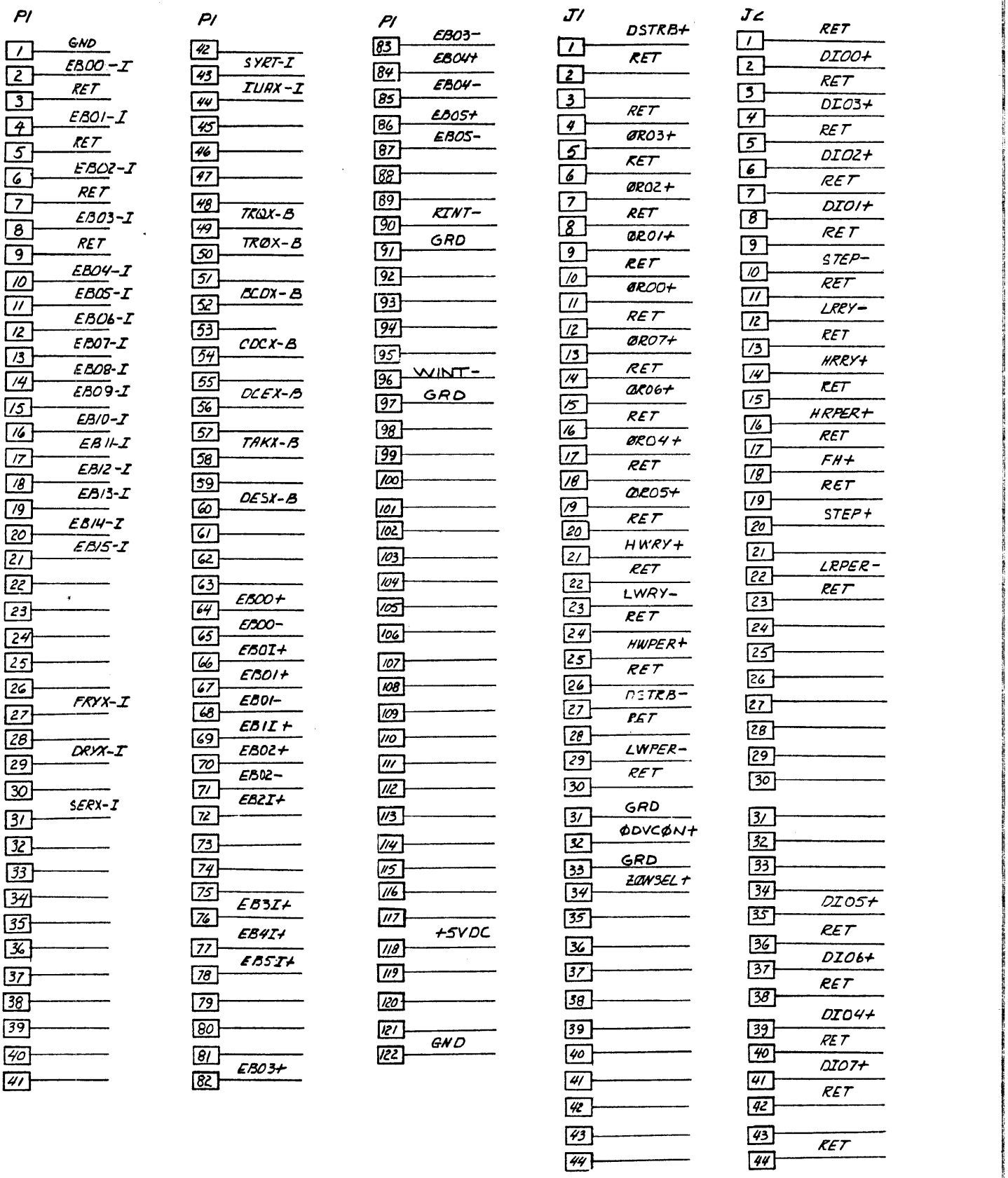
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0369	E
SCALE		SHEET 6 OF 9	



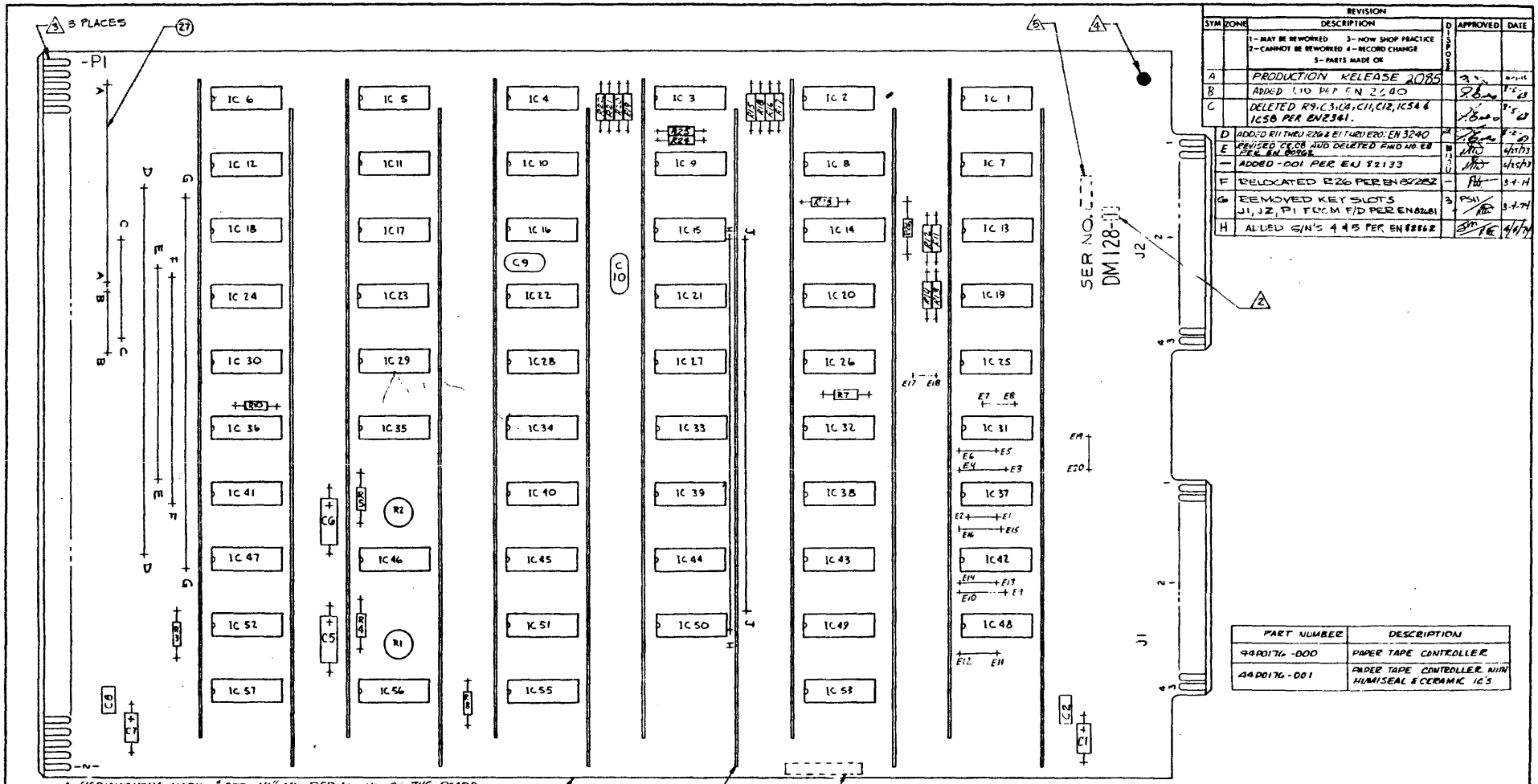
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0369	E
SCALE		SHEET 7 OF 9	



CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0369	E
SCALE		SHEET 8 OF 9	



CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0369	E
SCALE		SHEET 9 OF 9	



REVISION					
SYM	ZONE	DESCRIPTION	DISPOSITION	APPROVED	DATE
		1 – MAY BE REWORKED 3 – NOW SHOP PRACTICE 2 – CANNOT BE REWORKED 4 – RECORD CHANGE 5 – PARTS MADE OK			
A		PRODUCTION RELEASE 2085			
B		ADDED C10 PER EN 2640			7-5-73
C		DELETED R9, C3, C4, C11, C12, IC5 & 6 IC58 PER EN2341.			7-5-73
D		ADDED R11 THRU R226 & E1 THRU E20: EN 3240	M		7-2-73
E		REVISED CR, CB AND DELETED FIND NO. E8 PER EN 80962	M		4/25/73
—		ADDED -001 PER EN 82133	M		4/25/73
F		RELOCATED R26 PER EN 82282	—		3-1-74
G		REMOVED KEY SLOTS J1, J2, P1 FROM F/D PER EN 81281	B	PSH	3-1-74
H		ADDED S/N'S 4 & 5 PER EN 82862			4/8/74

PART NUMBER	DESCRIPTION
44D0176-000	PAPER TAPE CONTROLLER
44D0176-001	PAPER TAPE CONTROLLER WITH HUMISEAL & CERAMIC ICS

3 PERMANENTLY MARK "SER NO" AND SERIAL NO. OF THE BOARD IN .12 HIGH CHARACTERS APPROX WHERE SHOWN.

4 PERMANENTLY APPLY .3 YELLOW DOT TO BOARD APPROX WHERE SHOWN.

5 AFTER FINAL TEST AND PRIOR TO ACCEPTANCE TEST (-001 ONLY) MASK OFF CONNECTOR CONTACT AREA, BOTH SIDES OF F/N 1 AND TOTALLY COAT BOTH SIDES OF ASSEMBLY WITH F/N 40

2 MARK APPLICABLE VERSION (A) .19 HIGH PERMANENT CHARACTERS LOCATE APPROX. WHERE SHOWN.

1 MARK PART NUMBER 44D0176-(APPLICABLE VERSION) AND REVISION LETTER OF PARTS LIST TO WHICH PART WAS MANUFACTURED IN .12 HIGH PERMANENT CHARACTERS. LOCATE APPROX. WHERE SHOWN.

NOTE: UNLESS OTHERWISE SPECIFIED

REFERENCE DRAWINGS
91D0018 . . LOGIC DIAGRAM
91D0132 . . PHOTOMASTER
40D0199 . . BOARD DETAIL
44D0176 . . PARTS LIST

FIND NO.	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL OR CODE IDENT	SPECIFICATION
QTY REQD PER ASSY		LIST OF MATERIALS OR PARTS LIST		

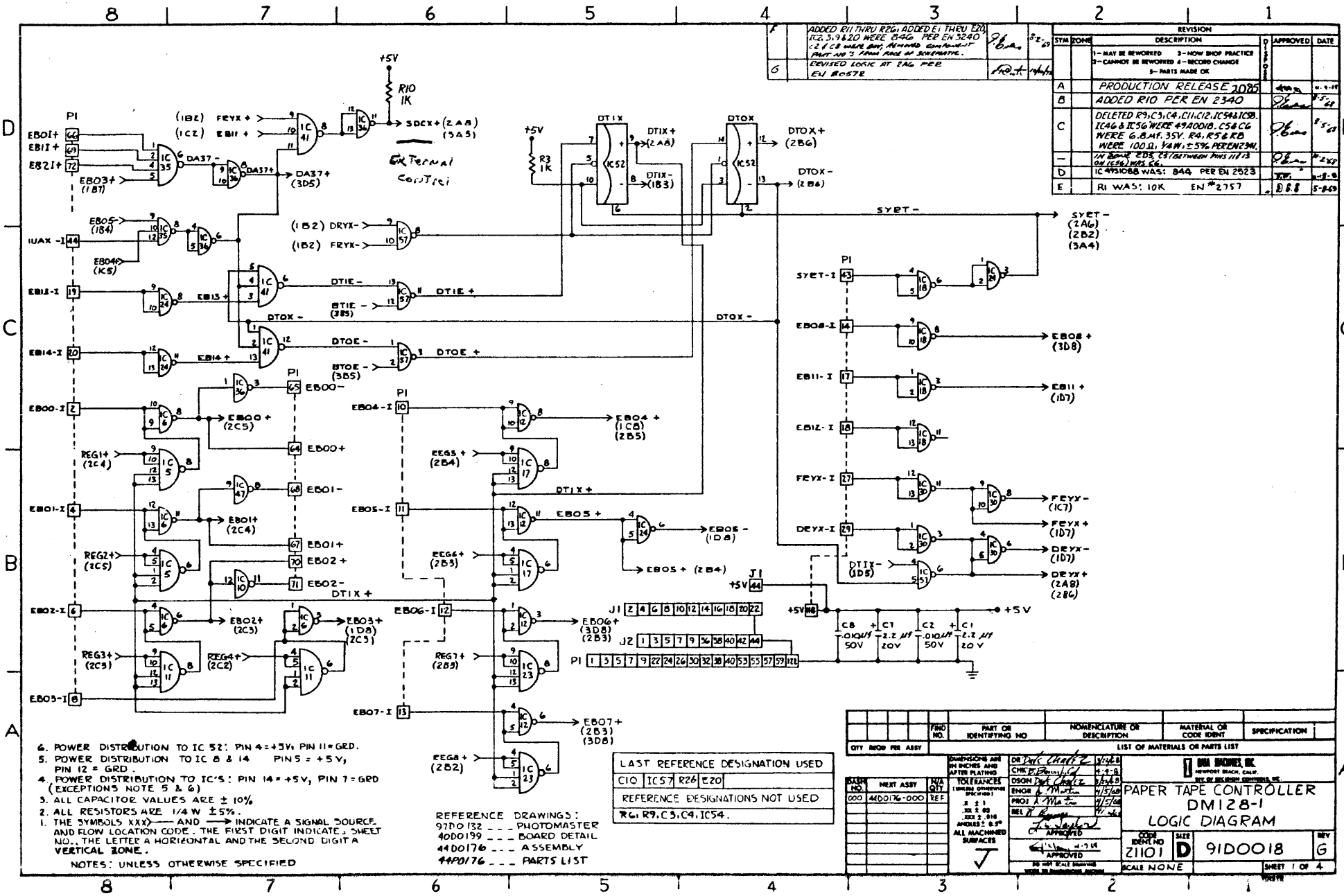
DASH NO.	NEXT ASSY	N/A QTY

DIMENSIONS ARE IN INCHES AND AFTER PLATING
TOLERANCES (UNLESS OTHERWISE SPECIFIED)
.X ± .1
.XX ± .03
.XXX ± .010
ANGLES ± 0.5°
ALL MACHINED SURFACES

DR Earl Christy 7/6/73
CHK [illegible] 7-9-73
DSGN [illegible]
ENGR [illegible]
PROJ [illegible]
REL A [illegible]
APPROVED
APPROVED
DO NOT SCALE DRAWING WORK TO DIMENSIONS ONLY

PAPER TAPE CONTROLLER
DM 128-1
ASSEMBLY

CODE IDENT NO	SIZE		REV
21101	D	44D0176	H
SCALE 2/1		SHEET 1 OF 1	



SYM	ZONE	REVISION DESCRIPTION	APPROVED	DATE
		1 - MAY BE REWORKED 3 - NOW SHOP PRACTICE 2 - CANNOT BE REWORKED 4 - RECORD CHANGE 5 - PARTS MADE OK		
A		PRODUCTION RELEASE 2085		4-9-69
B		ADDED R10 PER EN 2340		8-5-68
C		DELETED R3, C3, C4, C11, C12, IC58 & IC59. IC46 & IC56 WERE 4940018. C58 & C6 WERE 6.8 MF. 35V. R4, R5 & R8 WERE 100 Ω, ¼W, ± 5% PER EN 2341.		8-5-68
—		IN ZONE 2B5, C8 BETWEEN PINS 11 & 13 ON IC56 WAS C6.		4-8-9
D		IC 4931088 WAS: 844 PER EN 2523		5-8-69
E		R1 WAS: 10K EN #2757		5-8-69

SYM	ZONE		REVISION DESCRIPTION	APPROVED	DATE
F			ADDED R11 THRU R26; ADDED E1 THRU E20; IC2, 3, 9 & 20 WERE 846 PER EN 3240 C2 & C8 WERE 6MF; REMOVED COMPONENT PART NO'S FROM PAGE OF SCHEMATIC.		8-2-69
G			REVISED LOGIC AT 2A6 PER EN 80572		10-6-69

6. POWER DISTRIBUTION TO IC 52: PIN 4 = +5V, PIN 11 = GRD.
5. POWER DISTRIBUTION TO IC 8 & 14 PIN 5 = +5V, PIN 12 = GRD.
4. POWER DISTRIBUTION TO IC'S: PIN 14 = +5V, PIN 7 = GRD (EXCEPTIONS NOTE 5 & 6)
3. ALL CAPACITOR VALUES ARE ± 10%
2. ALL RESISTORS ARE 1/4 W ±5%.
1. THE SYMBOLS XXX ——— AND ———→ INDICATE A SIGNAL SOURCE AND FLOW LOCATION CODE. THE FIRST DIGIT INDICATES SHEET NO., THE LETTER A HORIZONTAL AND THE SECOND DIGIT A VERTICAL ZONE.

NOTES: UNLESS OTHERWISE SPECIFIED

LAST REFERENCE DESIGNATION USED				
C10	IC57	R26	E20	
REFERENCE DESIGNATIONS NOT USED				
R6, R9, C3, C4, IC54.				

REFERENCE DRAWINGS:
91D0132 - - - PHOTOMASTER
90D0199 - - - BOARD DETAIL
44D0176 - - - ASSEMBLY
44P0176 - - - PARTS LIST

FIND NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR CODE IDENT	SPECIFICATION	QTY REQD PER ASSY
		LIST OF MATERIALS OR PARTS LIST			

BASIC NO.	NEXT ASSY	N/A QTY
000	44D0176-000	REF

DIMENSIONS ARE IN INCHES AND AFTER PLATING
TOLERANCES (UNLESS OTHERWISE SPECIFIED)
.X ± 1
.XX ± 03
.XXX ± 010
ANGLES ± 0.5°
ALL MACHINED SURFACES

DR	Dale Chaffee	3/4/68
CHK	[illegible]	4-4-68
DSGN	Dale Chaffee	3/24/69
ENGR	A. Martin	4/5/68
PROJ	A. Martin	4/5/68
REL	[illegible]	4/5/68
	APPROVED	
	[illegible] 4-9-69 APPROVED	

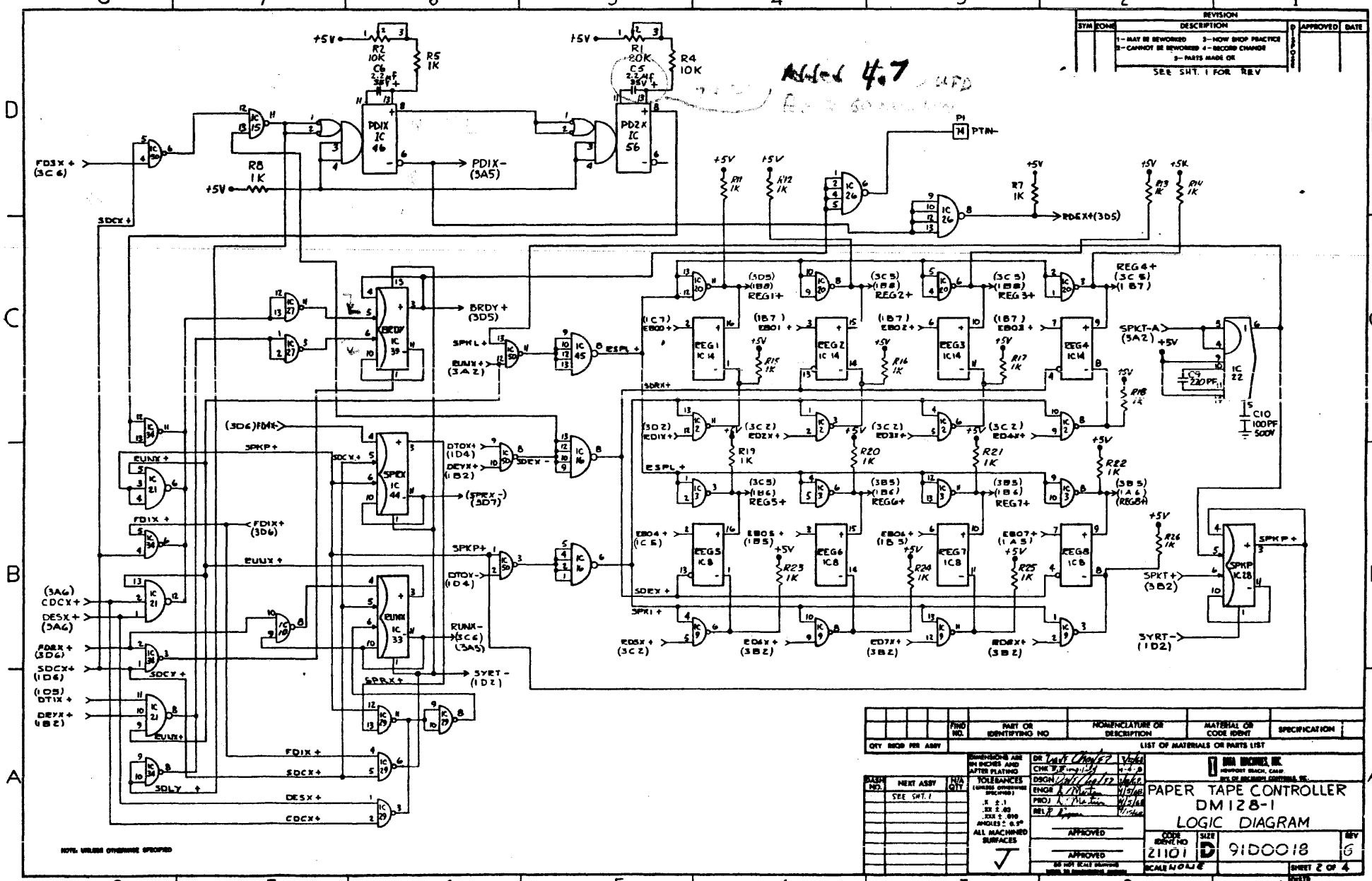
DO NOT SCALE DRAWING

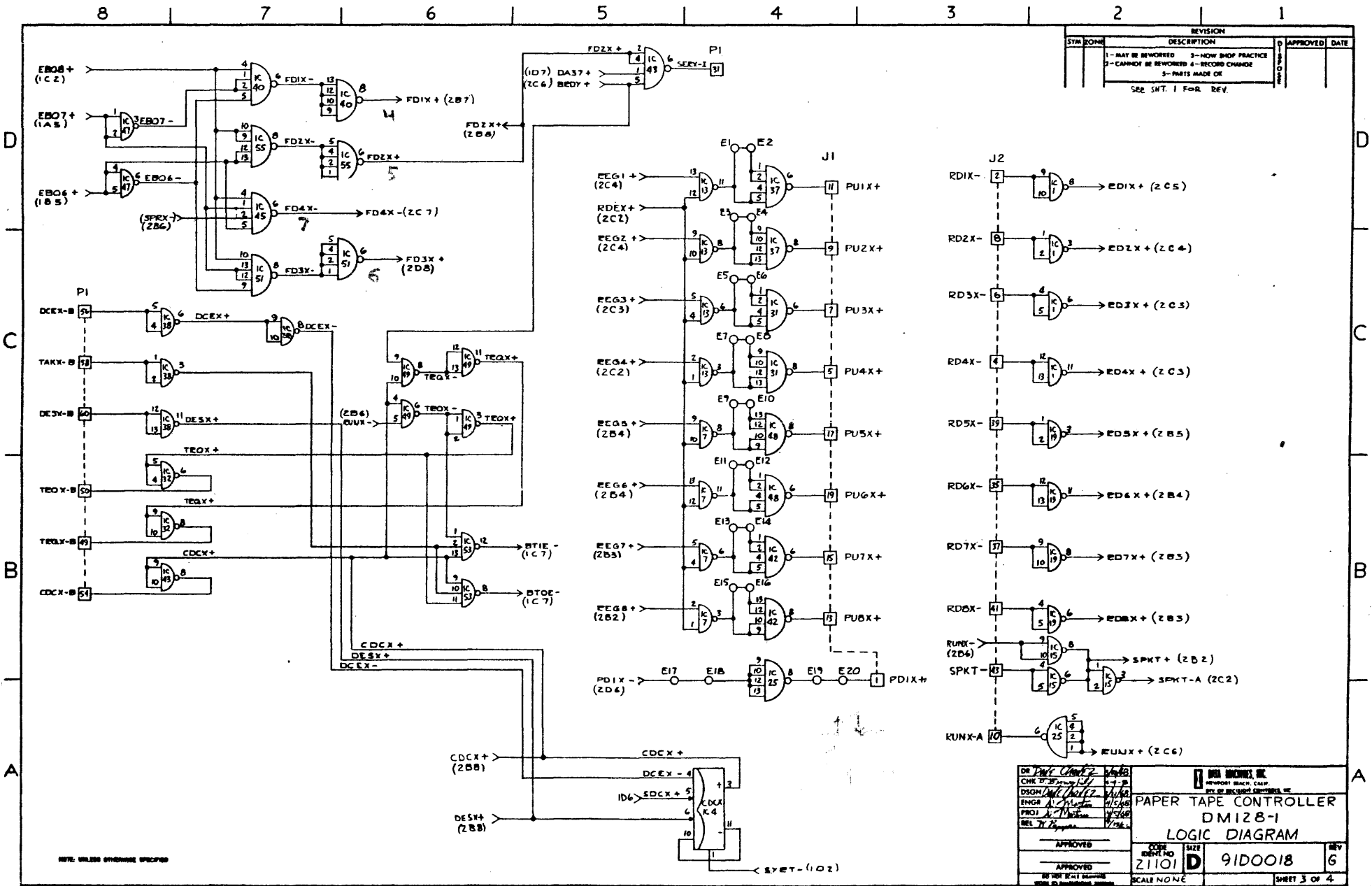
DIGI DYNAMICS, INC. NEWPORT BEACH, CALIF.

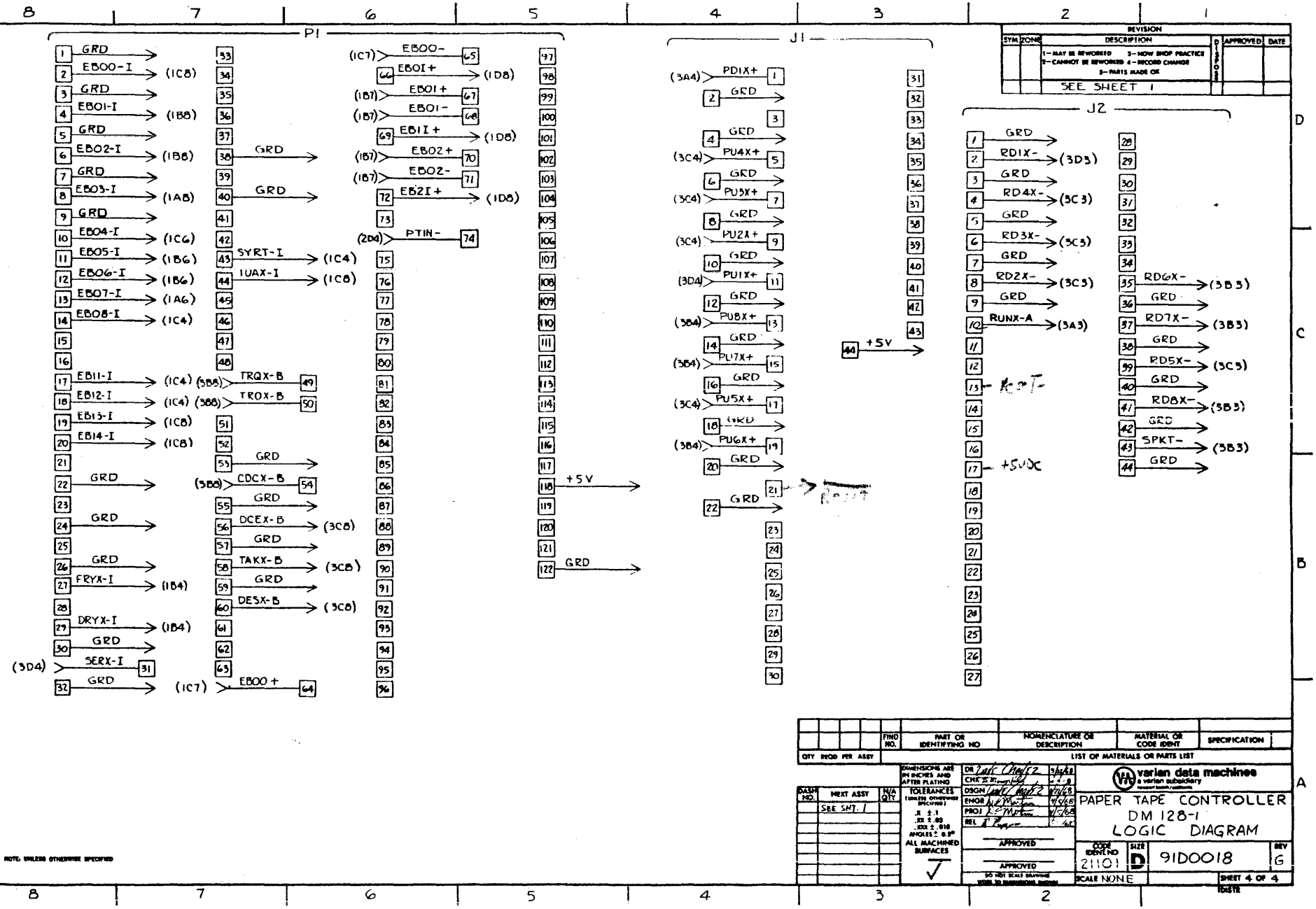
PAPER TAPE CONTROLLER
DM128-1
LOGIC DIAGRAM

CODE IDENT NO	SIZE	DWG NO	REV
21101	D	91D0018	G

SCALE NONE SHEET 1 OF 4


REVISION
SEE SHT. 1 FOR REV
PAPER TAPE CONTROLLER
DM128-1
LOGIC DIAGRAM
91D0018
SHEET 2 OF 4
PDIX-
(3A5)
PDEX+(3D5)
PTIN-
BRDY+
(3D5)
SPKT-A
(3A2)
SPKT+
(3B2)
SYRT-
(1D2)
RUNK-
(3C6)
(3A5)
SYET-
(1D2)
REG1+
REG2+
REG3+
REG4+
REG5+
REG6+
REG7+
REG8+
PDIX+
(3D6)
SPKP+
RUNX+
SDCX+
SDEX+
SPRX+
SDLY+
DESX+
CDCX+
FDIX+
FDEX+
SDRX+
SPKI+
ESPL+


REVISION
STM ZONE DESCRIPTION DATE APPROVED
1 - MAY BE REWORKED 3 - NOW SHOP PRACTICE
2 - CANNOT BE REWORKED 4 - RECORD CHANGE
5 - PARTS MADE OK
SEE SHT. 1 FOR REV.
EB08+ (1C2)
EB07+ (1A5)
EB06+ (1B5)
(SPRX-) (2B6)
FD1X+ (2B7)
FD4X-(2C7)
FD3X+ (2D8)
FD2X+ (2B8)
(1D7) DA37+
(2C6) BEDY+
SERY-1
P1
DCEX-B
TAKX-B
DESX-B
TEQX-B
TEQX-B
CDCX-B
DCEX+
DCEX-
TEQX+
TEQX-
TEQX+
(2B6) CLRX-
TEQX+
CDCX+
DESX+
DCEX-
BTIE-(1C7)
BTOE-(1C7)
J1
EEG1+ (2C4)
RDEX+ (2C7)
EEG2+ (2C4)
EEG3+ (2C3)
EEG4+ (2C2)
EEG5+ (2B4)
EEG6+ (2B4)
EEG7+ (2B3)
EEG8+ (2B2)
PU1X+
PU2X+
PU3X+
PU4X+
PU5X+
PU6X+
PU7X+
PU8X+
PD1X- (2D6)
PD1X+
J2
RD1X-
RD2X-
RD3X-
RD4X-
RD5X-
RD6X-
RD7X-
RD8X-
RUNX- (2D6)
SPKT-
RUNX-A
ED1X+ (2C5)
ED2X+ (2C4)
ED3X+ (2C3)
ED4X+ (2C3)
ED5X+ (2B5)
ED6X+ (2B4)
ED7X+ (2B3)
ED8X+ (2B3)
SPKT+ (2B2)
SPKT-A (2C2)
RUNX+ (2C6)
CDCX+ (2B8)
DESX+ (2B8)
CDCX+
DCEX-
SDCX+
SYET-(1D2)
PAPER TAPE CONTROLLER
DM128-1
LOGIC DIAGRAM
DR
CHK
DSGN
ENGR
PROJ
REL
APPROVED
APPROVED
DATA MACHINES, INC.
CODE IDENT NO 21101
SIZE D
91D0018
REV 6
SCALE NONE
SHEET 3 OF 4



REVISION					
SYM	ZONE	DESCRIPTION		APPROVED	DATE
		1 - MAY BE REWORKED 3 - NOW SHOP PRACTICE 2 - CANNOT BE REWORKED 4 - RECORD CHANGE 5 - PARTS MADE OK			
		SEE SHEET 1			

FIND NO.	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL OR CODE IDENT	SPECIFICATION
QTY REQD PER ASSY	LIST OF MATERIALS OR PARTS LIST			

ASSY NO.	NEXT ASSY	N/A QTY
	SEE SHT. 1	

DIMENSIONS ARE IN INCHES AND AFTER PLATING
TOLERANCES (UNLESS OTHERWISE SPECIFIED)
.X ± .1
.XX ± .03
.XXX ± .010
ANGLES ± 0.5°
ALL MACHINED SURFACES √

DR	Carl Chaffee	3/4/68
CHK	S Frumkin	3-4-68
DSGN	Carl Chaffee	3/4/68
ENGR	L F Martin	4/5/68
PROJ	L F Martin	4/5/68
REL	[illegible]	[illegible]

APPROVED

APPROVED

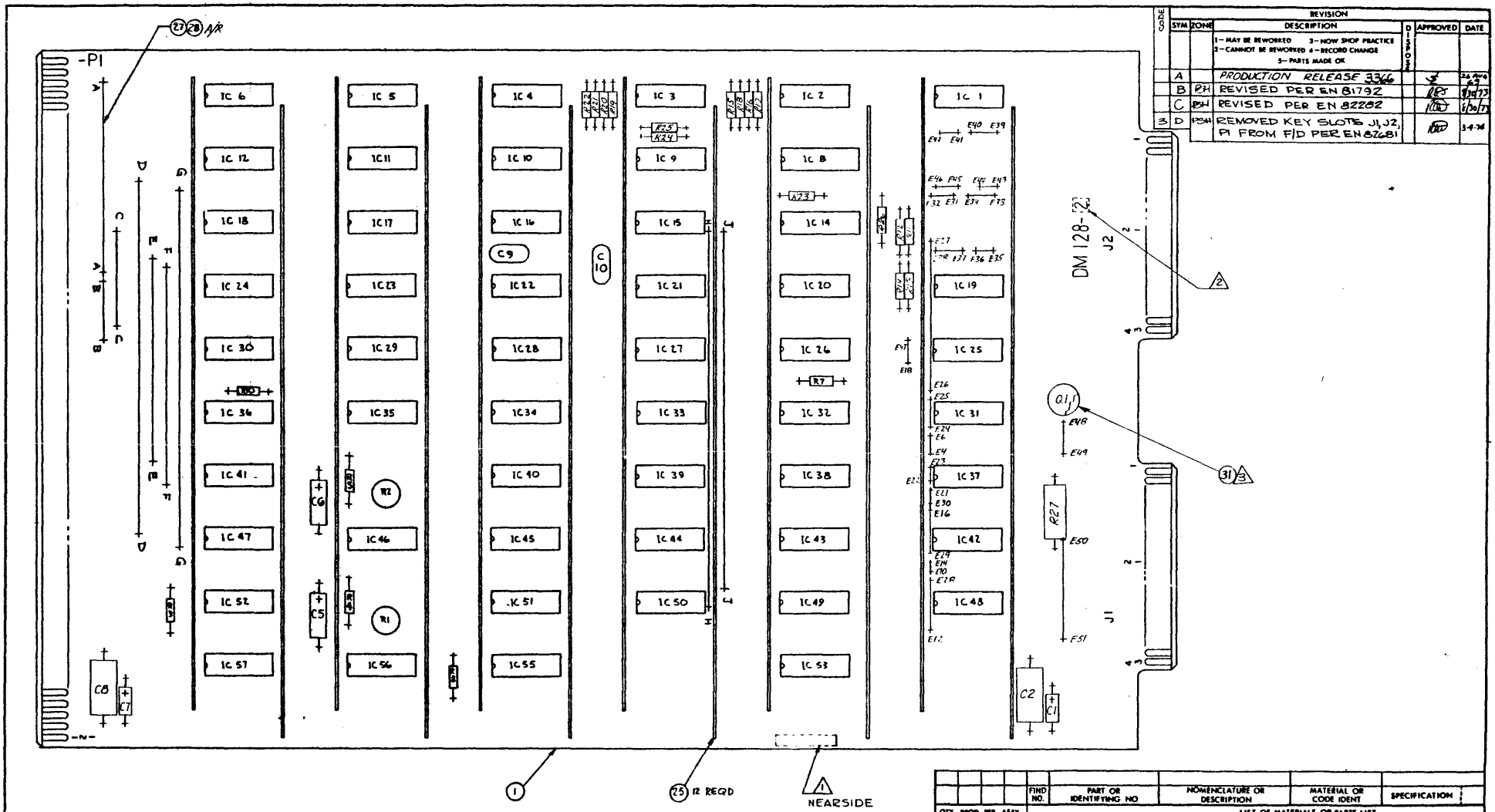
DO NOT SCALE DRAWING
WORK TO DIMENSIONS SHOWN

varian data machines
a varian subsidiary
newport beach, california

PAPER TAPE CONTROLLER
DM 128-1
LOGIC DIAGRAM

CODE IDENT NO	SIZE		REV
21101	D	91D0018	G
SCALE NONE			SHEET 4 OF 4

NOTE: UNLESS OTHERWISE SPECIFIED



CODE	SYM	ZONE	REVISION DESCRIPTION (1 – MAY BE REWORKED 2 – CANNOT BE REWORKED 3 – NOW SHOP PRACTICE 4 – RECORD CHANGE 5 – PARTS MADE OK)	DISPOSITION	APPROVED	DATE
	A		PRODUCTION RELEASE 3366			24 APR 69
	B	PH	REVISED PER EN 81792			9/9/73
	C	PSH	REVISED PER EN 82282			1/30/74
3	D	PSH	REMOVED KEY SLOTS J1, J2, P1 FROM F/D PER EN 82681			3-4-74

FIND NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR CODE IDENT	SPECIFICATION
QTY REQD PER ASSY		LIST OF MATERIALS OR PARTS LIST		

DASH NO.	NEXT ASSY	N/A QTY

DIMENSIONS ARE IN INCHES AND AFTER PLATING
TOLERANCES (UNLESS OTHERWISE SPECIFIED)
.X ± .1
.XX ± .03
XXX ± .010
ANGLES ± 0.5°
ALL MACHINED SURFACES

DR		11/2/69
CHK		7-31-69
DSGN		7/21/69
ENGR		
PROJ		
REL		

APPROVED

APPROVED

DO NOT SCALE DRAWING

DATA MACHINES, INC.
NEWPORT BEACH, CALIF.
DIV. OF BECKMAN CONTROLS, INC.

PAPER TAPE CONTROLLER ASSY, DM 128-2 (120 CPS)

CODE IDENT NO	SIZE	DWG NO	REV
21101	D	44D0311	D

SCALE 2/1 SHEET 1 OF 1

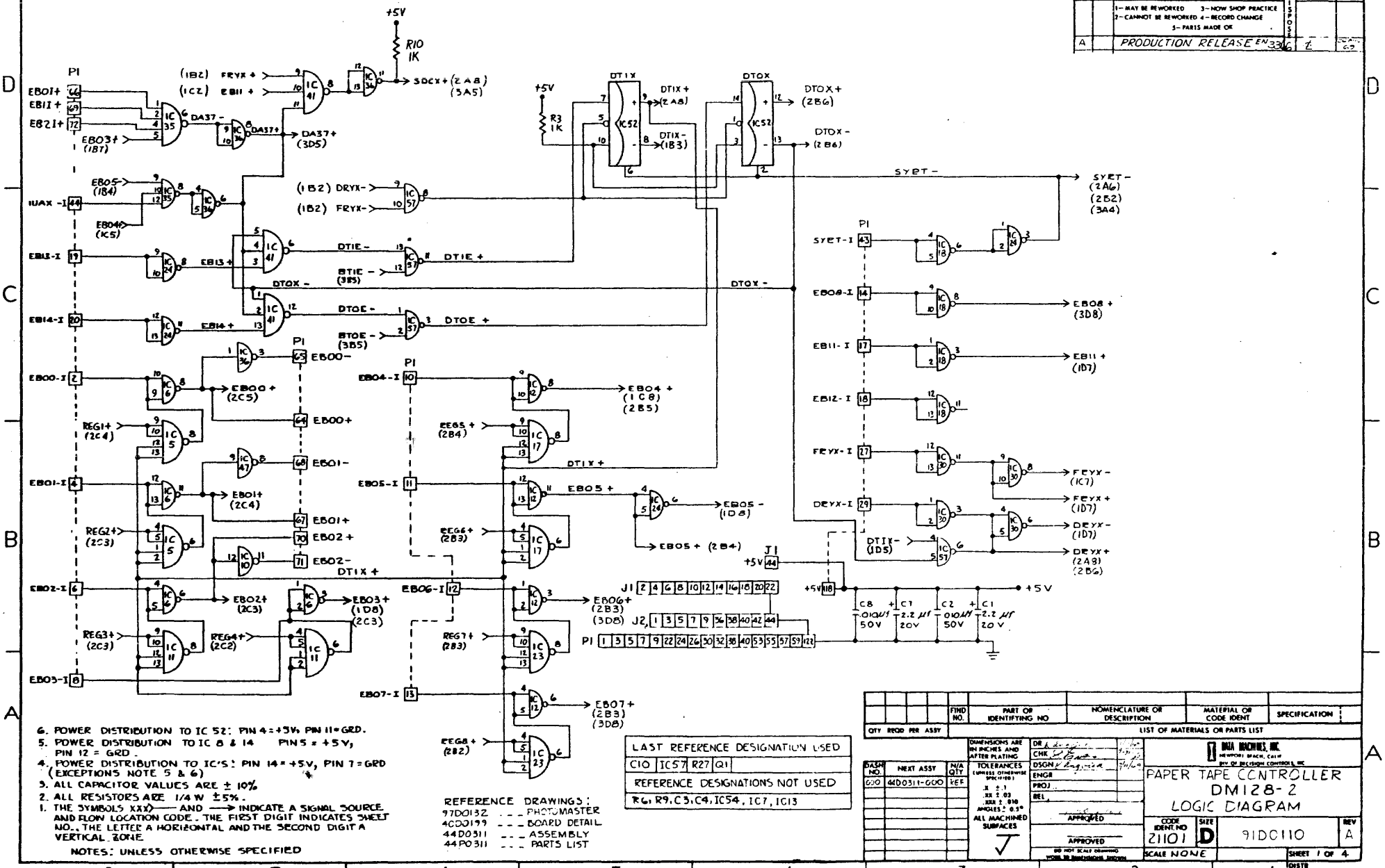
3 USE OF TRANSISTOR MOUNTING PADS OPTIONAL.

2 RUBBER STAMP VERSION APPROX WHERE SHOWN: USE .19 HIGH NUMBER AND BLACK ACID ETCH INK.

1 RUBBER STAMP CURRENT PARTS LIST NO., VERSION AND REVISION LETTER APPROX. WHERE SHOWN, USE .12 HIGH CHARACTERS AND BLACK ACID ETCH INK.

NOTE: UNLESS OTHERWISE SPECIFIED

REFERENCE DRAWINGS
91D0110 ___ LOGIC DIAGRAM
97D0132 ___ PHOTOMASTER
40D0199 ___ BOARD DETAIL
44P0311 ___ PARTS LIST



6. POWER DISTRIBUTION TO IC 52: PIN 4 = +5V, PIN 11 = GRD.
5. POWER DISTRIBUTION TO IC 8 & 14 PIN 5 = +5V, PIN 12 = GRD.
4. POWER DISTRIBUTION TO IC'S: PIN 14 = +5V, PIN 7 = GRD (EXCEPTIONS NOTE 5 & 6)
3. ALL CAPACITOR VALUES ARE ± 10%
2. ALL RESISTORS ARE 1/4 W ±5%.
1. THE SYMBOLS XXX⟩—— AND ——⟩ INDICATE A SIGNAL SOURCE AND FLOW LOCATION CODE. THE FIRST DIGIT INDICATES SHEET NO., THE LETTER A HORIZONTAL AND THE SECOND DIGIT A VERTICAL ZONE.

NOTES: UNLESS OTHERWISE SPECIFIED

LAST REFERENCE DESIGNATION USED
C10 IC57 R27 Q1
REFERENCE DESIGNATIONS NOT USED
R6, R9, C3, C4, IC54, IC7, IC13

REFERENCE DRAWINGS:
97D0132 ___ PHOTOMASTER
4CD0199 ___ BOARD DETAIL
44D0311 ___ ASSEMBLY
44P0311 ___ PARTS LIST

REVISION					
SYM	ZONE	DESCRIPTION	DISPOSITION	APPROVED	DATE
		1- MAY BE REWORKED 3- NOW SHOP PRACTICE 2- CANNOT BE REWORKED 4- RECORD CHANGE 5- PARTS MADE OR			
A		PRODUCTION RELEASE EN 33	C	Z	

FIND NO.	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL OR CODE IDENT	SPECIFICATION
QTY REQD PER ASSY	LIST OF MATERIALS OR PARTS LIST			

DASH NO.	NEXT ASSY	N/A QTY
000	44D0311-000	REF

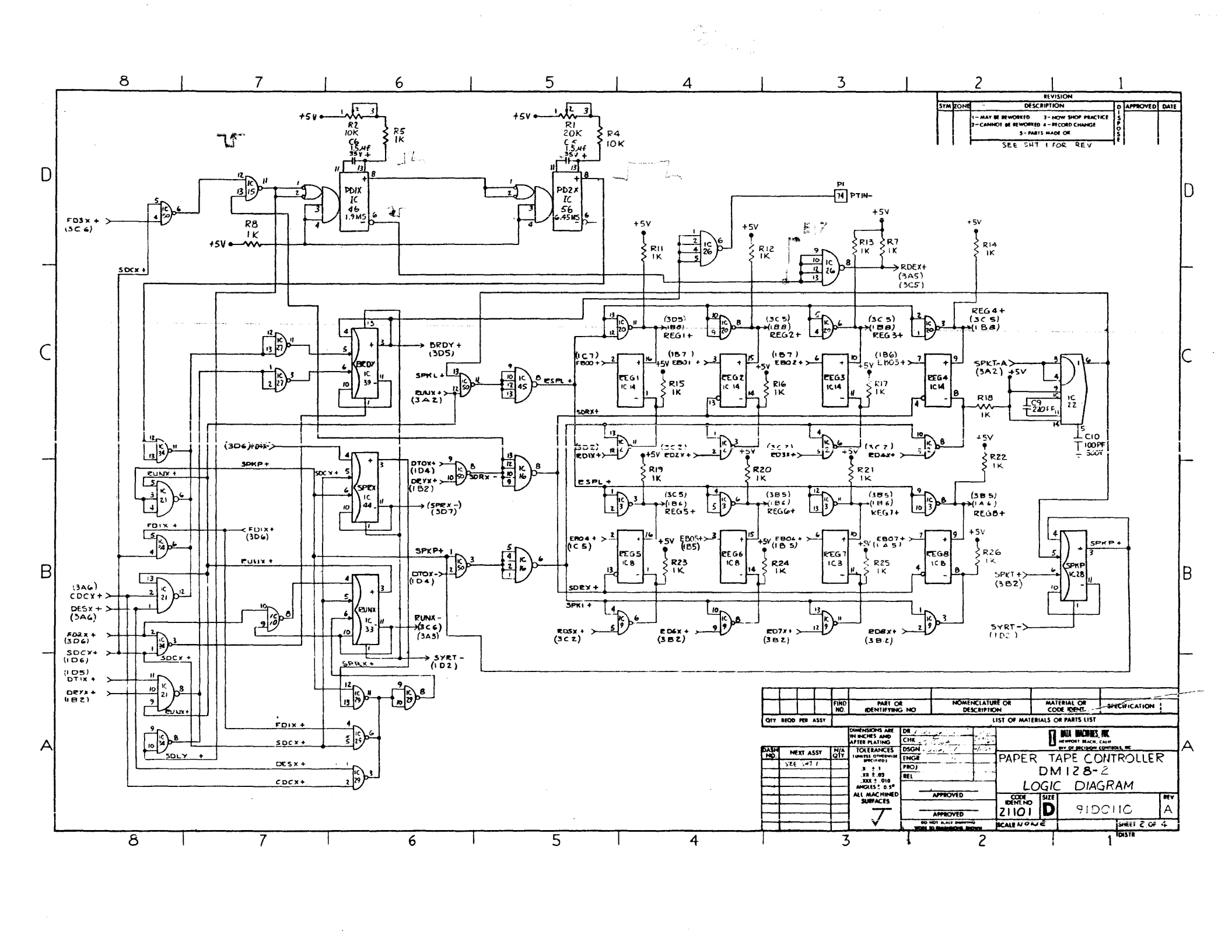
DIMENSIONS ARE IN INCHES AND AFTER PLATING
TOLERANCES (UNLESS OTHERWISE SPECIFIED) .X ± .1 .XX ± .03 .XXX ± .010 ANGLES ± 0.5° ALL MACHINED SURFACES

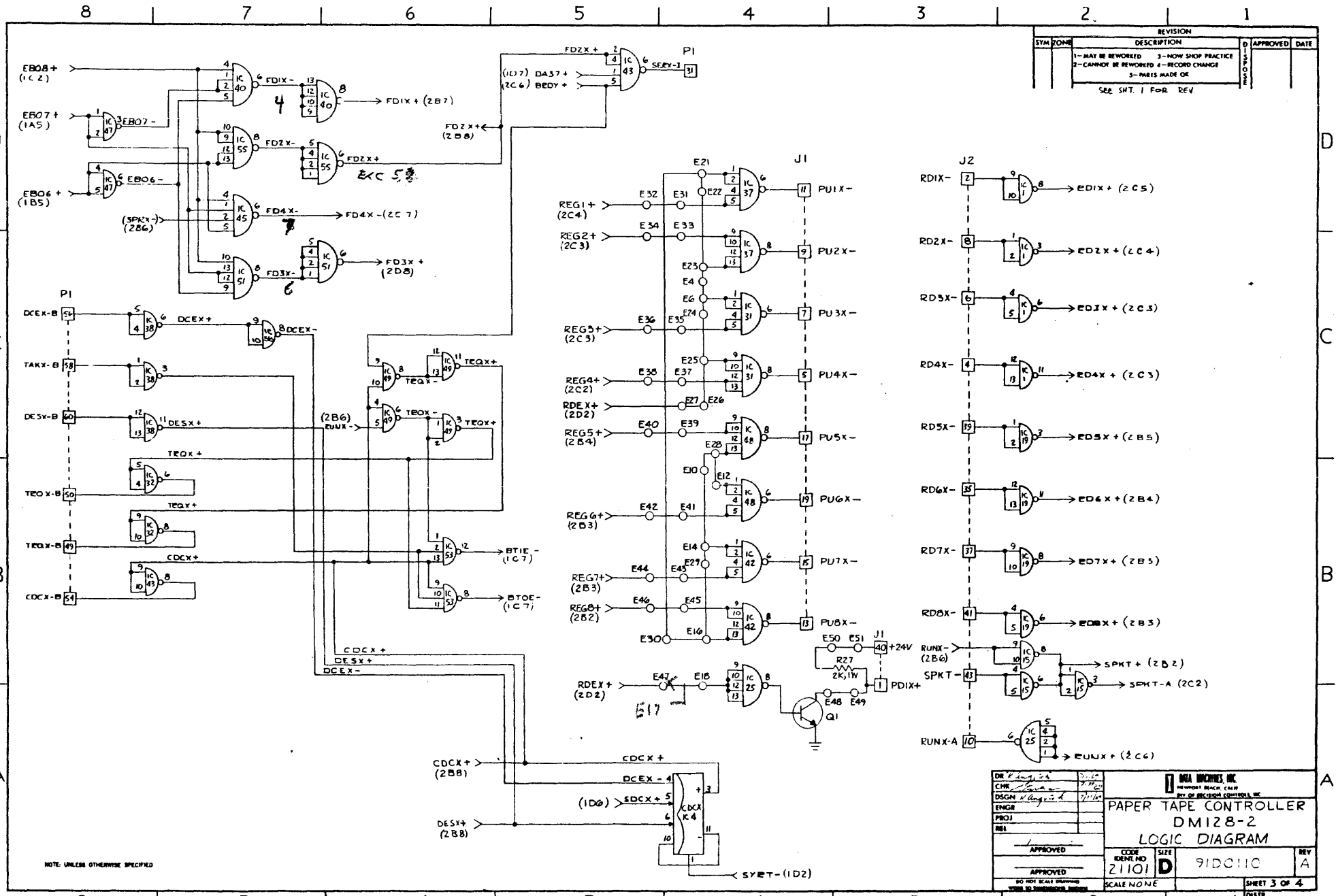
DR
CHK
DSGN
ENGR
PROJ
REL
APPROVED
APPROVED
DO NOT SCALE DRAWING WORK TO DIMENSIONS SHOWN

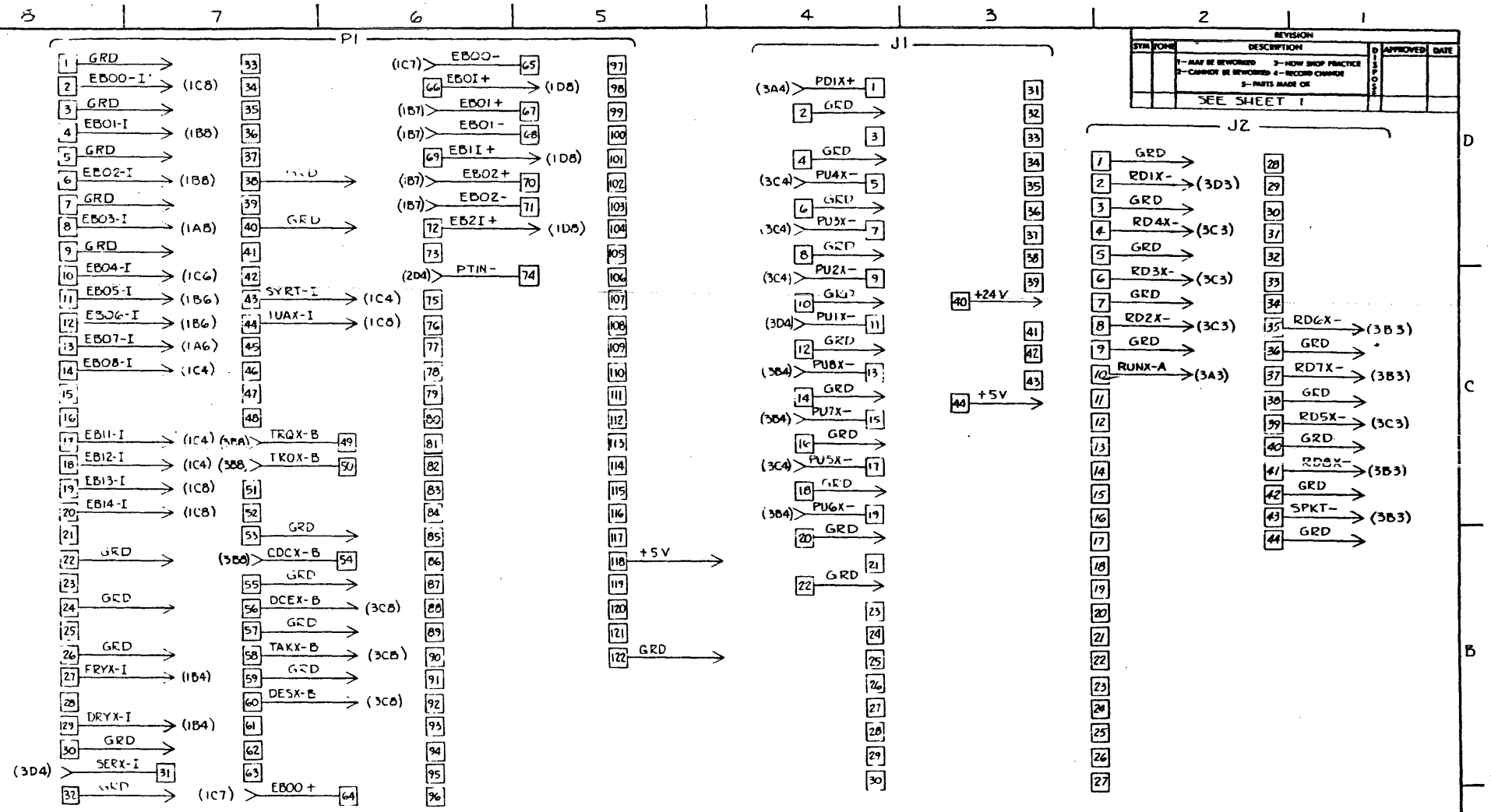
DATA DYNAMICS, INC. NEWPORT BEACH, CALIF. DIV. OF BECKMAN CONTROLS, INC.

PAPER TAPE CONTROLLER
DM128-2
LOGIC DIAGRAM

CODE IDENT NO	SIZE		REV
21101	D	91D0110	A
SCALE NONE		SHEET 1 OF 4	


REVISION
SYM ZONE DESCRIPTION APPROVED DATE
1 - MAY BE REWORKED 3 - NOW SHOP PRACTICE
2 - CANNOT BE REWORKED 4 - RECORD CHANGE
5 - PARTS MADE OR
SEE SHT 1 FOR REV
PAPER TAPE CONTROLLER
DM128-2
LOGIC DIAGRAM
DATA MACHINES, INC.
CODE IDENT NO 21101
SIZE D
91D0110
REV A
SCALE NONE
SHEET 2 OF 4
LIST OF MATERIALS OR PARTS LIST
FIND NO. PART OR IDENTIFYING NO. NOMENCLATURE OR DESCRIPTION MATERIAL OR CODE IDENT. SPECIFICATION
QTY REQD PER ASSY
DASH NO. NEXT ASSY N/A QTY
TOLERANCES
ALL MACHINED SURFACES
APPROVED
APPROVED
DR CHK DSGN ENGR PROJ REL
PTIN-
RDEX+ (3A5) (3C5)
BRDY+ (3D5)
SPKT-A (3A2)
SPKT+ (3B2)
SYRT- (1D2)
RUNX+ (3A2)
RUNX- (3C6) (3A3)
SPRX+
SDCX+
SDLY+
DESX+
CDCX+
FD3X+ (3C6)
FD2X+ (3D6)
SDCX+ (1D6)
(1D5) DTIX+
DEYX+ (1B2)
(3A6) CDCX+
DESX+ (3A6)
FDIX+ (3D6)
SPKP+
DTOX- (1D4)
DEYX+ (1B2)
(SPRX-) (3D7)
SDRX+
ESPL+
REG1+
REG2+
REG3+
REG4+
REG5+
REG6+
REG7+
REG8+
EB00+
EB01+
EB02+
EB03+
EB04+
EB05+
EB06+
EB07+
RDIX+
RDEX+
RD3X+
RD4X+
RDSX+
RD6X+
RD7X+
RD8X+
PDIX IC 46 1.9MS
PD2X IC 56 6.45MS
R1 20K
R2 10K
R4 10K
R5 1K
R7 1K
R8 1K
R11 1K
R12 1K
R13 1K
R14 1K
R15 1K
R16 1K
R17 1K
R18 1K
R19 1K
R20 1K
R21 1K
R22 1K
R23 1K
R24 1K
R25 1K
R26 1K
C5 1.5MF 35V
C6 1.5MF 35V
C9 .2MFD
C10 100PF 300V


REVISION
SYM ZONE DESCRIPTION APPROVED DATE
1-MAY BE REWORKED 3-NOW SHOP PRACTICE
2-CANNOT BE REWORKED 4-RECORD CHANGE
5-PARTS MADE OK
SEE SHT. 1 FOR REV.
EB08+ (1C2)
EB07+ (1A5)
EB07-
EB06+ (1B5)
EB06-
FDIX-
FD2X-
FD4X-
FD3X-
FDIX+ (2B7)
FD2X+ (2B8)
FD4X-(2C7)
FD3X+ (2D8)
FDZX+
(1D7) DA37+
(2C6) BEDY+
SERV-1
P1
DCEX-B
TAKX-B
DESX-B
TEQX-B
CDCX-B
DCEX+
DCEX-
TEQX+
TEQX-
BTIE- (1C7)
BTOE- (1C7)
(2B6) EUUX-
CDCX+
DESX+
DCEX-
CDCX+ (2B8)
DESX+ (2B8)
(1D6) SDCX+
SYET-(1D2)
J1
REG1+ (2C4)
REG2+ (2C3)
REG3+ (2C3)
REG4+ (2C2)
RDEX+ (2D2)
REG5+ (2B4)
REG6+ (2B3)
REG7+ (2B3)
REG8+ (2B2)
PU1X-
PU2X-
PU3X-
PU4X-
PU5X-
PU6X-
PU7X-
PU8X-
+24V
R27 2K,1W
PDIX+
Q1
RDEX+ (2D2)
J2
RDIX-
RD2X-
RD3X-
RD4X-
RD5X-
RD6X-
RD7X-
RD8X-
RUNX-(2B6)
SPKT-
RUNX-A
EDIX+ (2C5)
ED2X+(2C4)
ED3X+(2C3)
ED4X+(2C3)
ED5X+(2B5)
ED6X+(2B4)
ED7X+(2B5)
ED8X+(2B3)
SPKT+(2B2)
SPKT-A (2C2)
EUUX+(2C6)
NOTE: UNLESS OTHERWISE SPECIFIED
DR
CHK
DSGN
ENGR
PROJ
REL
APPROVED
APPROVED
DO NOT SCALE DRAWING
DATA MACHINES, INC.
NEWPORT BEACH, CALIF.
DIV. OF DECISION CONTROLS, INC
PAPER TAPE CONTROLLER
DM128-2
LOGIC DIAGRAM
CODE IDENT. NO 21101
SIZE D
91D0110
REV A
SCALE NONE
SHEET 3 OF 4
DISTR



DASH NO.	NEXT ASSY	N/A QTY
	SEE SHT. 1	

NOTE: UNLESS OTHERWISE SPECIFIED

varian data machines
a varian subsidiary

PAPER TAPE CONTROLLER
DM 128-2
LOGIC DIAGRAM

CODE IDENT NO	SIZE		REV
21101	D	91D0110	A

SCALE NONE SHEET 4 OF 4

DWG NO 89A0189

REVISIONS			
SYM	DESCRIPTION	APPROVED	DATE
X A	Pre Production Release Production Release EN 5753		6/8/71
B	REVISED PER EN 5757		9/8/71
C	CHANGES PER EN 80634		4/25/72
D	REVISED PER EN 82926		4/23/74

J. P. Spender approved
J. P. Spender, Engineering Operations

T. H. Sweere approved
T. H. Sweere, Systems Engineering

DR	B. Ribaudo	4-29-71
CHK		6-22-71
DSGN	D. Purcell	6-8-71
ENGR		
APPD		6-8-71
APPD		6/8/71

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2722 michelson drive / irvine / california / 92664

TITLE

SOFTWARE PERFORMANCE SPECIFICATION

Paper Tape System and BIC Test

CODE IDENT NO.	SIZE	DWG NO.	REV
21101	A	89A0189	D

SCALE

SHEET 1 OF 95

96A0153-001

TABLE OF CONTENTS

SECTION 1
TEST PROGRAM OVERVIEW

1.1 INTRODUCTION

The 620 Paper Tape System and BIC Test determines whether or not the high speed paper tape system and BIC are functioning correctly. The paper tape punch and paper tape reader can be tested with the same controller or with separate controllers. Punch, step-read, and continuous-read modes are checked. The BIC is thoroughly tested in a special BIC subtest but can also be employed in the punch and continuous - read areas.

The special case of the abnormal device stop occurring prior to the first data transfer is not tested.

The 620 Paper Tape System and BIC Test operates with the 620 Test Executive and thus uses standard teletype I/O routines and is equipped with both a Console Mode and a Teletype Mode (see Manual No. 98A9952-06R).

1.2 PROGRAM DESIGN OVERVIEW

The program first allows the user to indicate whether he wishes to test the BIC or the paper tape system. If he wishes to test the paper tape system (punch and/or reader), he may test the punch process in sense, PIM, or BIC mode; the step-read process in sense or PIM mode; or the continuous-read process in sense; PIM, or BIC mode. If he wishes to test the BIC, he may test it with or without a BIC - through interrupt. All device addresses, trap locations, and interrupt masks are input from the user. Data patterns are set by the user in the paper tape section of the test.

The BIC section of the test checks all critical address ranges for the initial and final BIC registers. The provided test tape (92V0107-023) must be used for this test.

1.3 HARDWARE SUMMARY

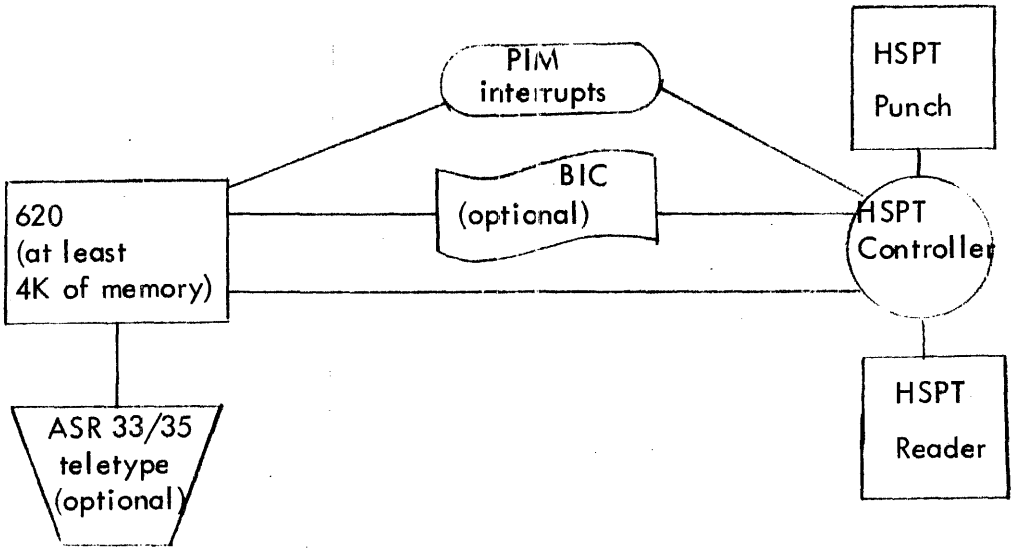
The following hardware items are required or are optional to use this program:

1. A 73/620 series computer with at least 4K of memory.
2. A High Speed Paper Tape Reader.
3. A High Speed Paper Punch*.
4. (Optional) PIM.

*The test may be employed if only the High Speed Paper Tape Punch or only the High Speed Paper Tape Reader is available.

5. (Optional) BIC (necessary for BIC section of test).

A hardware diagram is given below:



SECTION 2
EXTERNAL SPECIFICATIONS

2.1 GENERAL

The external specification provides all the operating procedures and information pertinent to user interface.

2.2 LOADING PROCEDURE

The 620 Paper Tape and BIC Test is available as an object tape.

2.2.1

The user must secure a copy of the 620 Test Executive object tape (part number 92U0107-001). The device used to load the tapes can be the ASR33 or ASR35 teletype paper tape reader or the high speed paper tape reader. The 620 Test Executive is loaded first and executed to set the Console/Teletype Mode flag (see 2.3) according to the user's entry point. The 620 Paper Tape and BIC Test is then loaded either by typing an "L." from the 620 Test Executive (if a teletype is being used), or by loading it from the console.

2.2.2

The user must then load the programs by manually starting the appropriate Executive loader (see manual number 98A9952-06R).

2.3 OPERATING PROCEDURE

After loading the 620 Test Executive, and the 620 Paper Tape and BIC Test, and setting the Console/Teletype Mode flag by entry point to the 620 Test Executive, the user sets the program counter to 0500 and resets SS3. The two procedures for Console and for Teletype Mode are given next.

2.3.1 Sense Switch Settings

Switch	'Set'	'Reset'
1	Suppress error printouts	Print Error messages

SS2	Halt on error (continue after error halt)	Do not halt on error
SS3	Terminate current operation return to beginning of test	Continue test

2.3.2 Teletype Mode

After starting the program at 0500, the teletype prints:

620 PAPER TAPE AND BIC TEST
PT PUNCH DA =
The user then inputs the octal device address of the high speed paper tape punch followed by a period or comma.

The teletype then prints:

PT READER DA =

The user then inputs the octal device address of the high speed paper tape reader followed by a period or comma.

The teletype then prints:

BIC TEST REQUESTED?

The user then responds with a 'Y' or an 'N' for 'yes' or 'no', respectively (no period or comma is input). if 'Y' is input see 2.3.2.2.

2.3.2.1

If 'N' is input, the test types:

BIC USED?

The user then responds with a 'Y' or an 'N' (no period or comma is input).

If the answer was 'Y', the test types:

BIC DA =

The user then inputs the octal device address of the BIC followed by period or comma.

The test then continues at 2.3.2.1.2.

If the answer was 'N' to BIC USED?, the test types:

PIM USED?

The user then responds with a 'Y' or an 'N' (no period or comma is input).

If the answer was 'N', the test then continues at 2.3.2.1.2.

2.3.2.1.1

If the answer was 'Y', the test types:

PIM DA =

The user then inputs the octal device address of the PIM followed by a period or comma.

The test then types:

TRAP LOCATION =

The user then inputs the octal address of the trap branch for the interrupt line being used followed by a period or comma.

The test then types:

INTERRUPT MASK =

The user then inputs the interrupt mask which masks-out all interrupts but the one being used followed by a period or comma. See table in 2.3.4.

2.3.2.1.2

After the I/O mode information is set, the test types:

INPUT TEST TYPE

The user then inputs 'P', 'R', or 'H' for 'punch', 'step-read', or 'continuous-read', respectively. If he wishes to use the data set last used (or on the first pass, the assembler default), he then inputs '.'. Otherwise he inputs ',' and the test types:

INPUT LOWER LIMIT, UPPER DATA LIMIT, AND DATA BLOCK SIZE

The user then inputs 3 octal values* in succession corresponding, respectively, to these terms and separated by commas or periods and ending with a period or comma.

The test then types:

CYCLES =

The user then inputs the number of cycles in octal or 0 for continuous, followed by a period or comma.

If the 'R' parameter was input for the test type, the test types:

TIME DELAY =

The user then inputs a positive number which produces a time delay of 13 times that number times the CPU cycle time. This delay is executed prior to executing the step-read command after the buffer ready is sensed. If the user inputs a negative number, a random number generator is invoked to give successive random wait periods to be executed instead. The value input must be followed by a period or comma .

After all this information is input the test is performed according to the given parameters. An error condition produces a descriptive message as given in 2.4. When the test is done the following is printed:

BIC TEST REQUESTED?

The process is then restarted, with the difference that device addresses, trap locations, and interrupt masks are input only once, unless SS3 is hit or the test restarted at 0500.

2.3.2.2

If 'Y' is input to 'BIC TEST REQUESTED?', the user must place the provided test tape (92V0107-023) in the reader positioned anywhere on the initial blank leader. The test types the following:

BIC DA =

The user then inputs the BIC device address in octal, followed by a period or comma. The test then types:

PIM USED?

The user responds by inputting 'Y' or 'N' (no period or comma is input). If 'N'

* When using the BIC to output or input data a maximum of 0400 is allowed for the data block size parameter, due to the provided buffer length.

is input the interrupt parameters are skipped.

If 'Y' is input, the test types:

PIM DA =

The user then inputs the octal value of the PIM device address followed by a period or comma.

The test then types:

TRAP LOCATION =

The user then inputs the address for the trap branch for the interrupt line to be used. This is followed by a period or comma.

The test then types:

INTERRUPT MASK =

The user then inputs the interrupt mask which masks-out the interrupt lines not used, followed by a period or comma. See table in 2.3.4.

The test then types:

CYCLES =

The user then inputs the number of cycles in octal or 0 for continuous followed by a period or comma.

The BIC test is then performed. The BIC test tape is read into the memory at the critical locations. If an error occurs, a descriptive message is typed (as given in 2.4).

When the test is through, the test types:

BIC TEST REQUESTED?

The process is then restarted, with the difference that device addresses, trap locations, and interrupt masks are input only once, unless SS3 is hit or the test restarted at 0500.

2.3.3 Console Mode

After starting the program at 0500, the program halts with 020 in the instruction

register. The user sets the A-register to the high speed paper tape punch device address and the B-register to the high speed paper tape reader address. He then hits 'RUN' and the program halts with 021 in the instruction register. The user then sets the A-register to '1' or '0' for BIC test or no BIC test, respectively. The user then hits 'RUN'. If the BIC test was specified see 2.3.3.2.

2.3.3.1

If the BIC test is not indicated, the test halts with 022 in the instruction register. The user sets the A-register to '-1', '0', or '1' for BIC mode, sense mode, and PIM mode, respectively. If the BI C mode is specified, the user must put the BIC device address in the B-register. 'RUN' is then hit. If sense or BIC mode was specified, the test goes to 2.3.3.1.2.

2.3.3.1.1

If PIM mode was specified, the test halts with 023 in the instruction register. The user then places the PIM device address in the A-register, the trap location in the B-register, and the interrupt mask in the X-register (see table 2.3.4). The user then hits 'RUN'. (see 2.3.3.1.2)

2.3.3.1.2

The test halts with 024 in the instruction register. The user then sets the A-register to 0, 1, or 2 for the punch test, the step-read test, or the continuous-read test, respectively. He then hits 'RUN'.

In any case the test then halts with 026 in the instruction register. The user then places the lower data limit in the A-register, the upper data limit in the B-register, and the data block size* in the X-register. He then hits 'RUN'.

The test then halts with 027 in the instruction register. The user then sets the A-register to the cycle count (0 means continuous) and hits 'RUN'.

If the step-read option was specified, the test halts with 025 in the instruction register. The user sets the A-register to a positive number or a negative number. If the number is positive, a time delay of 13 times that number times the CPU cycle time is executed prior to executing the step-read command after the buffer ready is sensed. If the number is negative, a random number generation is invoked to give successive random wait periods to be executed instead.
After all this information is obtained, the test is performed according to the given

* When using the BIC to output or input data a maximum of 0400 is allowed for the data block size parameter, due to the provided buffer length.

parameters. An error condition produces a halt as given in 2.6.

When the test is done, a halt occurs with 021 in the instruction register and the process repeats. The difference is that device addresses, trap locations, and interrupt masks are input only once, unless SS3 is hit or the test restarted at 0500.

2.3.3.2

If the user specified that he wishes to perform the BIC test, the test halts with 030 in the instruction register. The user must place the provided test tape (92V0107-023) in the reader positioned anywhere on the initial blank leader. The user then sets the A-register to the BIC device address, and the B-register to '1' for PIM used or '0' for no PIM used. The user then hits 'RUN.' If no PIM is specified, the PIM parameters are skipped.

If PIM is specified, the test halts with 031 in the instruction register. The user then sets the PIM device address in the A-register, the trap location in the B-register, and the interrupt mask in the X-register (see 2.3.4). The user then hits 'RUN'.

The test next halts with 032 in the instruction register. The user then sets the A-register to the number of cycles that the test is to be performed (a 0 means continuous). The user then hits 'RUN'.

The test is now performed according to the given parameters. An error condition produces a halt according to 2.6.

When the test is done, a halt occurs with 021 in the instruction register and the process repeats. The difference is that device addresses, trap locations, and interrupt masks are input only once, unless SS3 is hit or the test restarted at 0500.

2.3.4 Interrupt Table

Interrupt Line	Most Common Trap Location	Interrupt Mask
0	0100	0376
1	0102	0375
2	0104	0373
3	0106	0367
4	0110	0357
5	0112	0337
6	0114	0277
7	0116	0177

2.4 OUTPUT STATEMENTS

620 PAPER TAPE AND BIC TEST

PT PUNCH DA =

PT READER DA =

BIC USED?

PIM USED?

PIM DA =

TRAP LOCATION =

BIC DA =

INPUT TEST TYPE

BUFFER READY TIME-OUT

BIC BUSY TIME-OUT

BIC ABNORMAL STOP

ERROR(s)

INPUT LOWER DATA LIMIT, UPPER DATA LIMIT, AND DATA BLOCK SIZE

CYCLES =

INTERRUPT MASK =

BIC TEST REQUESTED?

SECTION	ACTUAL	
X	YYYYYY	} error data

CHIP	EXPECTED	ACTUAL	
XXXXXX	YYYYYY	ZZZZZZ	} error data

BIC-THROUGH INTERRUPT WHEN BIC BUSY

NO BIC-THROUGH INTERRUPT

TIME DELAY =

2.5 INPUT STATEMENTS

The following statements require the subsequent input of an octal value, followed by a period or comma.

PT PUNCH DA =

PT READER DA =

PIM DA =

TRAP LOCATION =

BIC DA =

CYCLES =

INTERRUPT MASK =

TIME DELAY =

The following statement requires the subsequent input of a sequence of 3 octal values separated and terminated by periods or commas or a mixture of both.

INPUT LOWER DATA LIMIT, UPPER DATA LIMIT, AND DATA BLOCK SIZE

The following statements require the input of 'Y' or 'N'.

BIC USED?

PIM USED?

BIC TEST REQUESTED?

The following statement requires the input of 'P', 'R', or 'H' followed by a comma or period.

INPUT TEST TYPE

2.6 HALT TABLE

Instruction Register	Significance
020	Set: A=HSPT punch device address, B=HSPT reader device address.

Instruction Register	Significance
021	Set: A = '1' for BIC test, '0' for no BIC test.
022	Set: A = '-1' for BIC used, '1' for PIM used, '0' for sense mode, B = BIC device address(if appropriate)
023	Set: A = PIM device address, B = trap location, X = interrupt mask. (buffer-ready interrupts)
024	Set: A = '0' for punch test, '1' for step-read test, '2' for continuous-read test.
025	Set: A = time delay for step-read test.
026	Set: A = lower data limit, B = upper data limit, X = data block size.
027	Set: A = cycle count, '0' for continuous.
030	Set: A = BIC device address, B = '1' for PIM used, '0' for no PIM used.
031	Set: A = PIM device address, B = trap location, X = interrupt mask. (BIC-through interrupts-BIC test)
032	Set: A = cycle count, '0' for continuous.
01	Buffer ready time-out.
02	BIC-busy time-out.
03	BIC abnormal stop.
04	Data error(s) read, number of errors in A-register.
05	(Halt on error mode) A = error data, B = expected data.
06	Data error(s) read (BIC test), number of errors in A-register.
07	Halt on error mode (BIC test), A contains error data, B contains expected data, and X contains the chip number.
010	BIC -through interrupt when BIC busy.
011	No BIC -through interrupt.

2.7 MEMORY MAP

Location	Contents
0-0200	Test Executive Area
0200-0212	Indirect Pointers
0220-0377	BIC Test Buffer
0400-0477	Test Executive Area
	Jump to Mainline
	User Interface Routine
0502-01101	I/O Buffer
01102-01133	Data and Flag Area
01134-01644	Mainline User
	Interface Routine
02000-02010	BIC Test Buffer
02011-02274	Punch Test Routine
02275-02400	PIM Enable, Sense
	Buffer Ready Routine
02401-02555	Punch (or Read) BIC Mode)
02556-03110	Step Reader Test Routine
03111-03137	Error Save Area
03140-03307	High Speed Reader
	Test Routine
03310-03543	Read (Sense or PIM Mode)
03544-03602	Pseudo-Random
	Number Generator
03603-03707	Parameter Setting Subroutine
04000-04010	BIC Test Buffer
04011-05203	BIC Test Routine
05204-05230	Device Address Setter
05231-05617	Message Buffers
05620-07777	Test Executive
0220-0377	BIC Test Buffers
0502-0512	(If Memory Equipted with such addresses)
01000-01010	
02000-02010	
04000-04010	
010220-010377	
020220-020377	
040220-040377	

2.8 UNDERSTANDING THE BIC TEST PRINTOUT

Section	Memory Address To Be Trapped Into	Data To Be Input	Address Logic On BIC Activated
1	220 - 377	220 - 377	7 - 0
2	502 - 512	102 - 112	8 Plus 7 - 0
3	1000 - 1010	0 - 10	9 Plus 7 - 0
4	2000 - 2010	0 - 10	10 Plus 7 - 0
5	4000 - 4010	0 - 10	11 Plus 7 - 0
6	10220 - 10377*	220 - 377	12 Plus 7 - 0
7	20220 - 20377*	220 - 377	13 Plus 7 - 0
8	40220 - 40377*	220 - 377	14 Plus 7 - 0

*If these memory locations do not exist, no error printout will occur.

SECTION 3
INTERNAL SPECIFICATIONS

3.1 GENERAL DESCRIPTION

The 620 Paper Tape System and BIC test consists of 5 major subsections each consisting of a set of routines. Some of the subroutines used in the major sections are common to more than one section.

The major sections are 1) Mainline User Interface Routine, 2) Punch Test Routine, 3) Step Speed Reader Test Routine, 4) High Speed Reader Test Routine, 5) BIC Test Routine.

3.2 COMPONENT SPECIFICATIONS

Title: Mainline User Interface Routine

Symbolic Name: EP01

Purpose: To allow the user to communicate the test specifications to the program and to comply with those directives by setting various values and by branching to the appropriate test routine.

Description: HSPT ready and punch device address, I/O mode, and the test to be performed are communicated to the program via a teletype (Teletype Mode), or via the 620 console (Console Mode). The appropriate test is then invoked.

Entry Points: Location 0500, EP01, EP10, EP10+5. The first two entry points cause test to type test I.D. The third entry point causes the parameters like device addresses and trap locations to be input the fourth entry point ships these inputs.

Calling Sequence: EP01 is not a closed routine and is entered either by a JMP insruction, or by setting the entry address in the P-register, clearing the Instruction-register, and hitting run.

Entrance Parameters: None

Exit Point: None

Exit Parameters: Not applicable

Table or Files Modified or Read:	$PCH, $RRD, $PIM, $BIC, MODE, MASK PMLO, PRFL, PMFL, and BCFL are altered.
Tables or Files Created:	Not applicable
Called By:	Not applicable
Called From:	OUTD, OUTC, INPG, INPD, OUTG.
Exception Conditions:	In teletype mode, when an overtly invalid parameter is input by the user, 'INVALID' is typed and the parameter must be re-input.
Timing:	Not applicable (Test is HSPT - bound, timewise)
Size:	See Memory Map
Comments:	Start test at 0500 and a jump to EP01 is automatically executed. Always run the test only when the Maintain II Test Executive also resides in memory and make sure the Teletype/Console Mode Flag in the Test Executive is first set.
Special Notation:	Not applicable
Hardware Details:	620 computer
Flowcharts:	See 3.3.

Title:	Punch Test Routine
Symbolic Name:	PTST
Purpose:	To test the high speed paper tape punch according to user given paramters.
Description:	Data parameteas are bbtained from the user through subroutine PARS, unless the user wishes to use the default parameters (i.e. - the last data parameters input; or on the first time, the assembled parameters). Subroutines are then invoked to punch the specified data. Errors are reported to the user.

Entry Points:	**PTST**
Calling Sequence:	**The Punch Test Routine is not a closed subroutine and is entered by a jump to PTST, or a console start from PTST.**
Entrance Parameters:	HSPT device addresses and I/O mode information must be set at entry time. The Teletype/Console Mode Flag must also be set.
Exit Point:	PTST normally returnes to EP01 at either EP10 or EP10+5.
Exit Parameters:	Not applicable
Table or Filew Modified or Read:	$PCH, $PIM, $BIC, MODE, TSTF, TOFL, LOLM, UPLM, BLSZ, CYCL, CRCY, CRCD, CRCT, MASK, PMLO
Tables or Files Created:	Not applicable
Called By:	Entered from EP01
Called From:	INPG, OUTC, PARS, DVAD, PPUN, PPNB
Exception Conditions:	Errors are reported to the user. In general, hit 'SYSTEM RESET' and 'RUN' to continue.
Timing:	HSPT - bound
Size:	See Memory Map
Comments:	None
Special Notation:	None
Hardware Details:	620 computer, HSPT controller with HSPT punch. PIM, BIC optional
Flowcharts:	See 3.3

Title:	**Step Speed Reader Test Routine**
Symbolic Name	RTST
Purpose:	To test the high speed paper tape reader in step speed according to user given parameters.
Description:	Data parameters are obtained from the user through subroutine PARS, unless the user wishes to use the default parameters (i.e. - the last data parameters input or on the first time the assembled parameters). A delay parameter is also obtained from the user. Subroutines are then invoked to read the tape in step, speed and compare with the specified data. Errors are reported to the user.
Entry Points:	RTST and special HTST entry points RT05 and RT01+2.
Calling Sequence:	The Step Speed Test Routine is not a closed subroutine and is entered by a jump to RTST, or a console start from RTST.
Entrance Parameters:	HSPT device addresses and I/O mode information must be set at entry time. The Teletype/Console Mode Flag must also be set.
Exit Point:	RTST normally returns to EP01 at either EP10 or EP10+5.
Exit Parameters :	Not applicable
Table or Files Modified or Read:	$RRD, $PIM, $BIC, MODE, TSTF, IOFL, LOLM, UPLM, BLSZ, CYCL, CRCY, CRCD, CRCT, MASK, PMLO, DELY
Tables or Files Created:	Input Buffer - BUFF is used.
Called By:	Entered from EP01 and HTST.
Called From:	INPG, PARS, OUTC, OUTD, DVAD, CLER, PRDR, QUTE,
Exception Conditions:	Errors are reported to the user. In general (except for data errors) hit 'SYSTEM RESET' and 'RUN' to continue.
Timing:	HSPT - bound
Size:	See Memory Map

Comments:	None
Special Notation:	None
Hardware Details:	620 computer, HSPT controller with HSPT reader, PIM optional.
Flowcharts:	See 3.3
Title:	High Speed Reader Test Routine
Symbolic Name:	HTST
Purpose:	To test the high speed paper tape reader in continuous mode according to user given parameters.
Description:	Data parameters are obtained from the user through subroutine PARS, unless the user wishes to use the default parameters (i.e. - the last data parameters input, or, on the first time, the assembled parameters). Subroutines are then invoked to read the tape in continuous mode and compare with the specified data. Errors are reported to the user.
Entry Points:	HTST
Calling Sequence:	The High Speed Test Routine is not a closed subroutine and is entered by a jump to HTST, or a console start from HTST.
Entrance Parameter:	HSPT device addresses and I/O mode information must be set at entry time. The Teletype/Console Mode Flag must also be set.
Exit Point:	HTST normally returns to EP01 at either EP10 or EP10+5.
Exit Parameters:	Not applicable
Tables or Files Modified or Read:	$RRD, $PIM, $BIC, MODE, TSTF, IOFL, LOLM, UPLM, BLSZ, CYCL, CRCY, CRCD, CRCT, MASK, PMLO
Tables or Files Created:	Input Buffer - BUFF is used.
Called By:	Entered from EP01
Called From:	Enters RTST, calls INPG, OUTC, PARS, DVAD, CLER, PPNB.

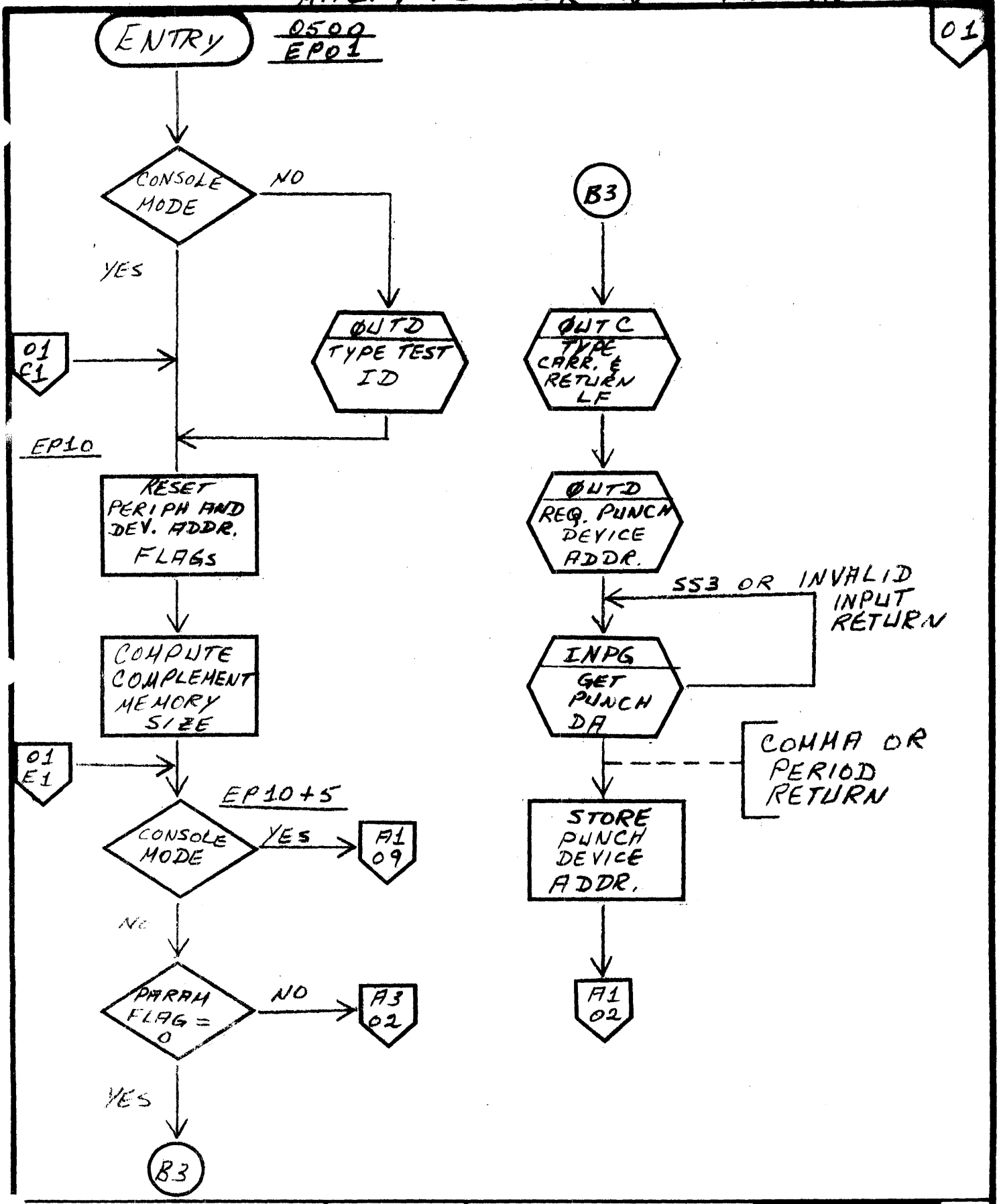
Exception Conditions:	Errors are reported to the user. In general (except for data errors), hit 'SYSTEM RESET' and 'RUN' to continue.
Timing:	HSPT - bound
Size:	See Memory Map
Comments:	None
Special Notation:	None
Hardware Details:	620 computer, HSPT controller with HSPT reader. PIM and BIC optional.
Flowcharts:	See 3.3

Title:	BIC Test Routine
Symbolic Name:	BTST
Purpose:	To throughly test the BIC using the high speed paper tape reader.
Description:	Data parameters are obtained from the user to give the program I/O Mode information and cycle count. Subroutine are then invoke to BIC in from the given BIC Test Tape. The results are compared with the specified data. Mechanical or data errors are reproted to the user.
Entry Points:	BTST
Calling Sequence:	The BIC Test Routine is not a closed subroutine and is entered by a jump to BTST, or a console start from BTST.
Entrance Parameters:	HSPT device addresses must be set at entry time. The Teletype/ Console Mode Flag must also be set.
Exit Point:	BTST normally returns to EP01 at EP10 or EP10+5.
Exit Parameters:	Not applicable
Table or Files Modified or Read:	$RRD, $PIM, $PM2, $BIC, MODE, TSTF, BTMD, IOFL, CRCY, CYCL, MSK2, PML2, PMF2, BCFL
Tables or Files Created:	A set of input areas are used.

Called By:	Entered from EP01
Called From:	DVAD, OUTD, INPG, OUTC, INPD, OUTG, CLER, PRDR, BCIN, CMPR, QUTE
Exception Conditions:	Errors are reported to the user. In general (except for data errors), hit 'SYSTEM RESET' and 'RUN' to continue.
Timing:	HSPT - found
Size:	See Memory Map
Comments:	None
Special Notation:	None
Hardware Details:	620 computer, HSPT controller with HSPT reader, BIC. PIM options .
Flowcharts:	See 3.3

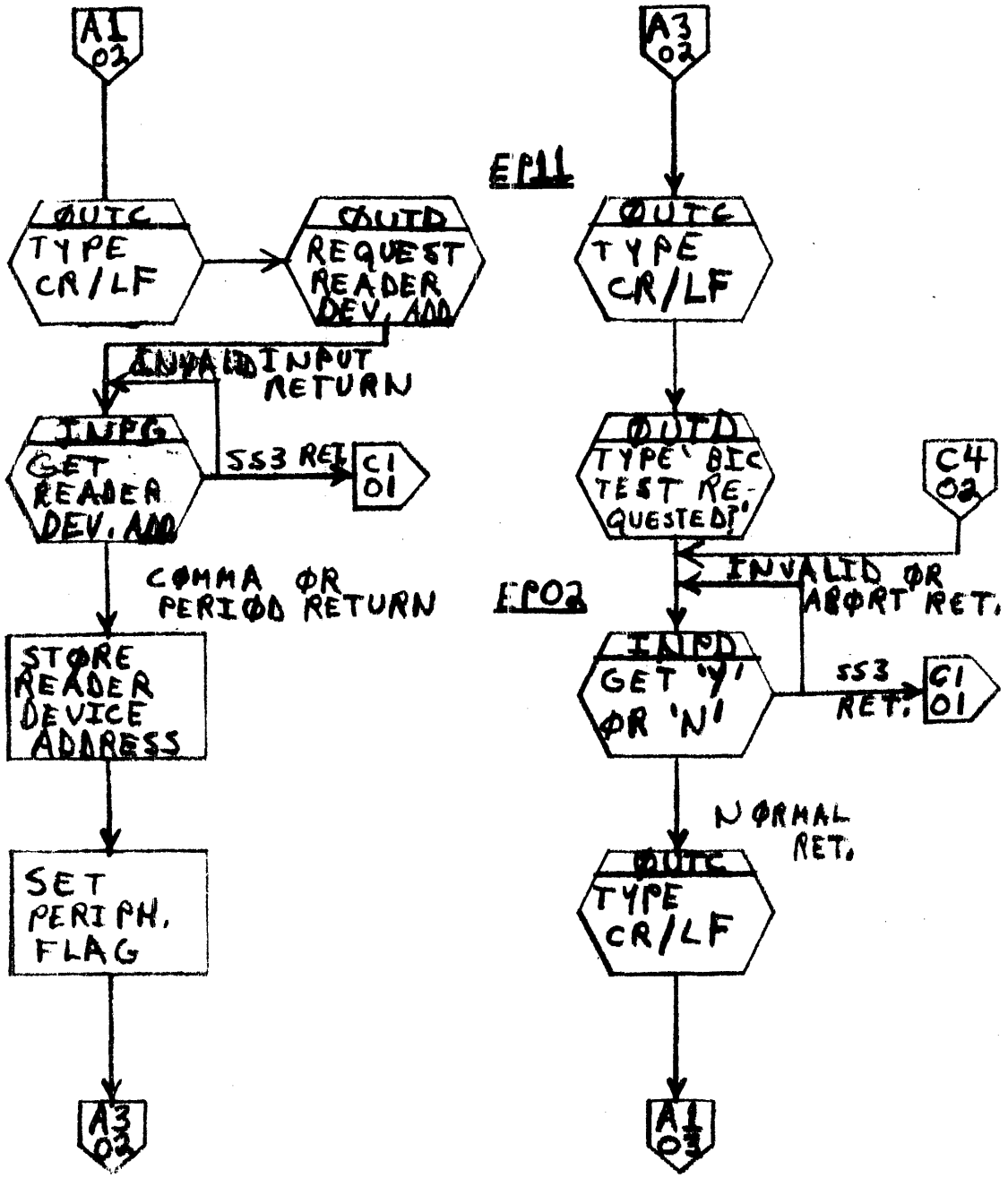
3.3 FLOWCHARTS

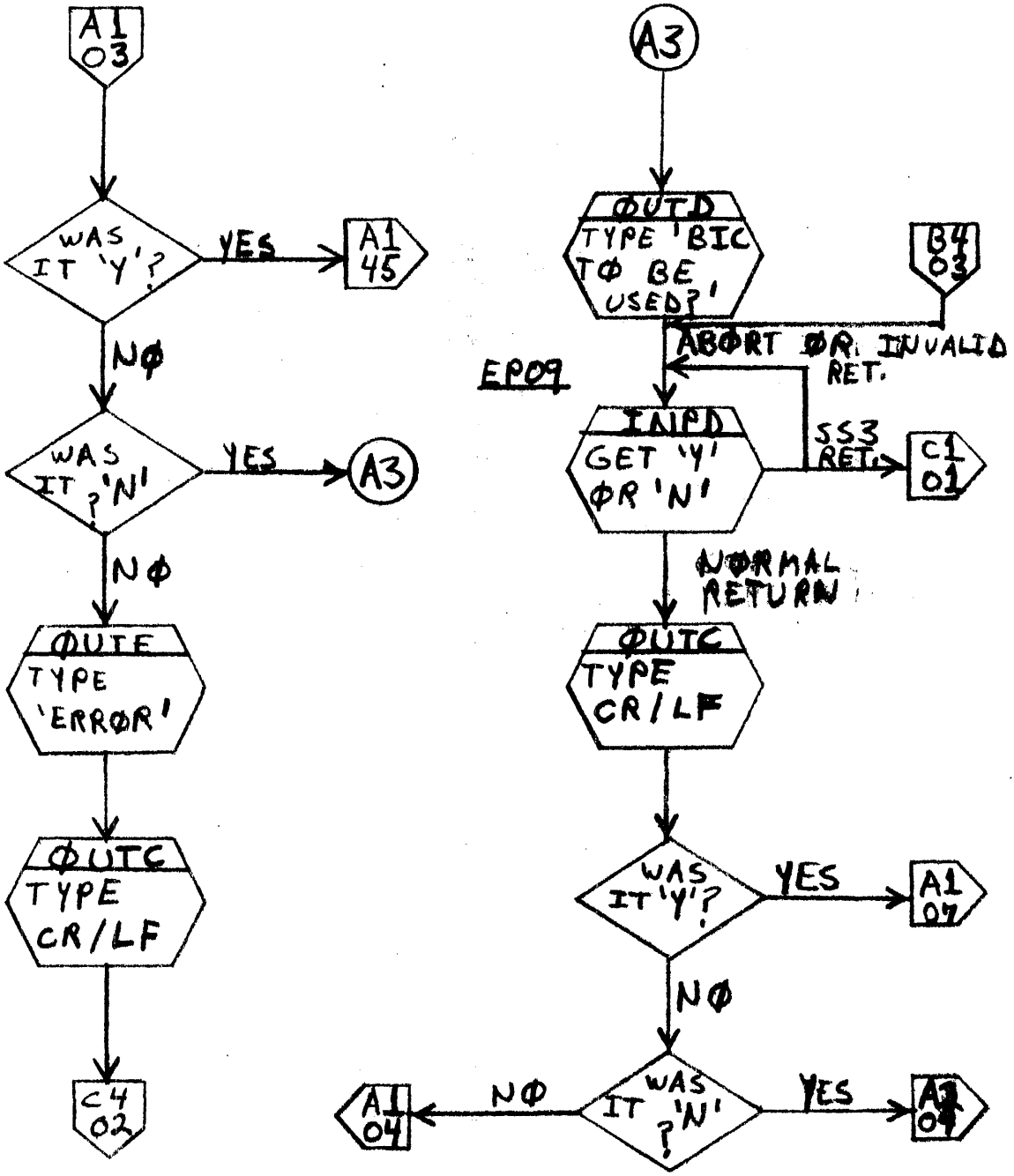
MAINLINE WORK INTERFACE ROUTINE

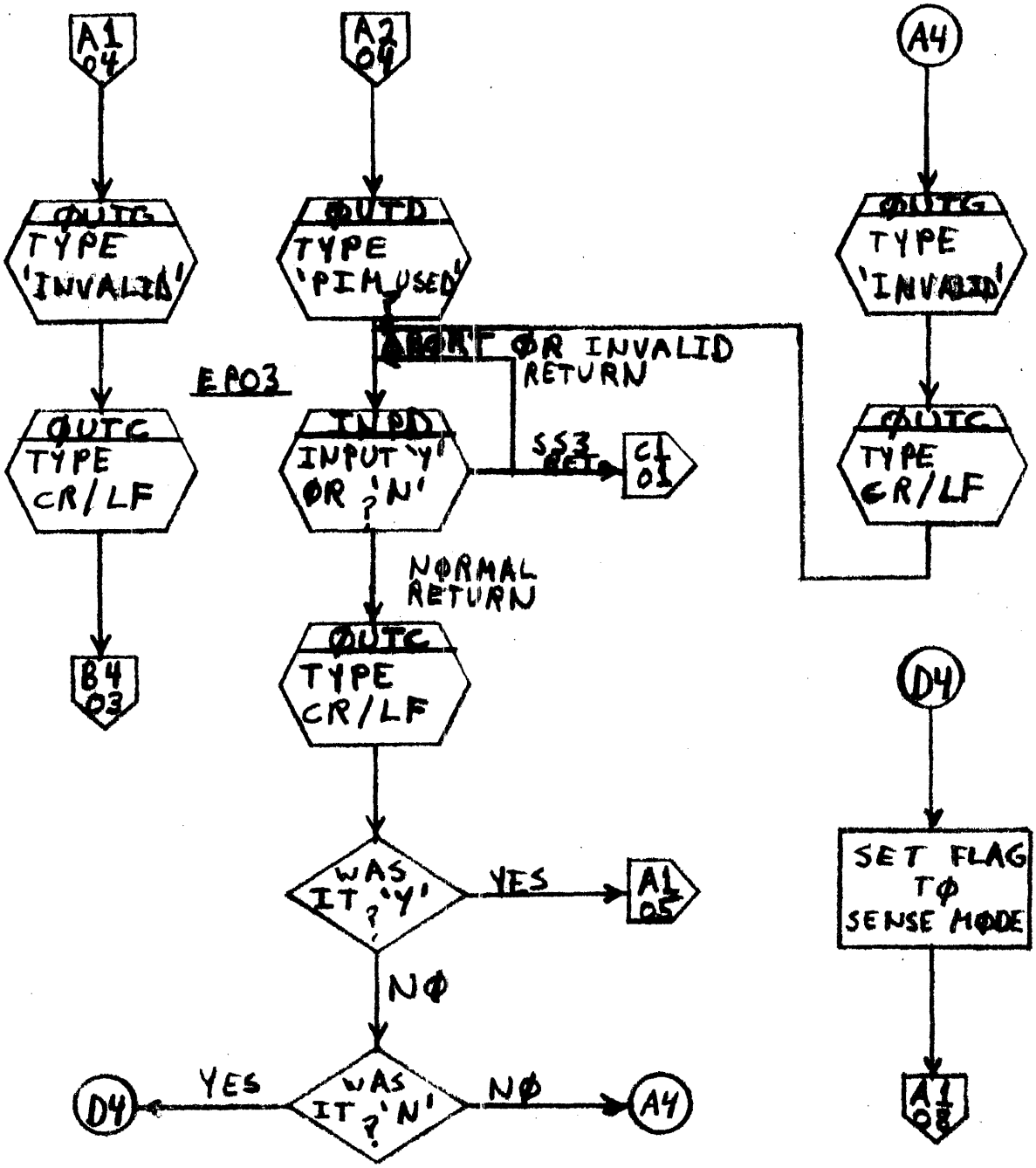


varian data machines a varian subsidiary	CODE IDENT NO. 21101		89A0189 SH 25 OF 95	D REV

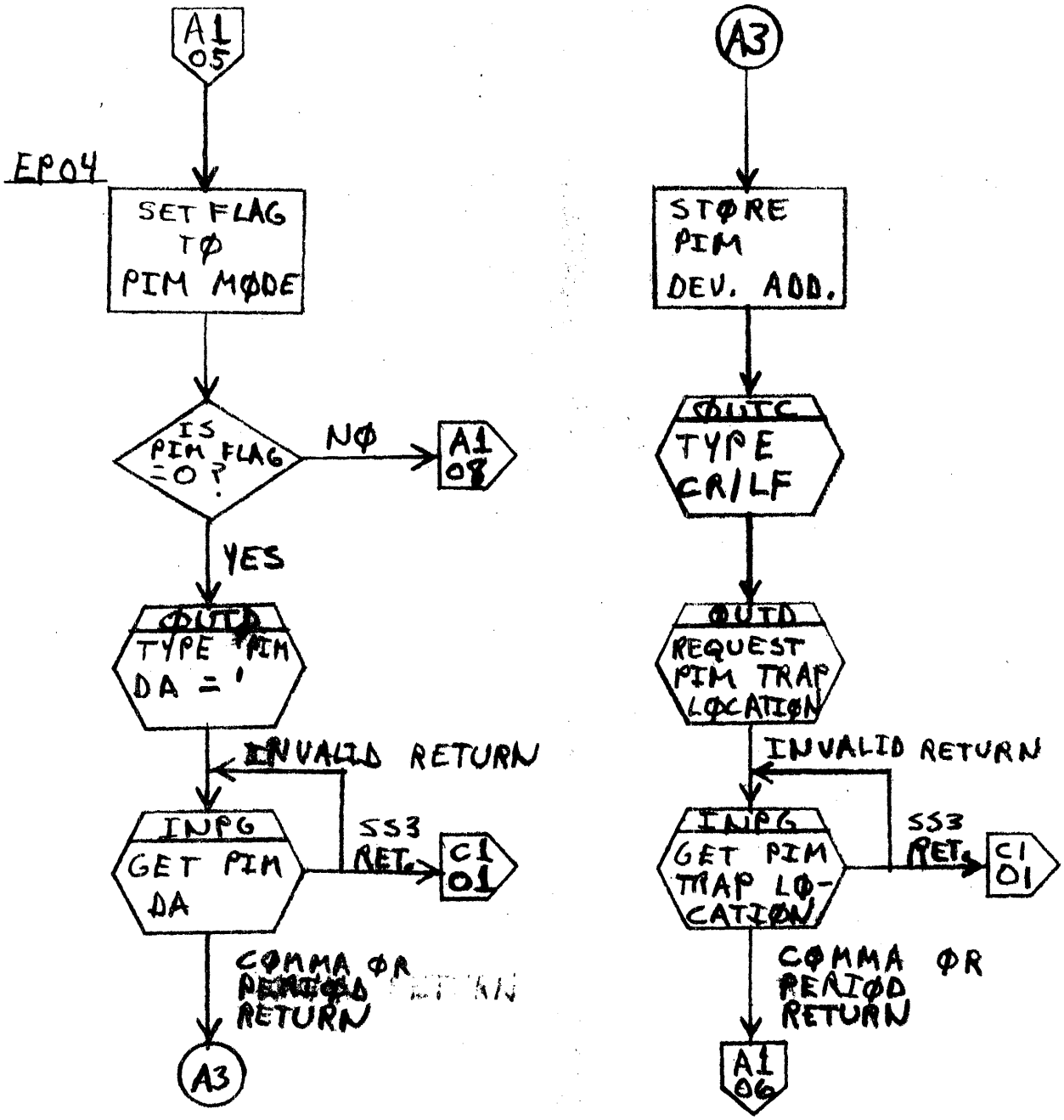
96A0393-000

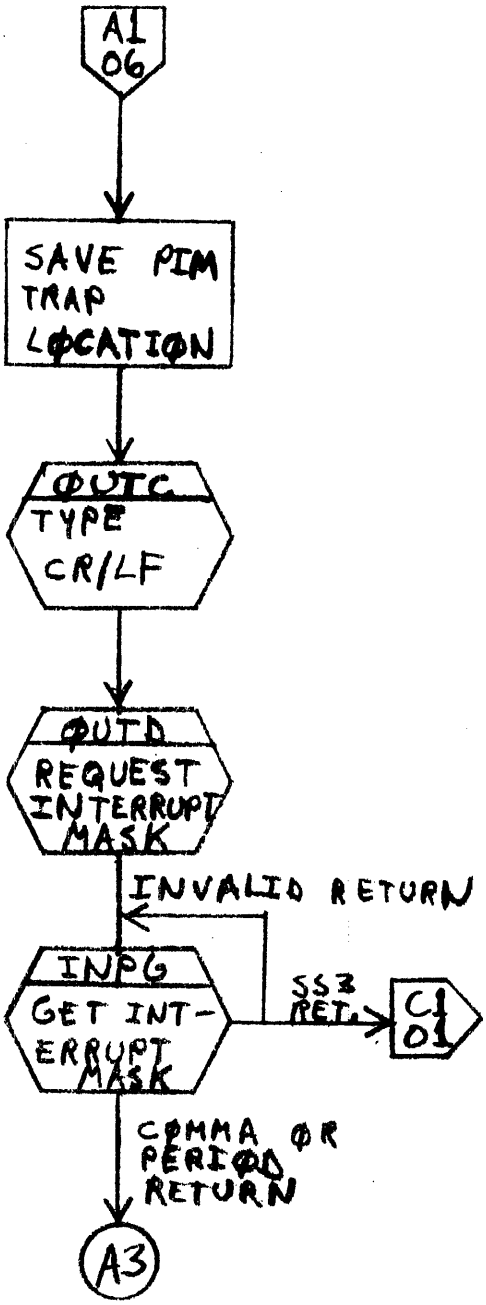

A1 02
ØUTC TYPE CR/LF
ØUTD REQUEST READER DEV. ADD
INVALID INPUT RETURN
INPG GET READER DEV. ADD
553 RET
C1 01
COMMA ØR PERIØD RETURN
STORE READER DEVICE ADDRESS
SET PERIPH. FLAG
A3 02
EP11
A3 02
ØUTC TYPE CR/LF
ØUTD TYPE 'BIC TEST REQUESTED?'
C4 02
INVALID ØR ABØRT RET.
EP02
INPD GET 'Y' ØR 'N'
553 RET.
C1 01
NØRMAL RET.
ØUTC TYPE CR/LF
A1 03

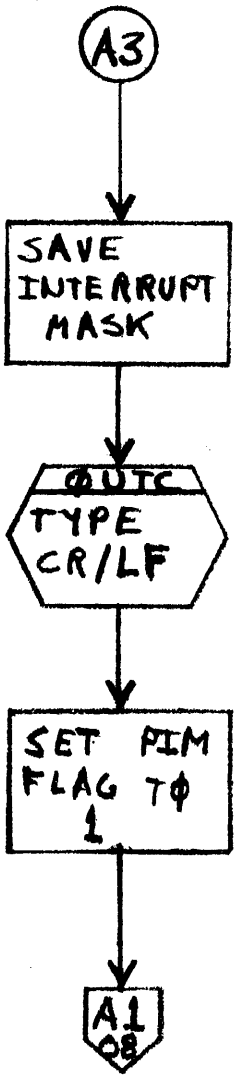

A1 03
WAS IT 'Y'?
YES
A1 45
NØ
WAS IT 'N'?
YES
A3
NØ
ØUTE TYPE 'ERRØR'
ØUTC TYPE CR/LF
C4 02
A3
ØUTD TYPE 'BIC TØ BE USED?'
B4 03
ABØRT ØR INVALID RET.
EP09
INPD GET 'Y' ØR 'N'
SS3 RET.
C1 01
NØRMAL RETURN
ØUTC TYPE CR/LF
WAS IT 'Y'?
YES
A1 07
NØ
WAS IT 'N'?
NØ
A1 04
YES
A1 04

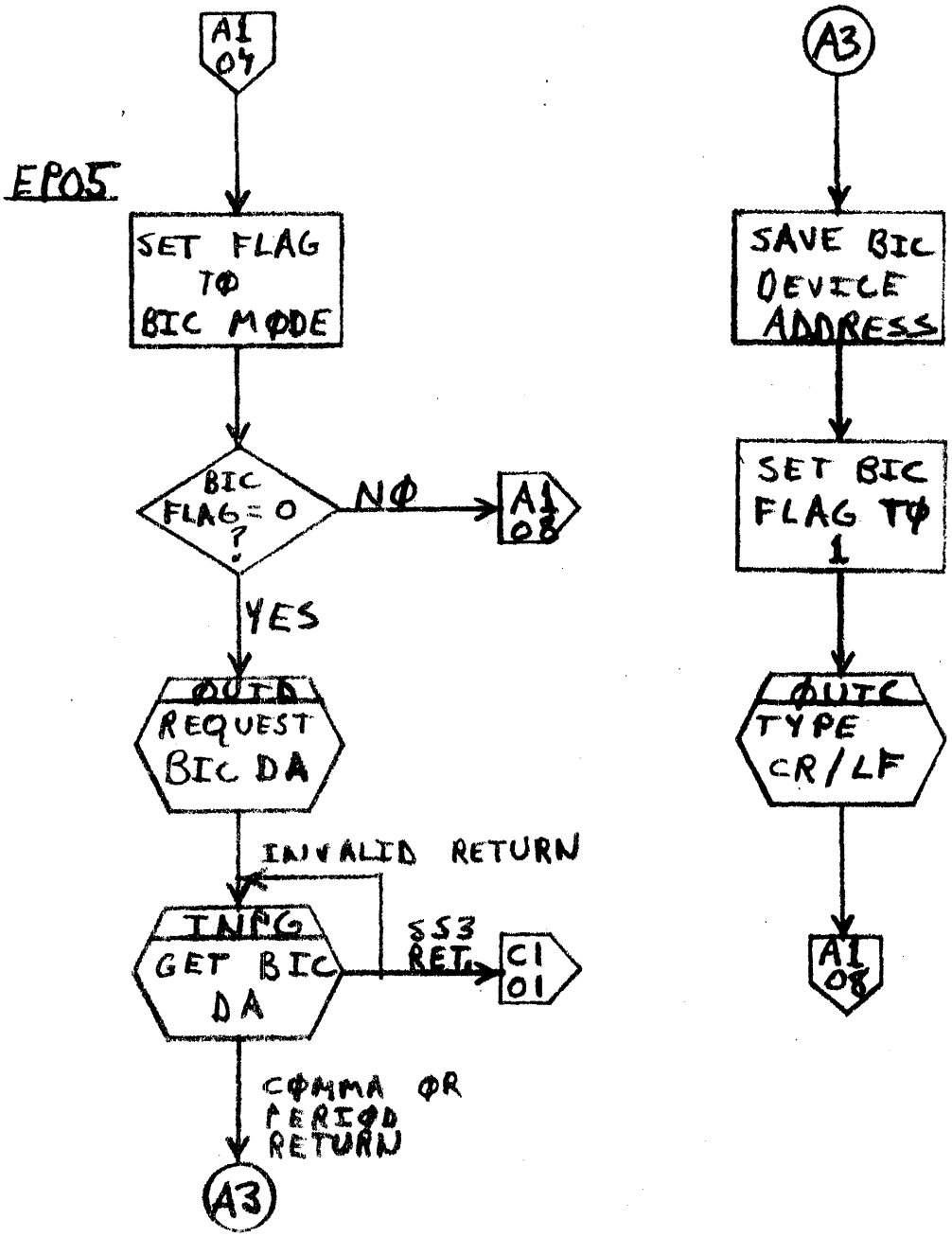


varian data machines a varian subsidiary	CODE IDENT NO. 21101		89A0189 SH 28 OF 95	D REV

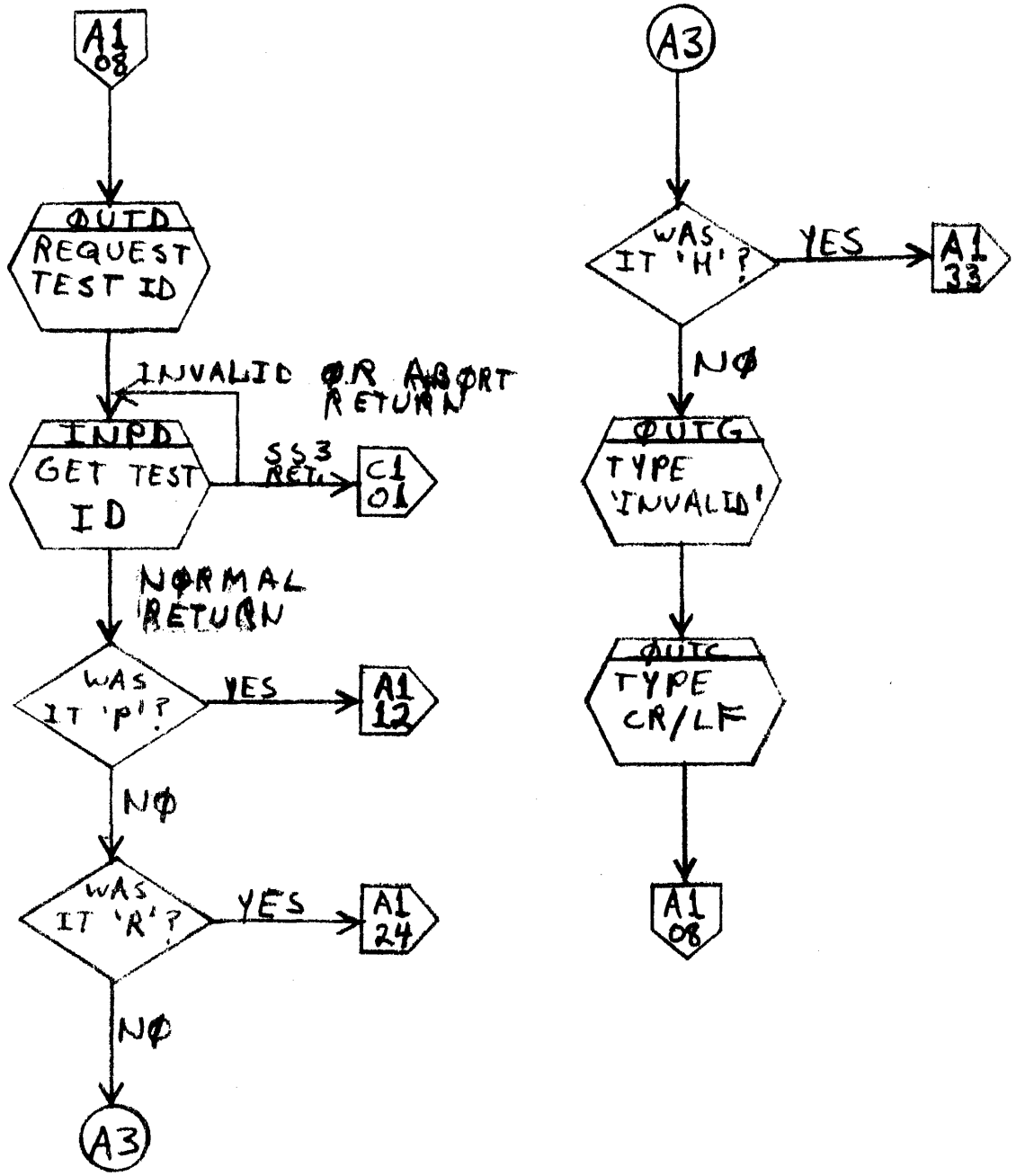

A1 05
EP04
SET FLAG TØ PIM MØDE
IS PIM FLAG =0 ?
NØ
A1 08
YES
ØUTC TYPE PIM DA = '
INVALID RETURN
INPG GET PIM DA
SS3 RET
C1 01
COMMA ØR PERIØD RETURN
A3
A3
STØRE PIM DEV. ADD.
ØUTC TYPE CR/LF
ØUTC REQUEST PIM TRAP LØCATIØN
INVALID RETURN
INPG GET PIM TRAP LØCATIØN
SS3 RET
C1 01
COMMA ØR PERIØD RETURN
A1 06

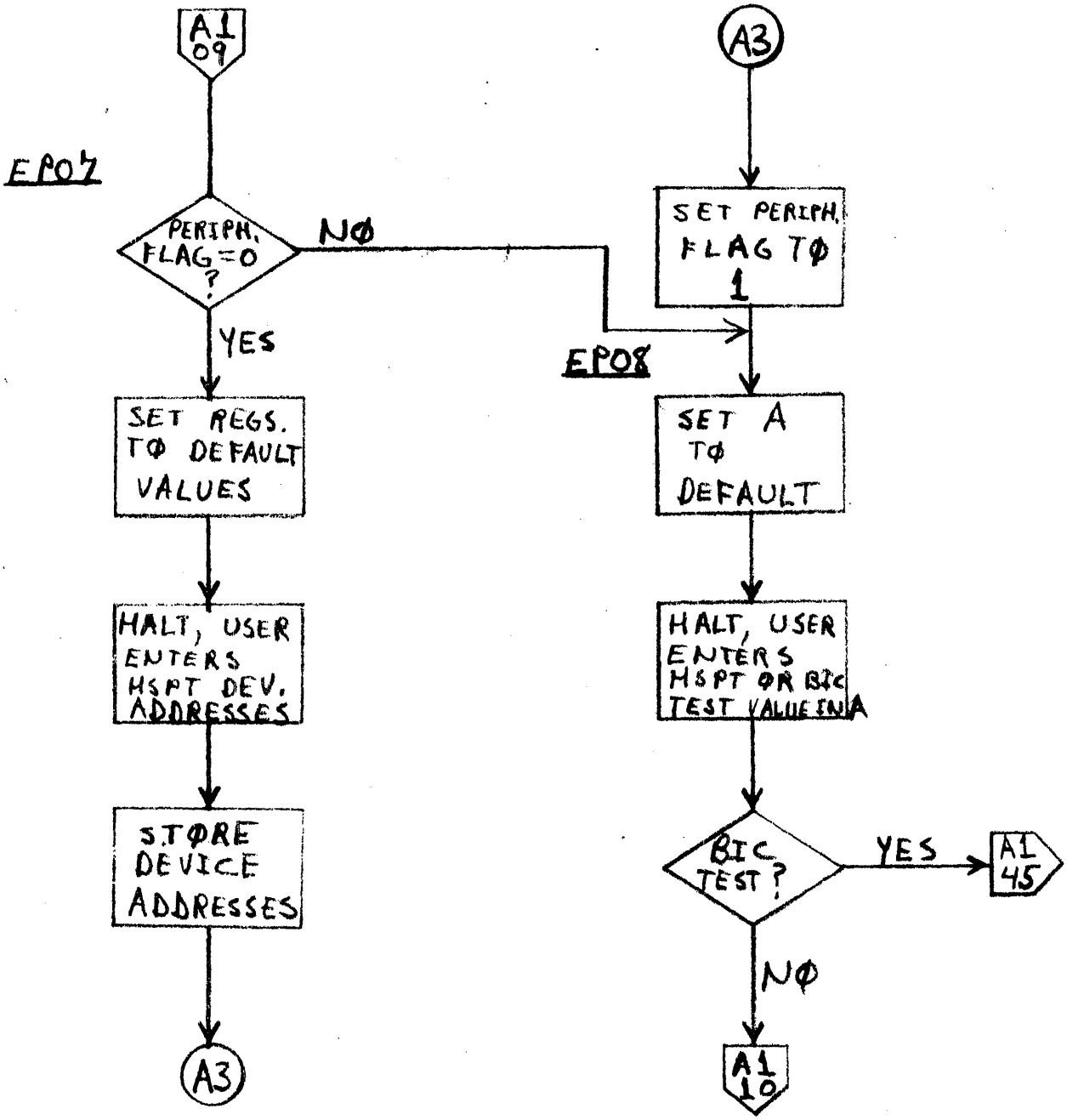

A1
06
SAVE PIM
TRAP
LOCATION
OUTC
TYPE
CR/LF
OUTO
REQUEST
INTERRUPT
MASK
INVALID RETURN
INPG
GET INT-
ERRUPT
MASK
SS3
RET.
C1
01
COMMA OR
PERIOD
RETURN
A3

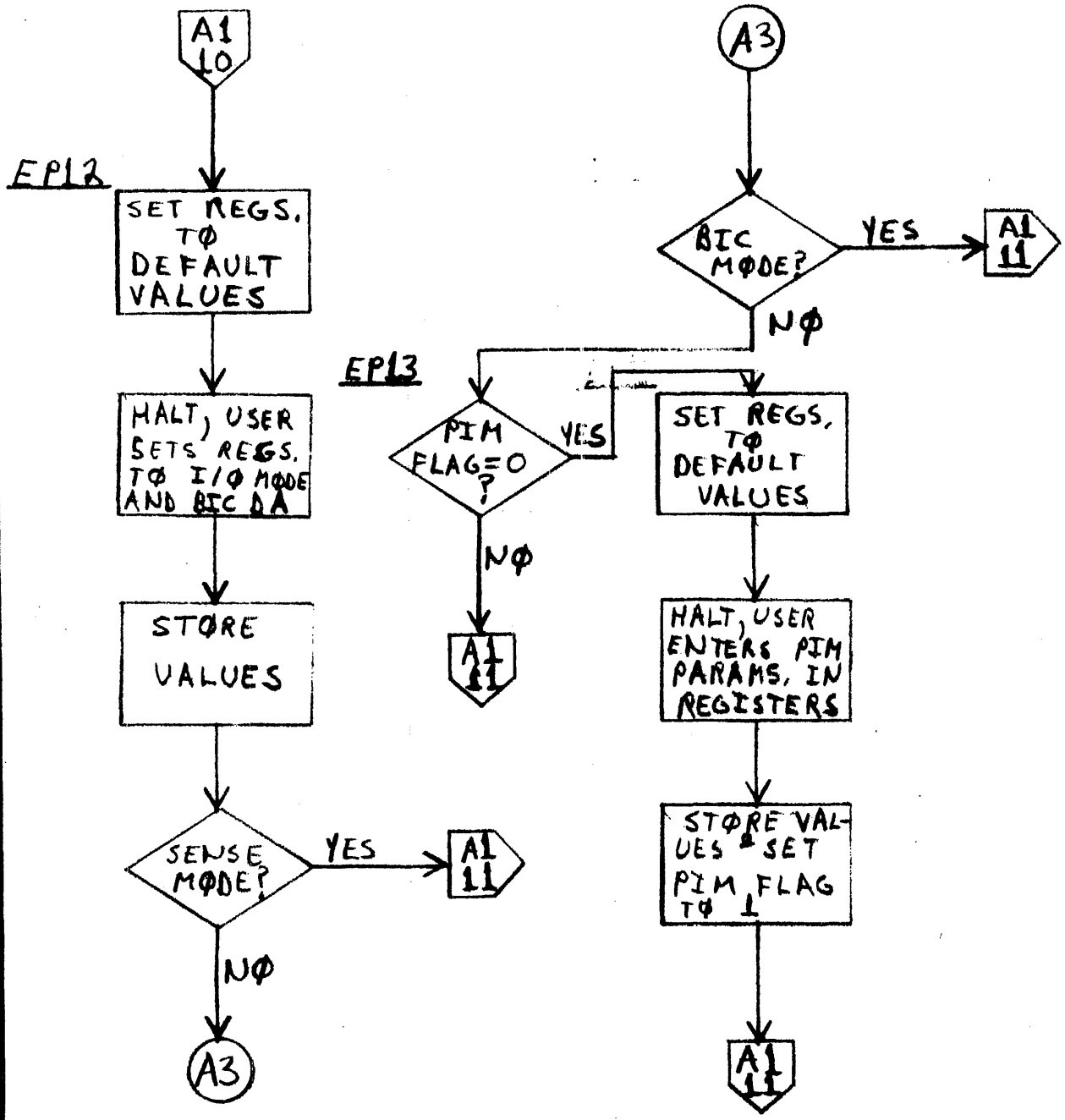

A3
SAVE
INTERRUPT
MASK
OUTC
TYPE
CR/LF
SET PIM
FLAG TO
1
A1
08

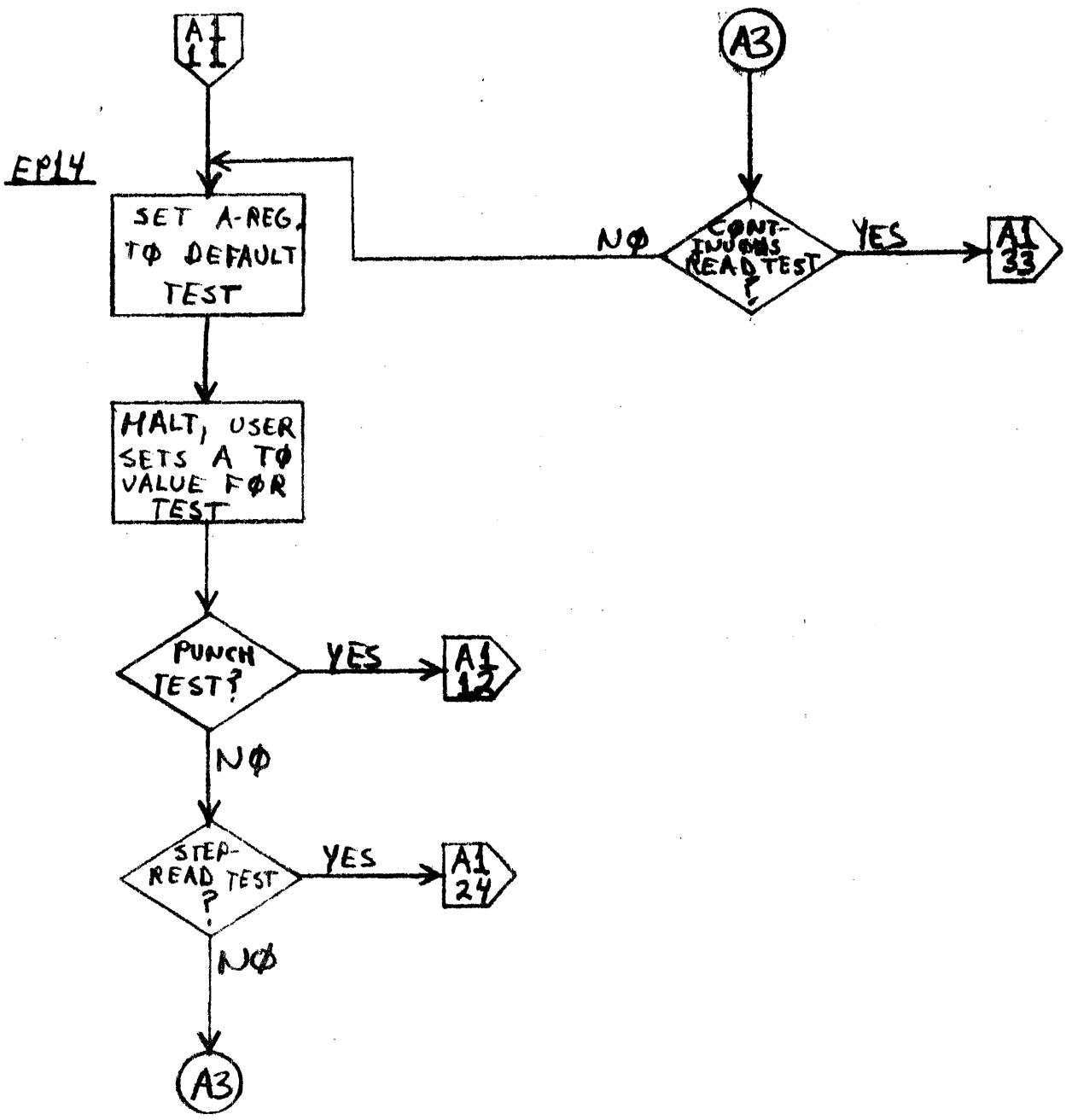

AI 04
EP05
SET FLAG TO BIC MODE
BIC FLAG = 0 ?
NO
AI 08
YES
QUID
REQUEST BIC DA
INVALID RETURN
INPG
GET BIC DA
SS3 RET
CI 01
COMMA OR PERIOD RETURN
A3
A3
SAVE BIC DEVICE ADDRESS
SET BIC FLAG TO 1
QUIC
TYPE CR/LF
AI 08

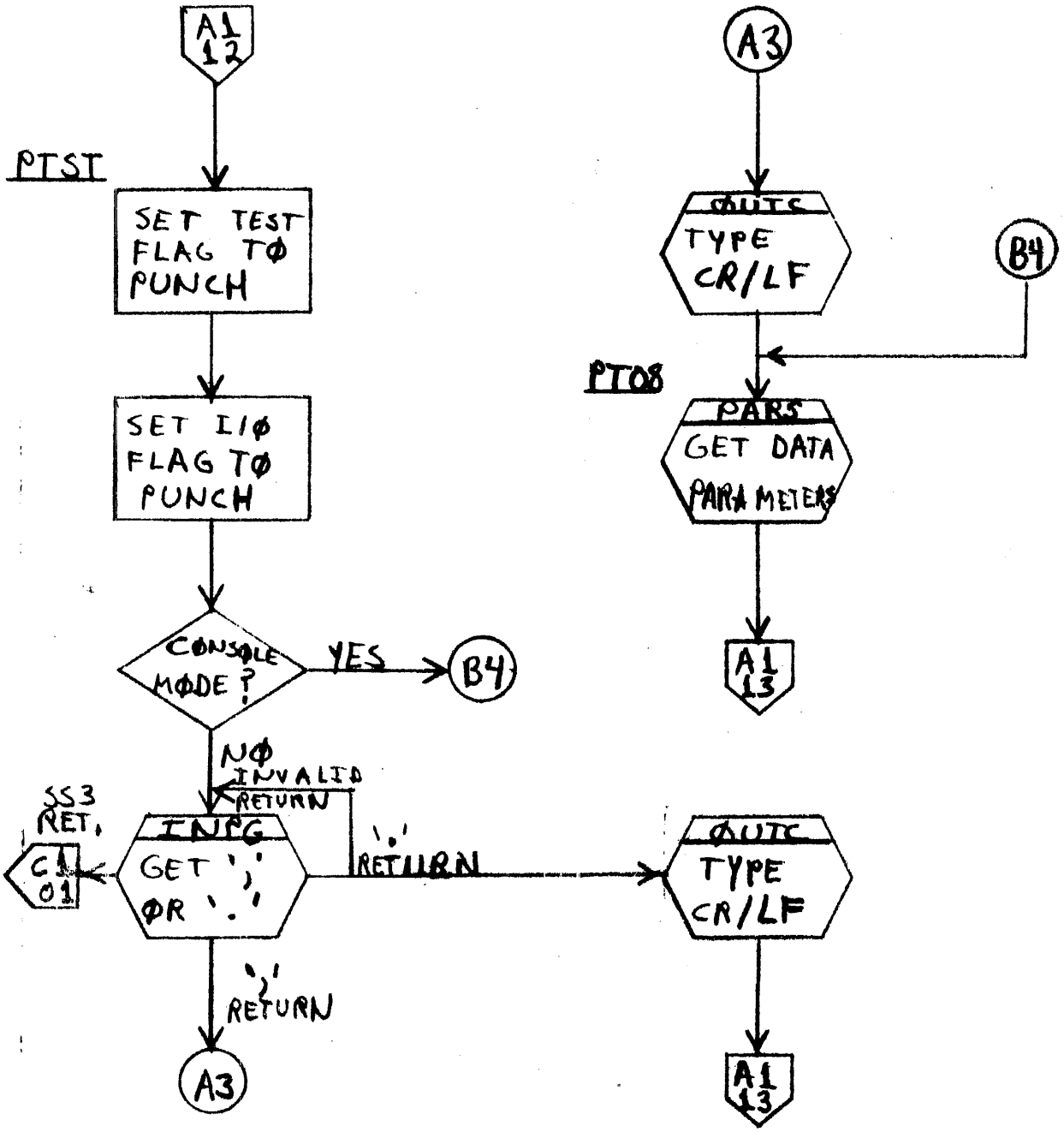
EP06

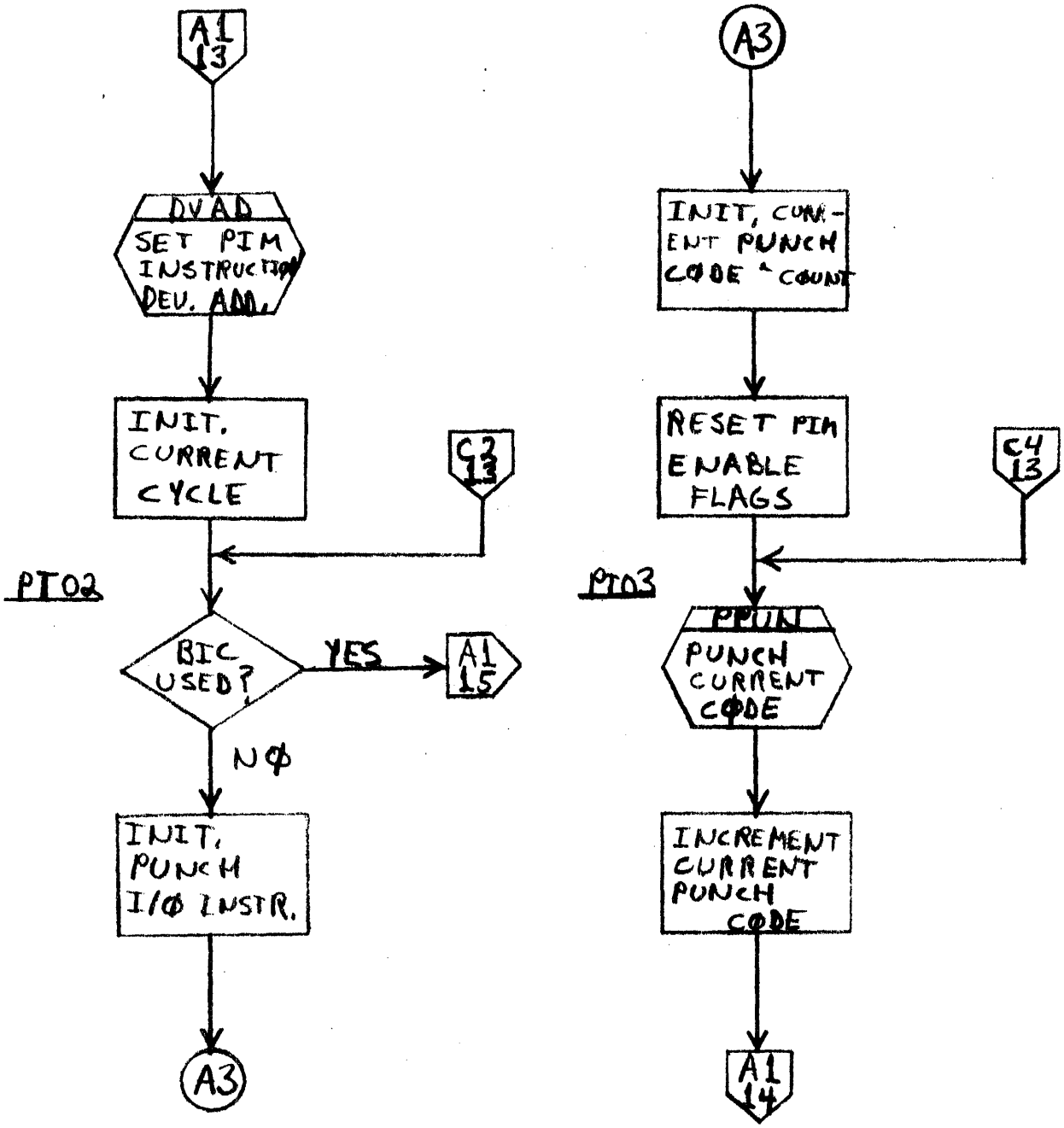

A1 08
ØUTD
REQUEST TEST ID
INVALID ØR ABØRT RETURN
INPD
GET TEST ID
SS3 RET
C1 01
NØRMAL RETURN
WAS IT 'P'?
YES
A1 12
NØ
WAS IT 'R'?
YES
A1 24
NØ
A3
A3
WAS IT 'H'?
YES
A1 33
NØ
ØUTG
TYPE 'INVALID'
ØUTC
TYPE CR/LF
A1 08

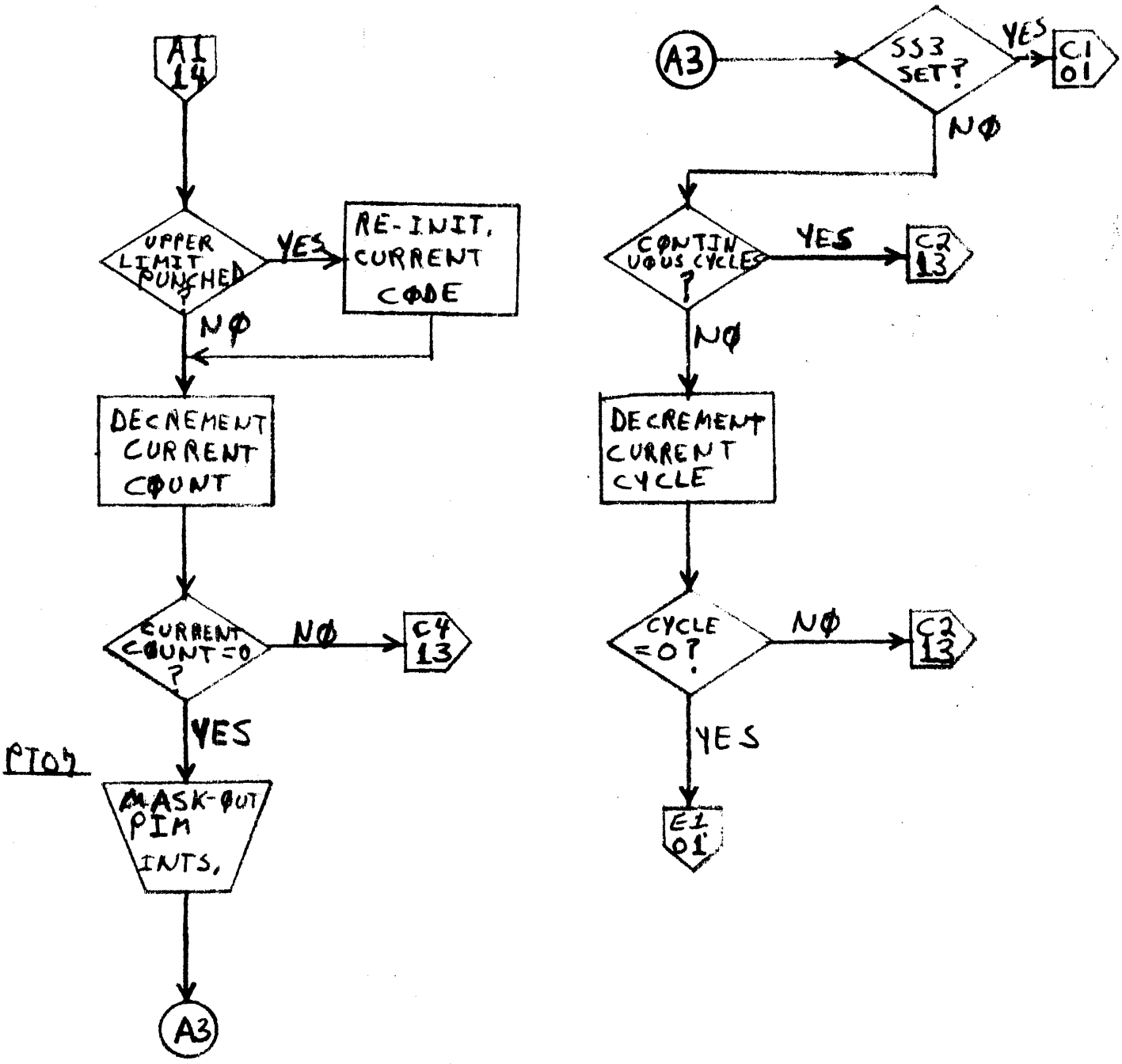

A1
09
EP07
PERIPH. FLAG=0 ?
NØ
YES
SET REGS. TØ DEFAULT VALUES
HALT, USER ENTERS HSPT DEV. ADDRESSES
STØRE DEVICE ADDRESSES
A3
A3
SET PERIPH. FLAG TØ 1
EP08
SET A TØ DEFAULT
HALT, USER ENTERS HSPT ØR BIC TEST VALUE IN A
BIC TEST ?
YES
A1
45
NØ
A1
10

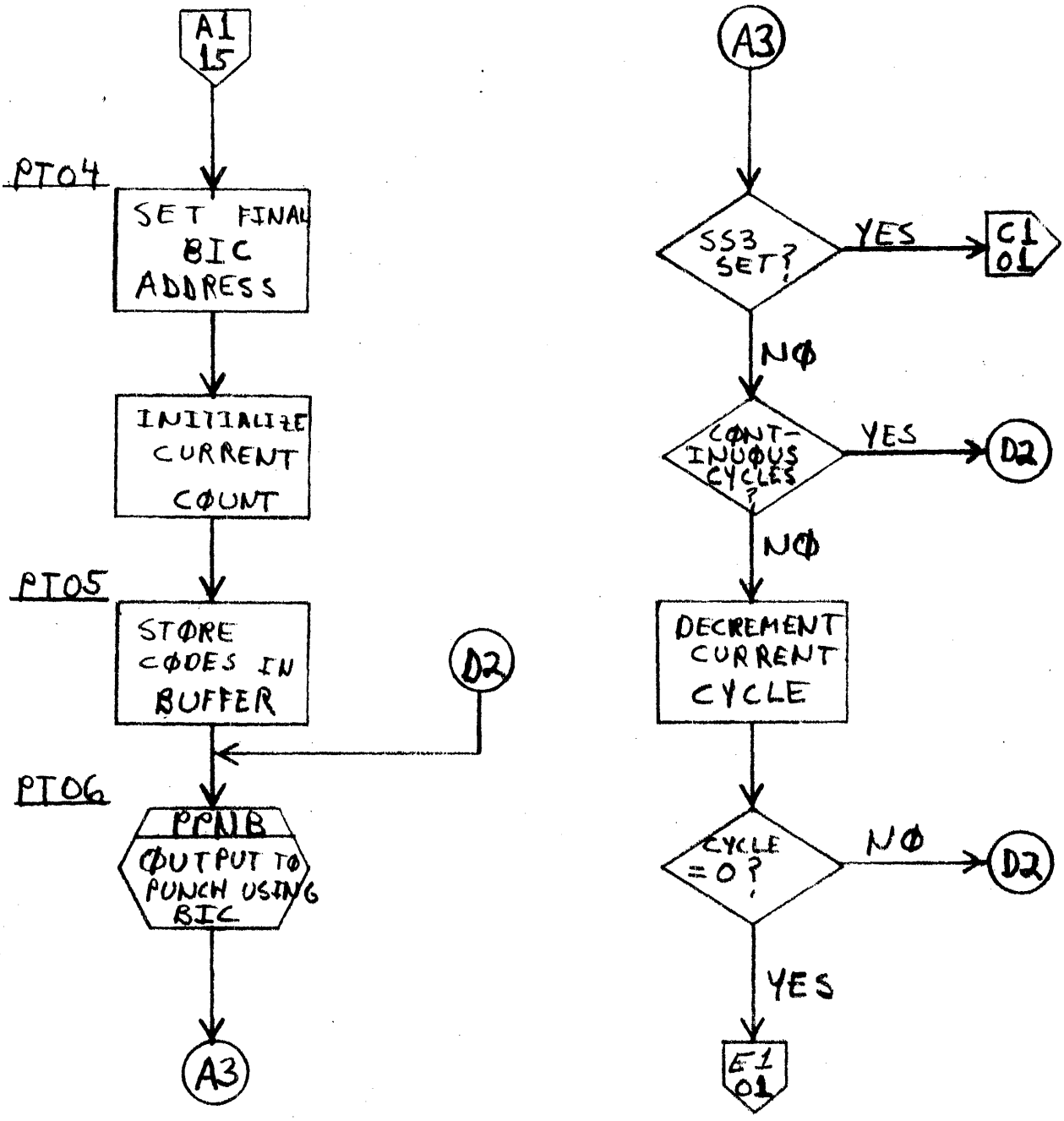

A1 10
EP12
SET REGS. TØ DEFAULT VALUES
HALT, USER SETS REGS. TØ I/Ø MØDE AND BIC DA
STØRE VALUES
SENSE MØDE?
YES
A1 11
NØ
A3
A3
BIC MØDE?
YES
A1 11
NØ
EP13
PIM FLAG=0 ?
YES
NØ
A1 11
SET REGS, TØ DEFAULT VALUES
HALT, USER ENTERS PIM PARAMS. IN REGISTERS
STØRE VALUES & SET PIM FLAG TØ 1
A1 11


A1 11
A3
EP14
SET A-REG TO DEFAULT TEST
NO
CONT-INUOUS READ TEST ?
YES
A1 33
HALT, USER SETS A TO VALUE FOR TEST
PUNCH TEST?
YES
A1 12
NO
STEP-READ TEST ?
YES
A1 24
NO
A3

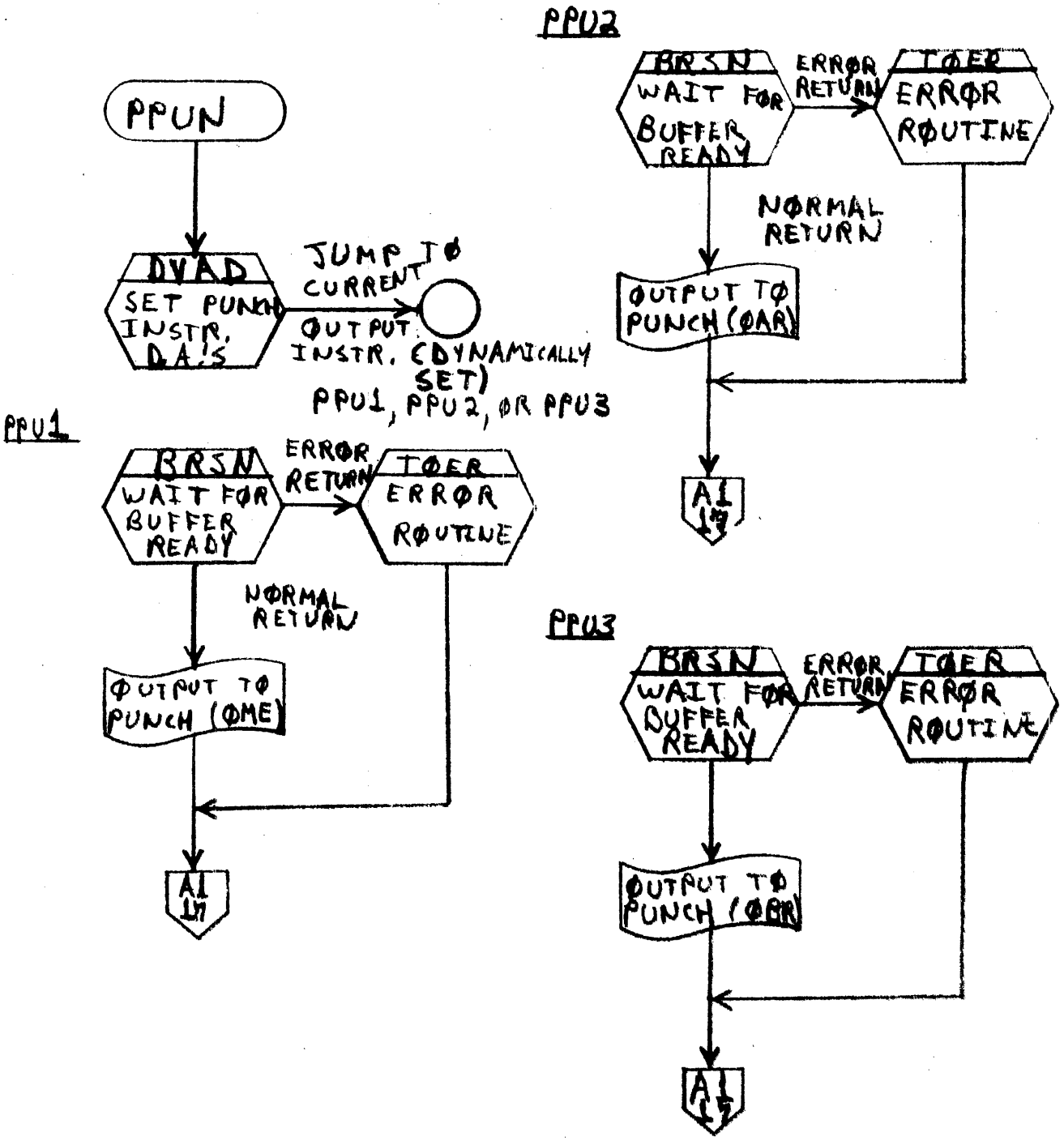

A1 12
PTST
SET TEST FLAG TØ PUNCH
SET I/Ø FLAG TØ PUNCH
CONSOLE MØDE ?
YES
B4
NØ
INVALID
RETURN
SS3 RET.
C1 01
INPG
GET ',' ØR '.'
RETURN
A3
A3
ØUTS
TYPE CR/LF
B4
PTØS
PARS
GET DATA PARAMETERS
A1 13
ØUTC
TYPE CR/LF
A1 13

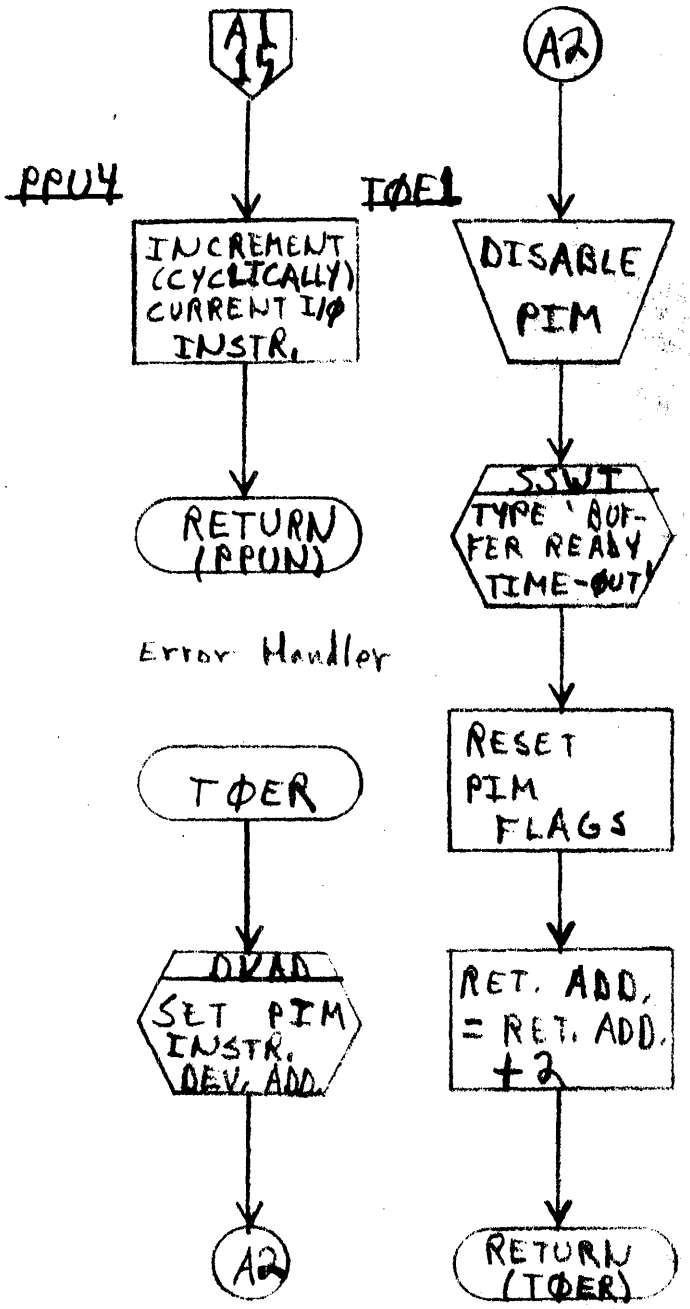

A1
13
DVAD
SET PIM
INSTRUCTION
DEV. ADD.
INIT.
CURRENT
CYCLE
C2
13
PT02
BIC
USED?
YES
A1
15
NO
INIT.
PUNCH
I/O INSTR.
A3
A3
INIT, CURR-
ENT PUNCH
CODE & COUNT
RESET PIM
ENABLE
FLAGS
C4
13
PT03
PPUN
PUNCH
CURRENT
CODE
INCREMENT
CURRENT
PUNCH
CODE
A1
14


A1
14
UPPER LIMIT PUNCHED ?
YES
RE-INIT. CURRENT CODE
NO
DECREMENT CURRENT COUNT
CURRENT COUNT=0 ?
NO
C4
13
YES
PIOT
MASK-OUT PIM INTS.
A3
A3
SSS SET?
YES
C1
01
NO
CONTIN UOUS CYCLES ?
YES
C2
13
NO
DECREMENT CURRENT CYCLE
CYCLE =0?
NO
C2
13
YES
E1
01

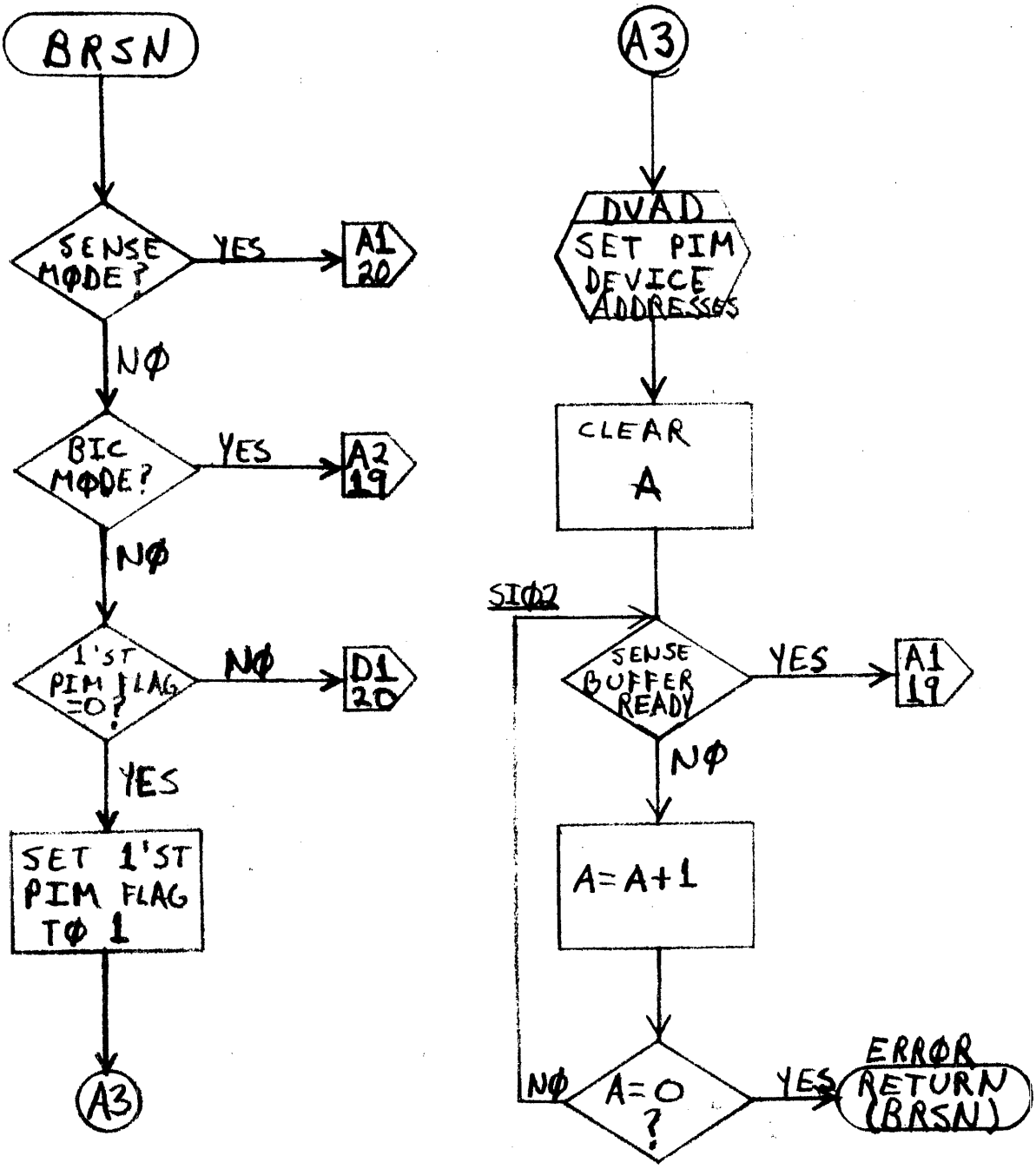

A1
15
PTO4
SET FINAL BIC ADDRESS
INITIALIZE CURRENT COUNT
PTO5
STORE CODES IN BUFFER
D2
PTO6
PCNB
OUTPUT TO PUNCH USING BIC
A3
A3
SS3 SET?
YES
C1
01
NO
CONT-INUOUS CYCLES?
YES
D2
NO
DECREMENT CURRENT CYCLE
CYCLE =0?
NO
D2
YES
E1
01

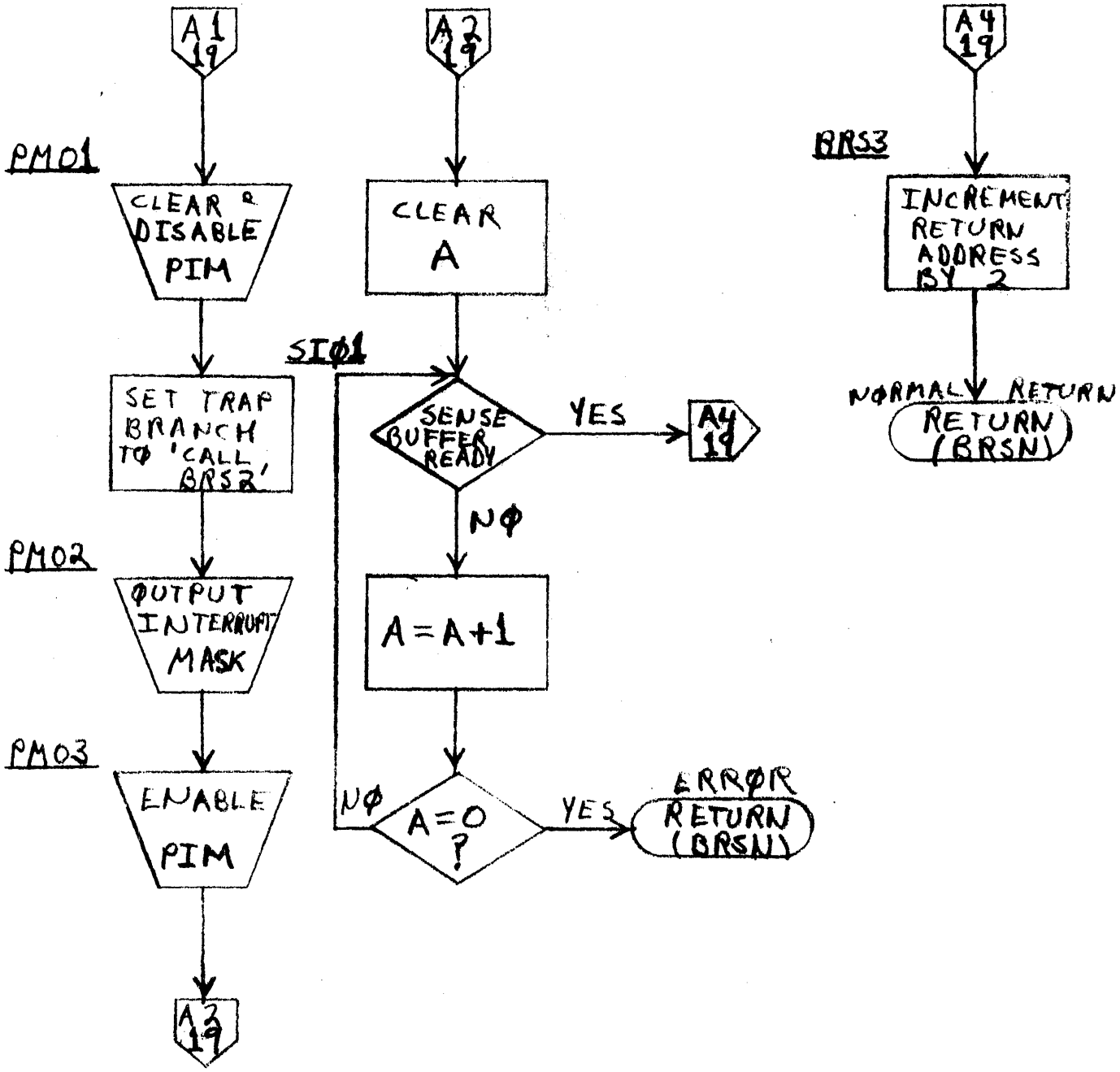
PUNCH (SENSE ØR PIM MØDE)

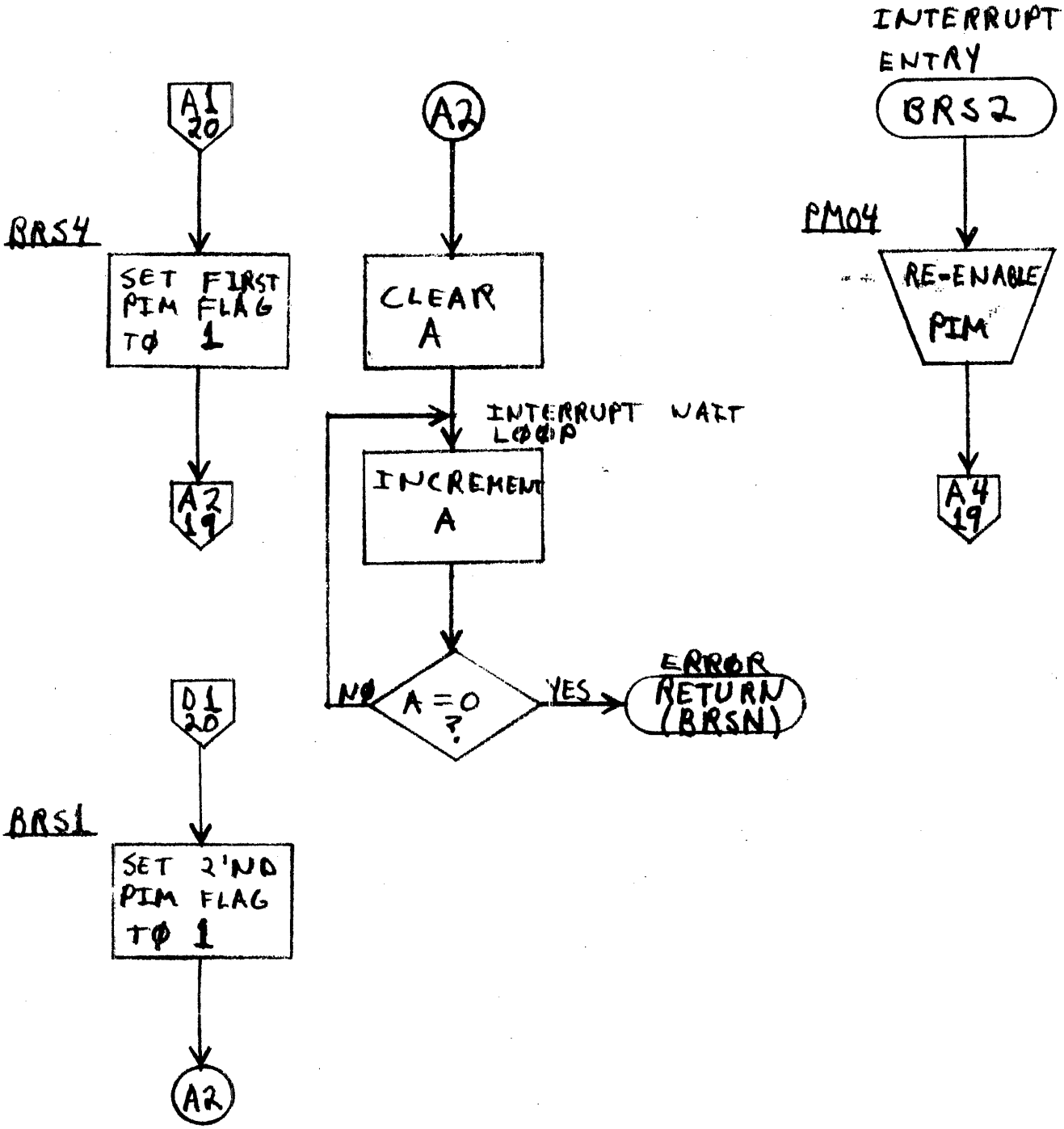



A1
A2
PPU4
INCREMENT (CYCLICALLY) CURRENT I/O INSTR.
RETURN (PPUN)
Error Handler
TOER
DVAD
SET PIM INSTR. DEV. ADD.
A2
IOE1
DISABLE PIM
SSWT
TYPE 'BUFFER READY' TIME-OUT
RESET PIM FLAGS
RET. ADD. = RET. ADD. +2
RETURN (IOER)

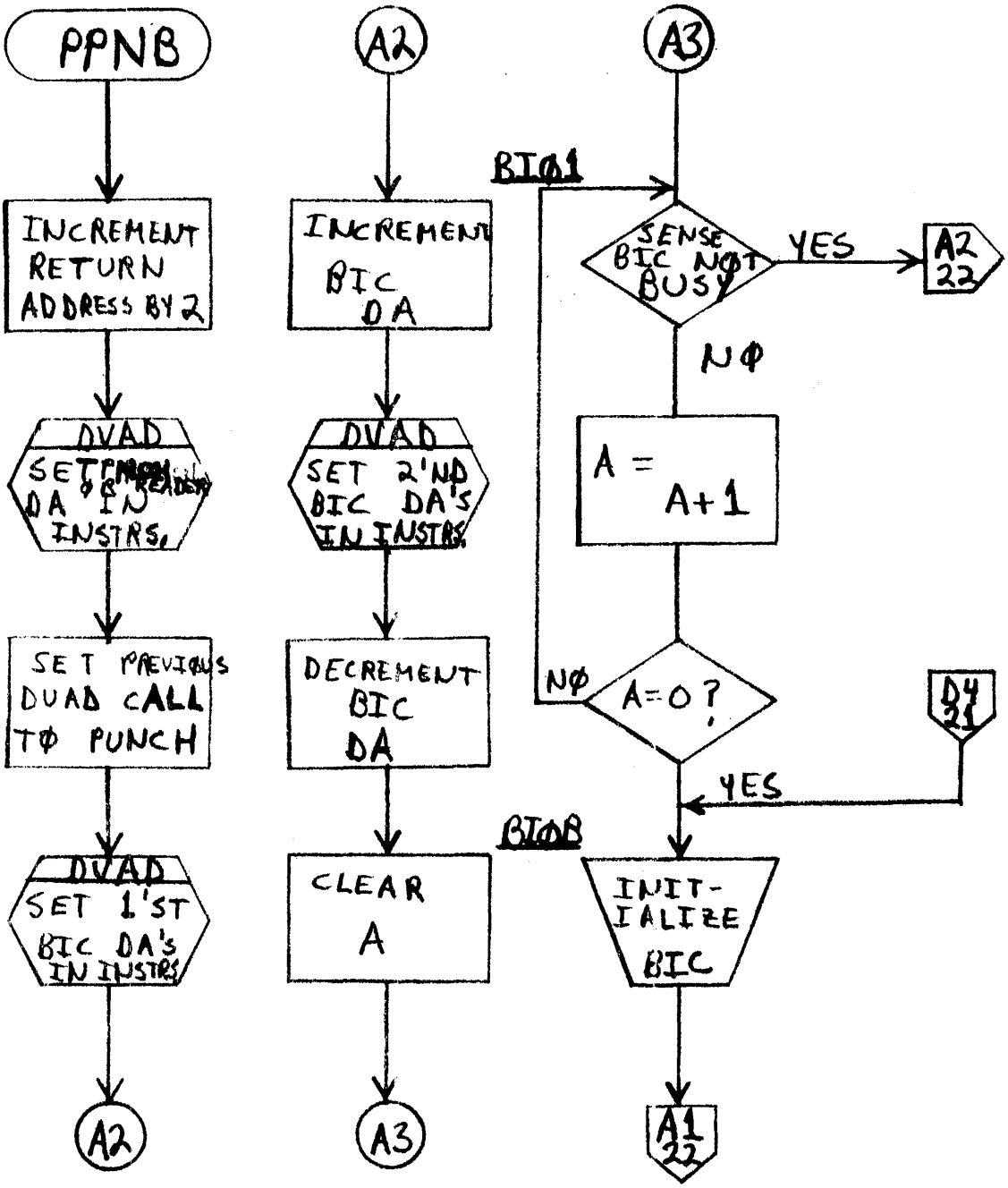
PIM ENABLE/SENSE BUFFER READY ROUTINE

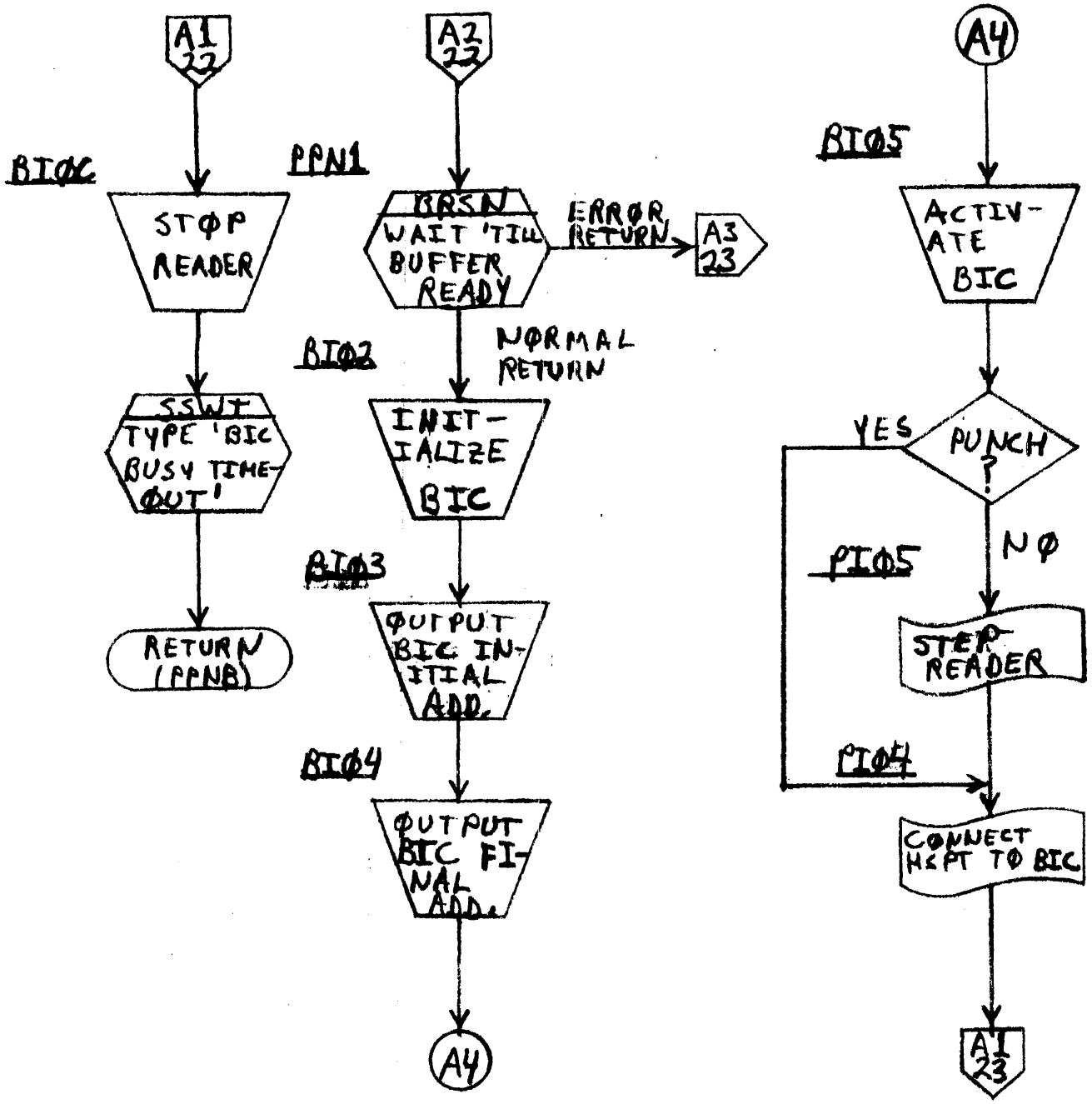


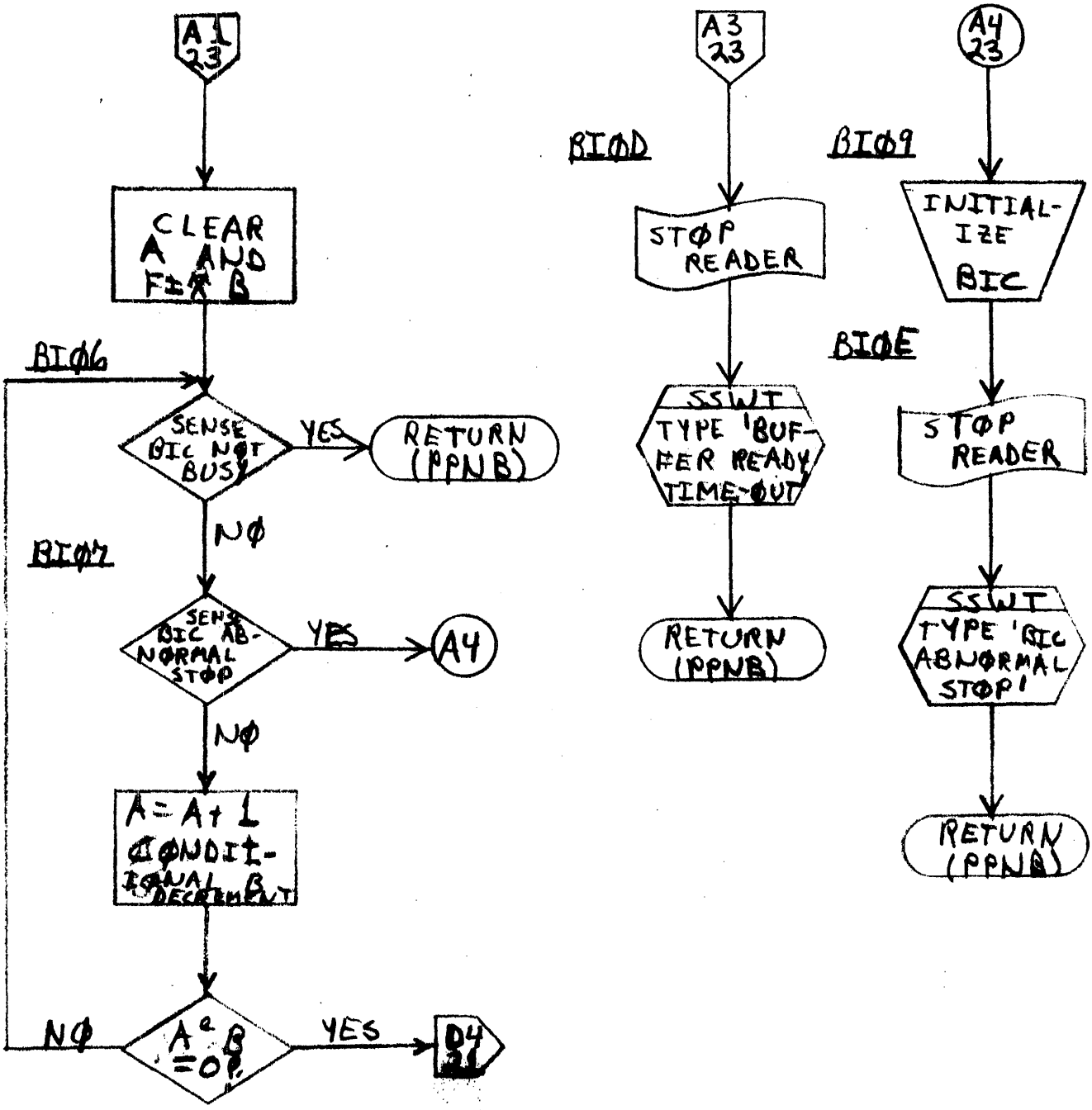

A1 19
A2 19
A4 19
PM01
CLEAR & DISABLE PIM
CLEAR A
BRS3
INCREMENT RETURN ADDRESS BY 2
NORMAL RETURN
RETURN (BRSN)
SI01
SET TRAP BRANCH TO 'CALL BRS2'
SENSE BUFFER READY
YES
A4 19
NO
PM02
OUTPUT INTERRUPT MASK
A=A+1
PM03
ENABLE PIM
NO
A=0 ?
YES
ERROR RETURN (BRSN)
A3 19

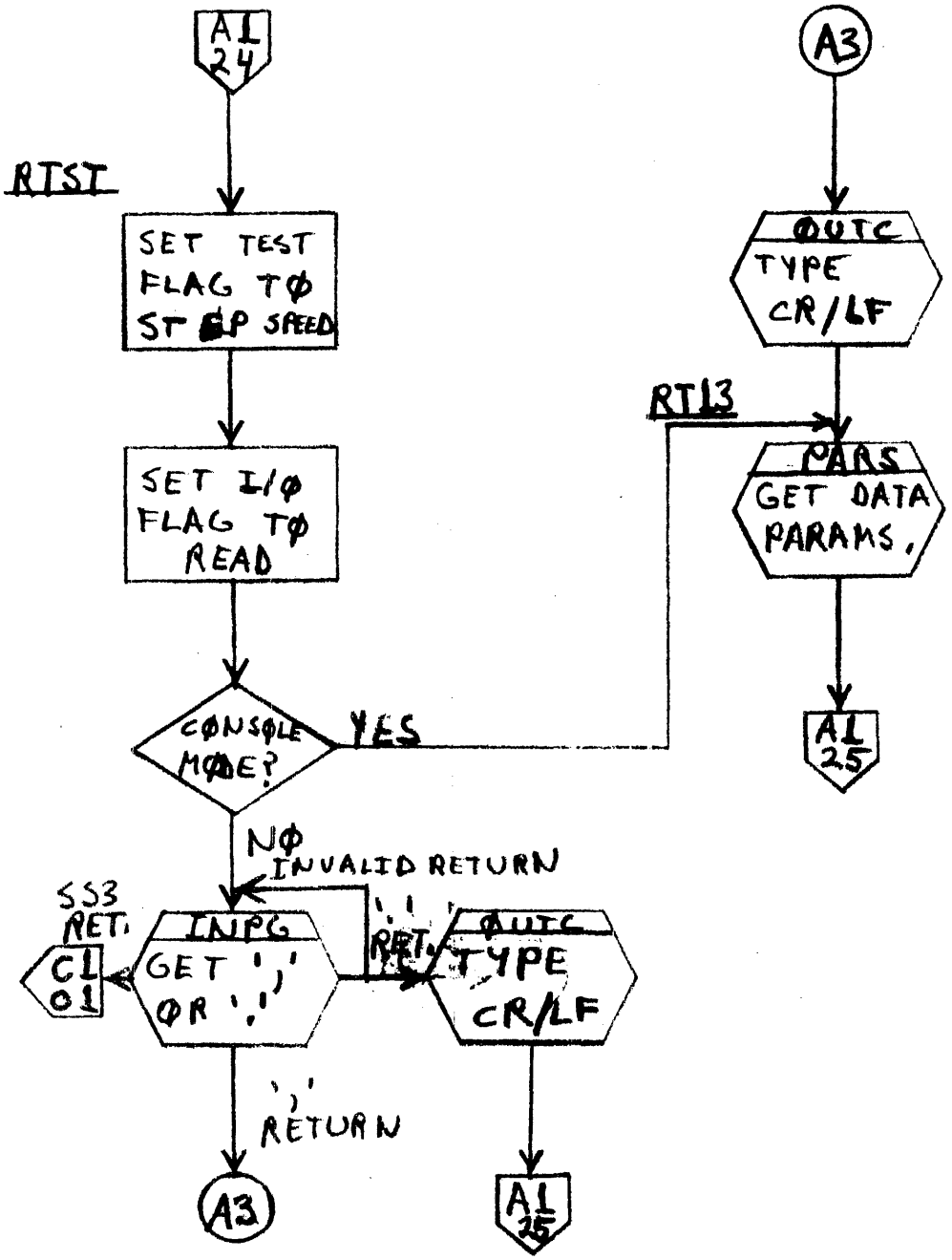

INTERRUPT ENTRY
BRS2
PM04
RE-ENABLE PIM
A4 19
A1 20
BRS4
SET FIRST PIM FLAG TO 1
A2 19
A2
CLEAR A
INTERRUPT WAIT LOOP
INCREMENT A
NO
A = 0 ?
YES
ERROR RETURN (BRSN)
D1 20
BRS1
SET 2'ND PIM FLAG TO 1
A2

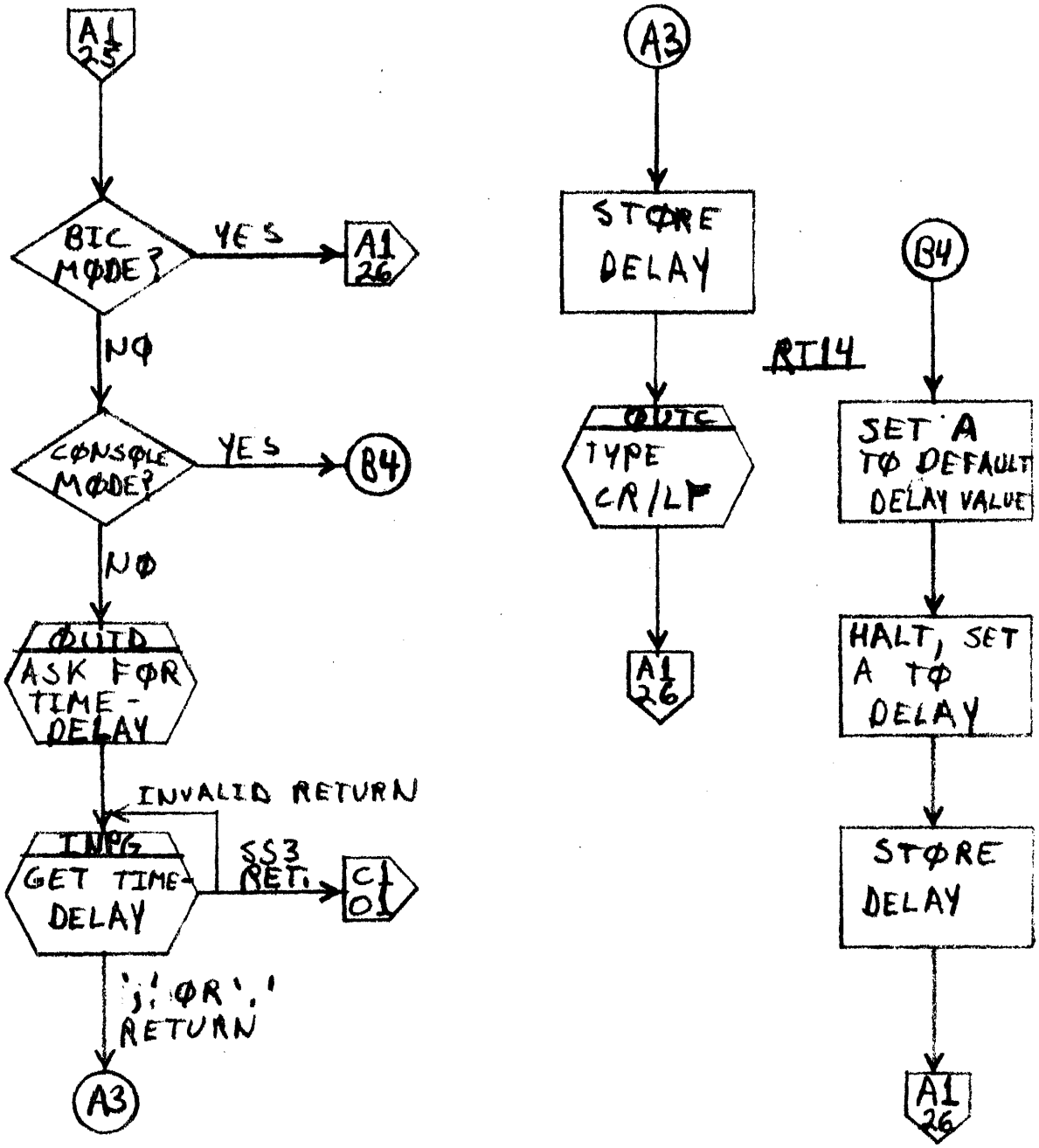
PUNCH (OR READ) (BIC MODE)

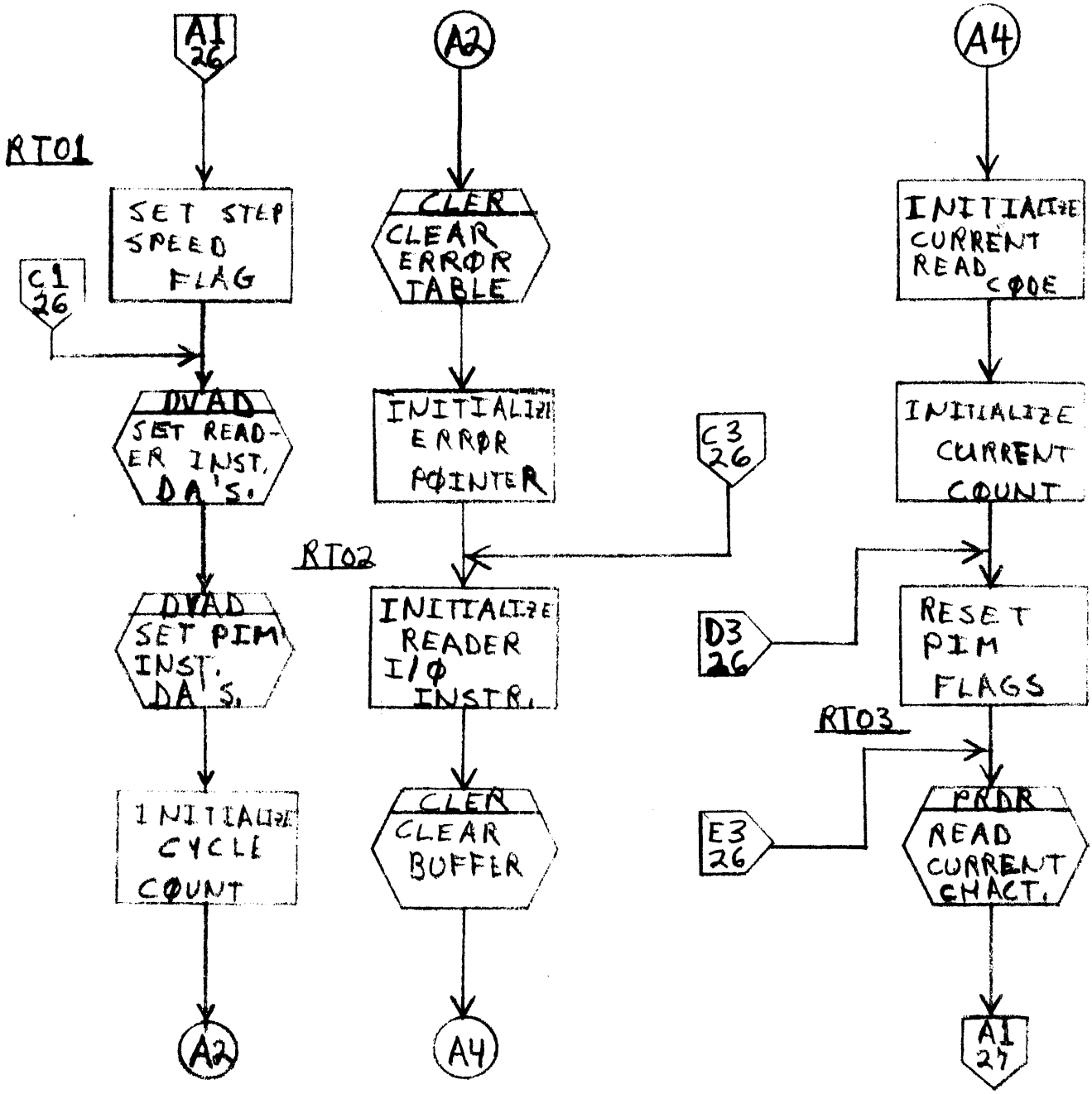



A1 22
A2 22
A4
BIØC
PPN1
BIØ5
STØP READER
BRSN WAIT 'TIL BUFFER READY
ERRØR RETURN
A3 23
ACTIV-ATE BIC
SSWT TYPE 'BIC BUSY TIME-ØUT'
BIØ2
NØRMAL RETURN
INIT-IALIZE BIC
YES
PUNCH ?
PIØ5
NØ
BIØ3
STEP READER
RETURN (PPNB)
ØUTPUT BIC IN-ITIAL ADD.
PIØ4
BIØ4
CONNECT HØPT TØ BIC
ØUTPUT BIC FI-NAL ADD.
A4
A1 23


A1 23
CLEAR A AND FIX B
BIØ6
SENSE BIC NOT BUSY
YES
RETURN (PPNB)
NØ
BIØ7
SENSE BIC AB-NORMAL STOP
YES
A4
NØ
A=A+L CONDIT-IONAL B DECREMENT
A=B ?
NØ
YES
B4
A3 23
BIØD
STOP READER
SSWT TYPE 'BUF-FER READY TIME-OUT
RETURN (PPNB)
A4 23
BIØ9
INITIAL-IZE BIC
BIØE
STOP READER
SSWT TYPE 'BIC ABNORMAL STOP'
RETURN (PPNB)


A1 24
RTST
SET TEST FLAG TØ
ST ØP SPEED
SET I/Ø FLAG TØ READ
CØNSØLE MØDE?
YES
NØ
INVALID RETURN
SS3 RET.
C1 01
INPG
GET ',' ØR '.'
RET.
ØUTC
TYPE CR/LF
',' RETURN
A3
A1 25
A3
ØUTC
TYPE CR/LF
RT13
PARS
GET DATA PARAMS.
A1 25


A1 25
BIC MODE?
YES
A1 26
NO
CONSOLE MODE?
YES
B4
NO
QUIT
ASK FOR TIME-DELAY
INVALID RETURN
INPG
GET TIME-DELAY
SS3 RET.
C1 01
';' OR '.' RETURN
A3
A3
STORE DELAY
QUIT
TYPE CR/LF
A1 26
RT14
B4
SET A TO DEFAULT DELAY VALUE
HALT, SET A TO DELAY
STORE DELAY
A1 26



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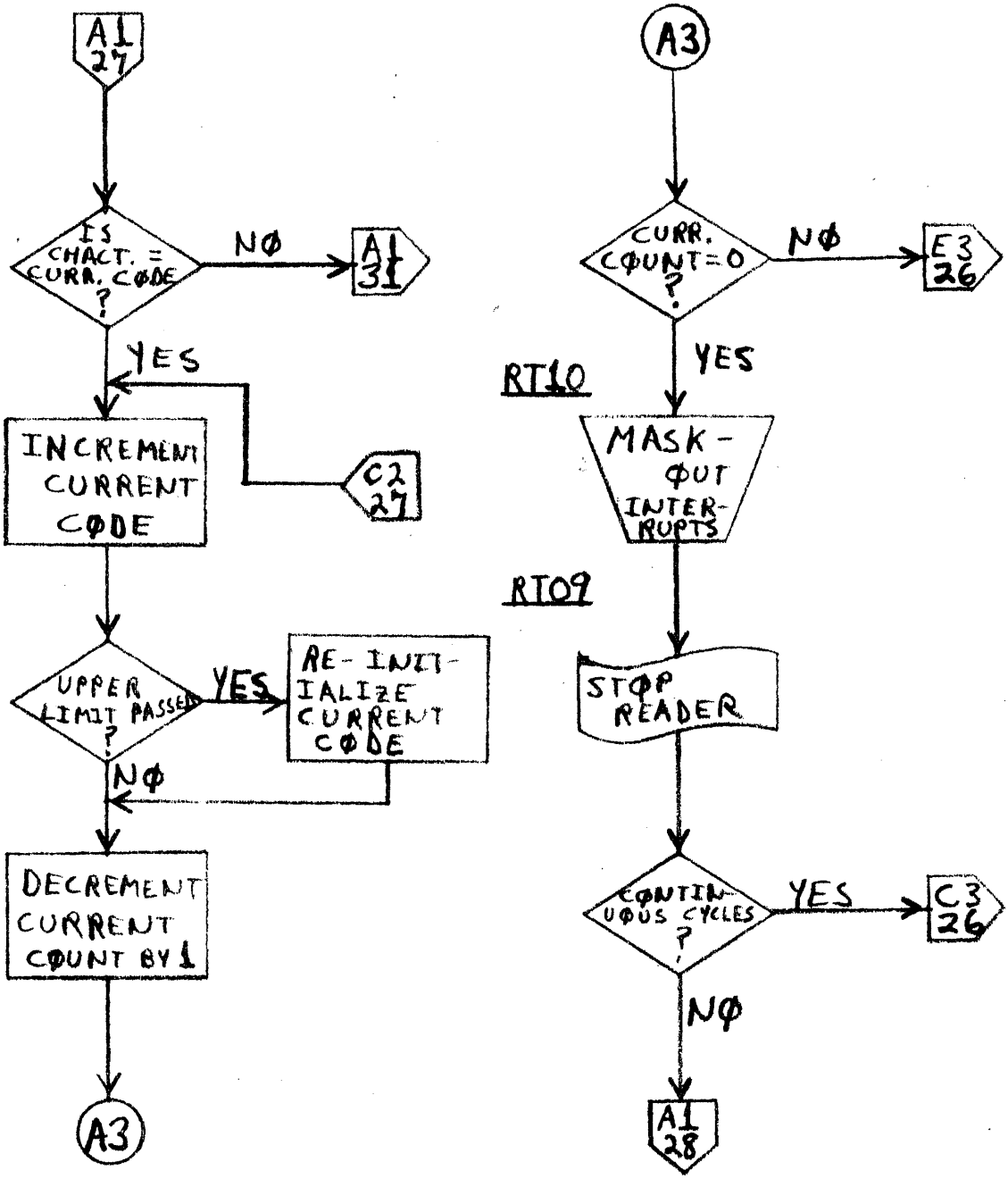
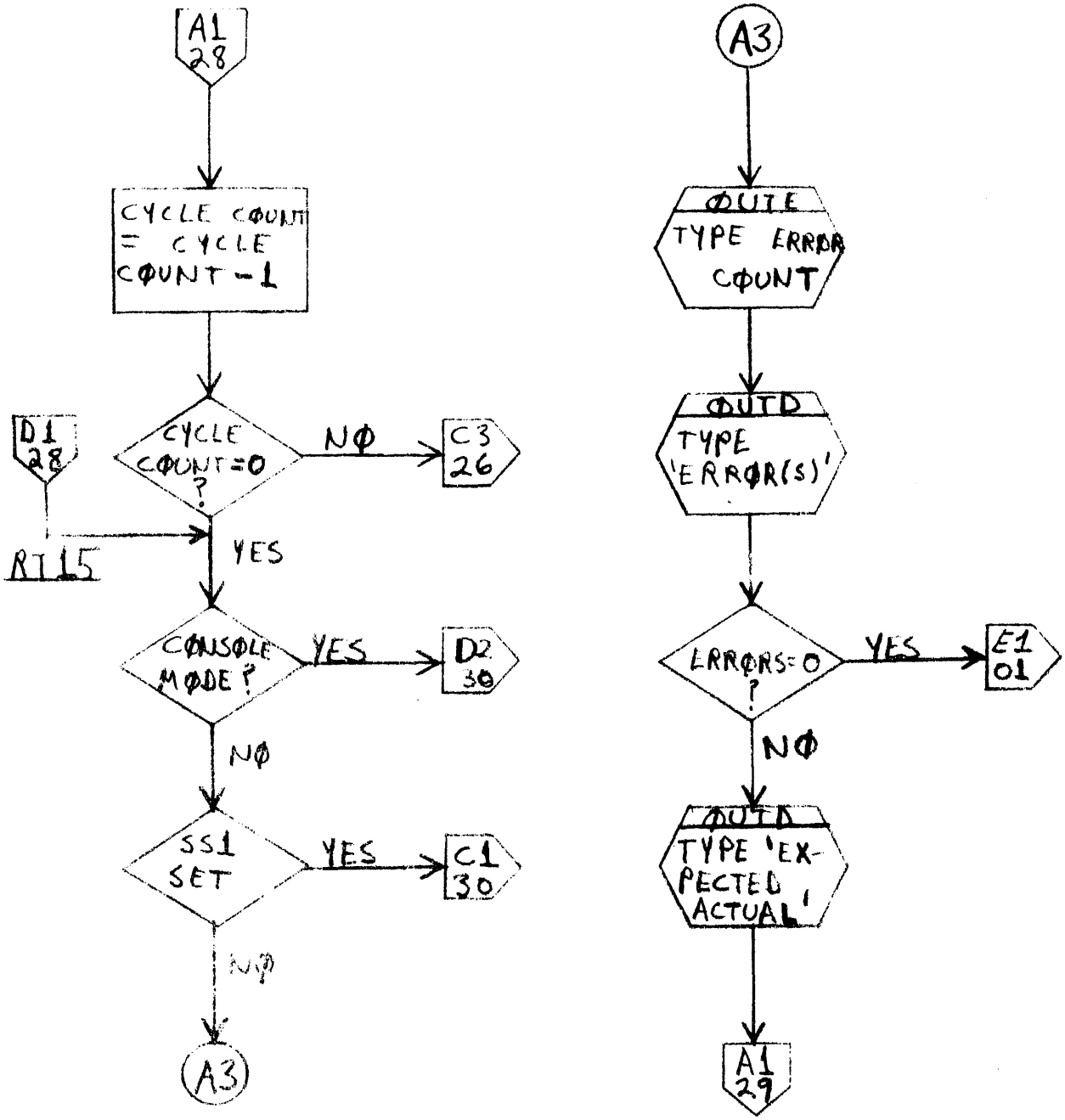
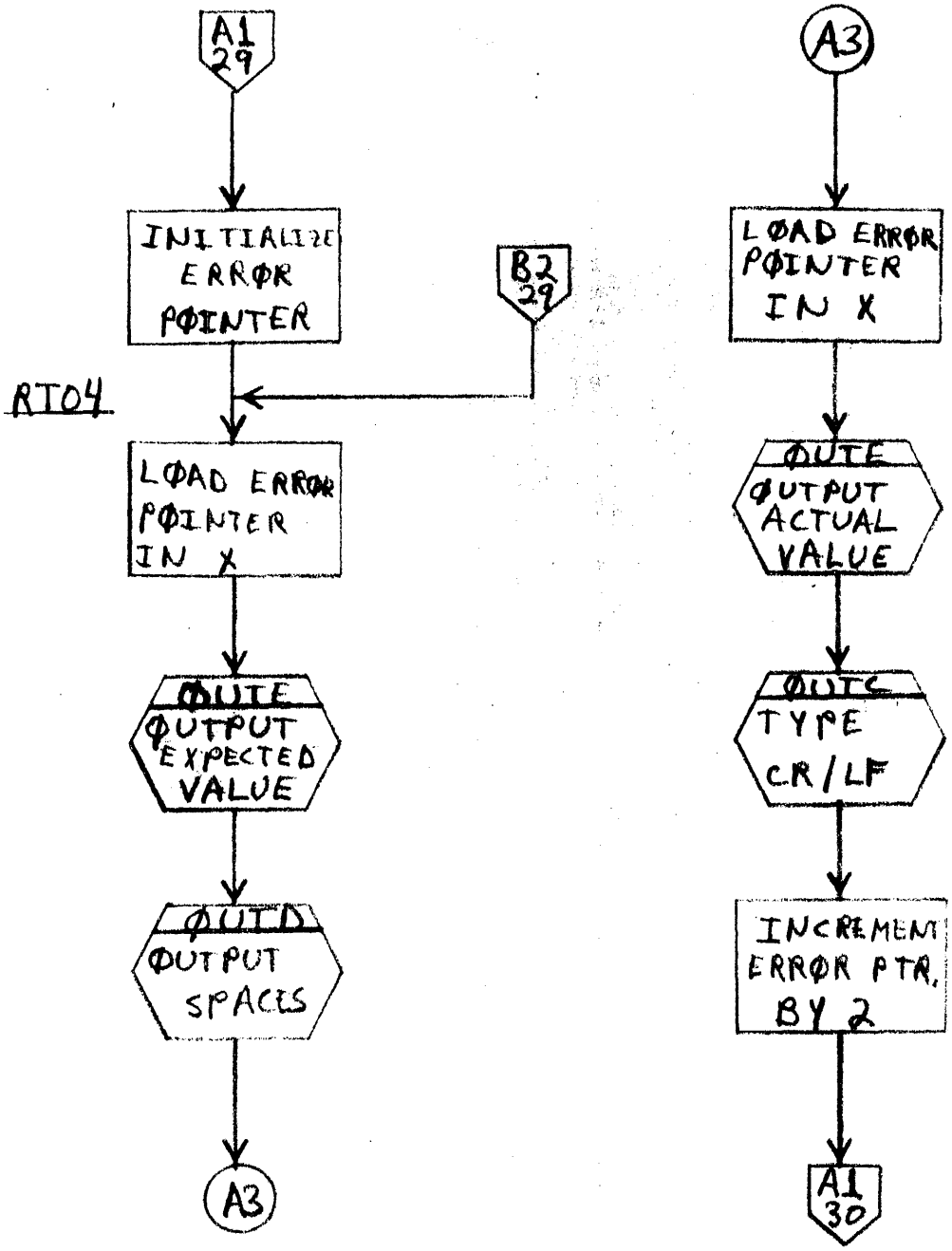
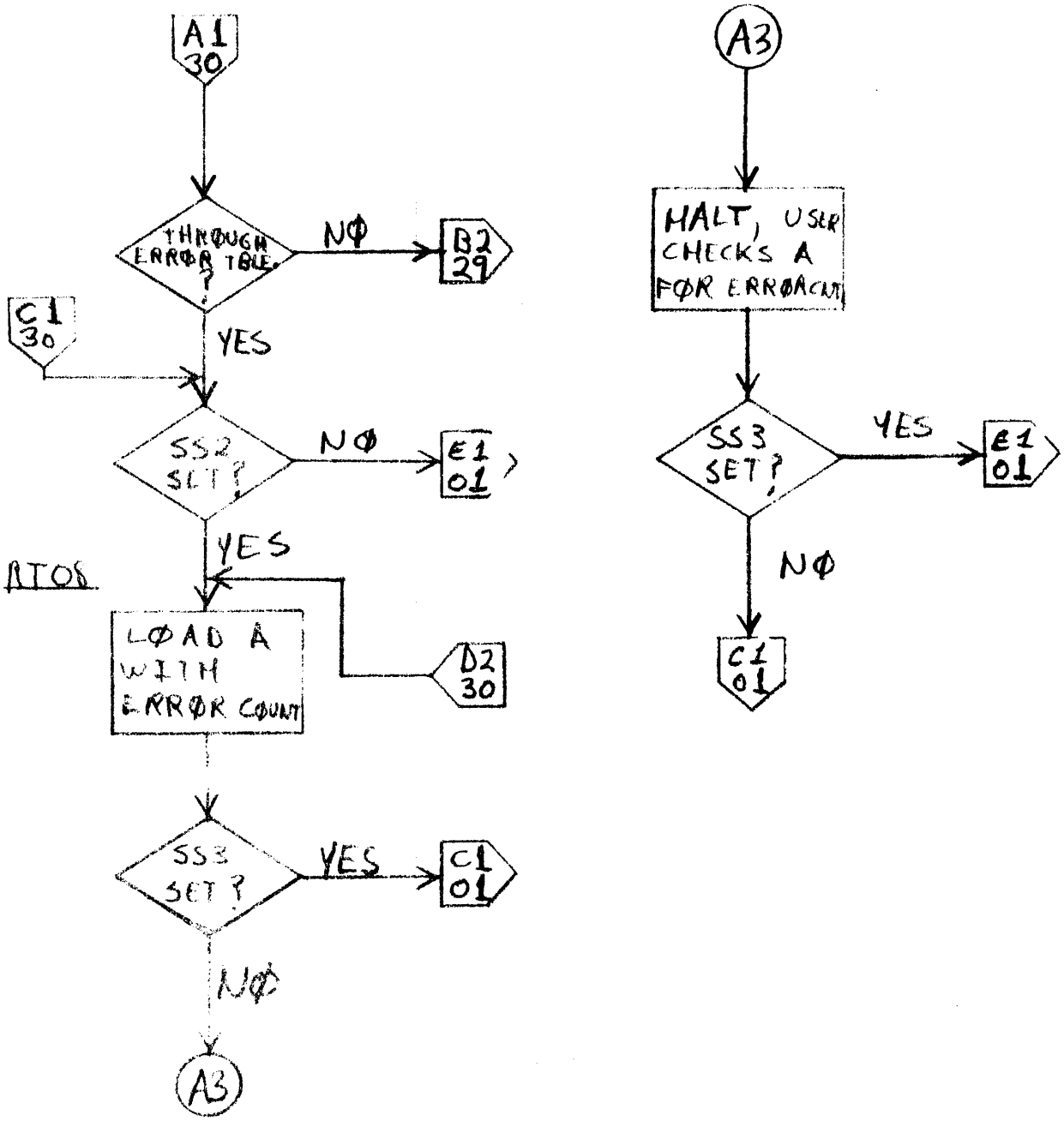
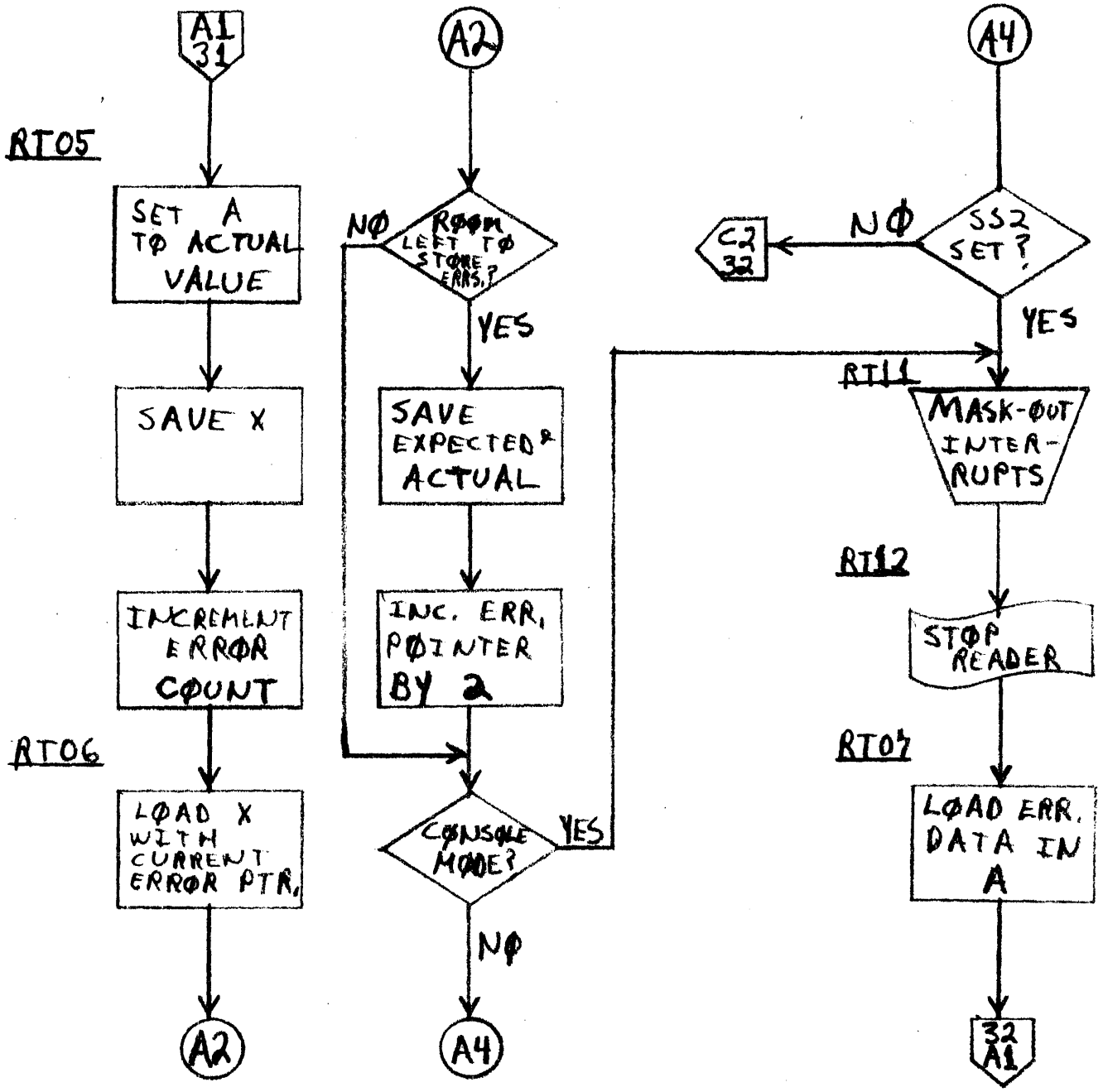
			SH 50 OF 96	REV

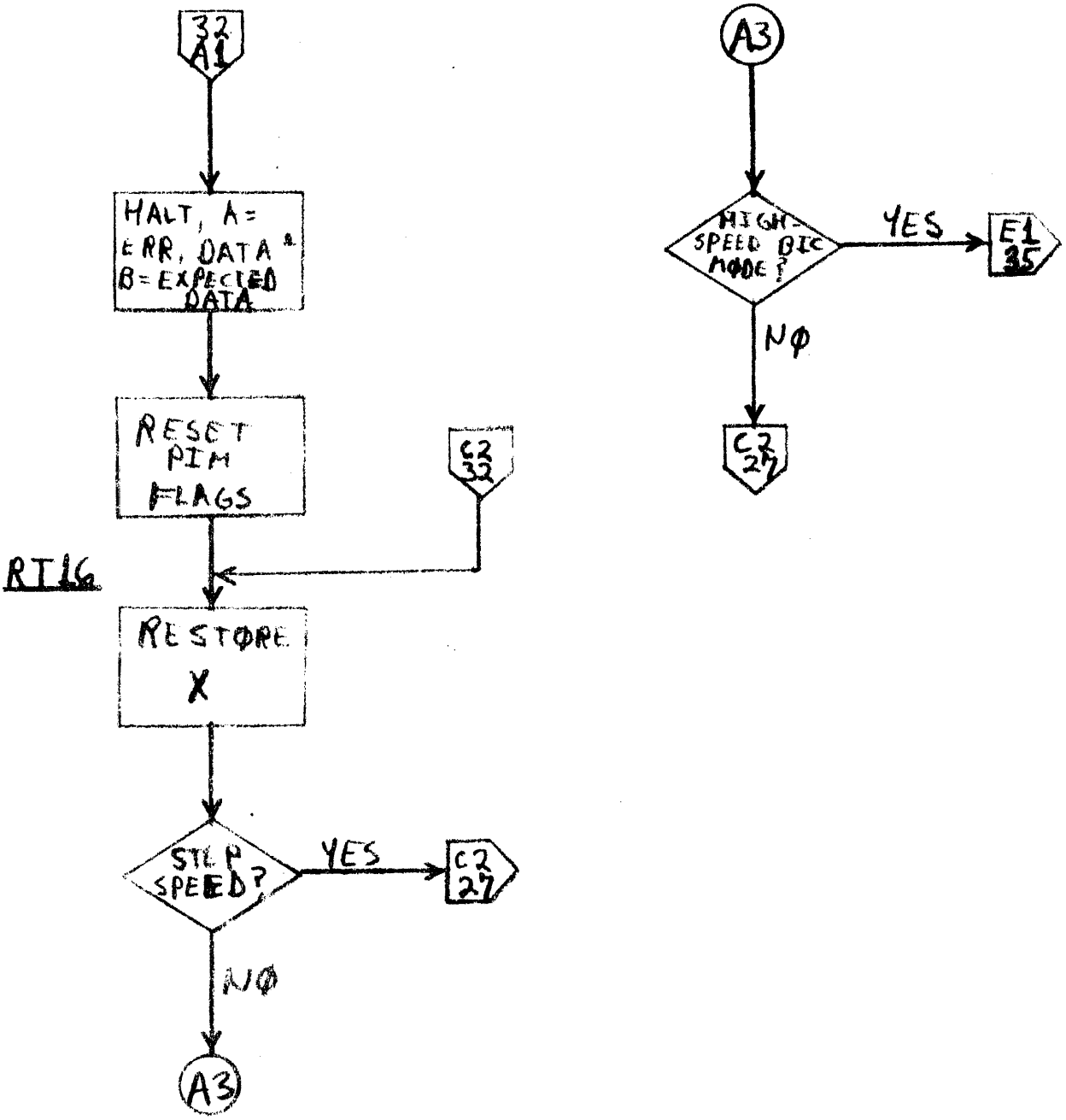

A1
27
IS CHACT. = CURR. CODE ?
NO
A1
31
YES
INCREMENT CURRENT CODE
C2
27
UPPER LIMIT PASSED ?
YES
RE-INITIALIZE CURRENT CODE
NO
DECREMENT CURRENT COUNT BY 1
A3
A3
CURR. COUNT=0 ?
NO
E3
26
YES
RT10
MASK-OUT INTERRUPTS
RT09
STOP READER
CONTINUOUS CYCLES ?
YES
C3
26
NO
A1
28

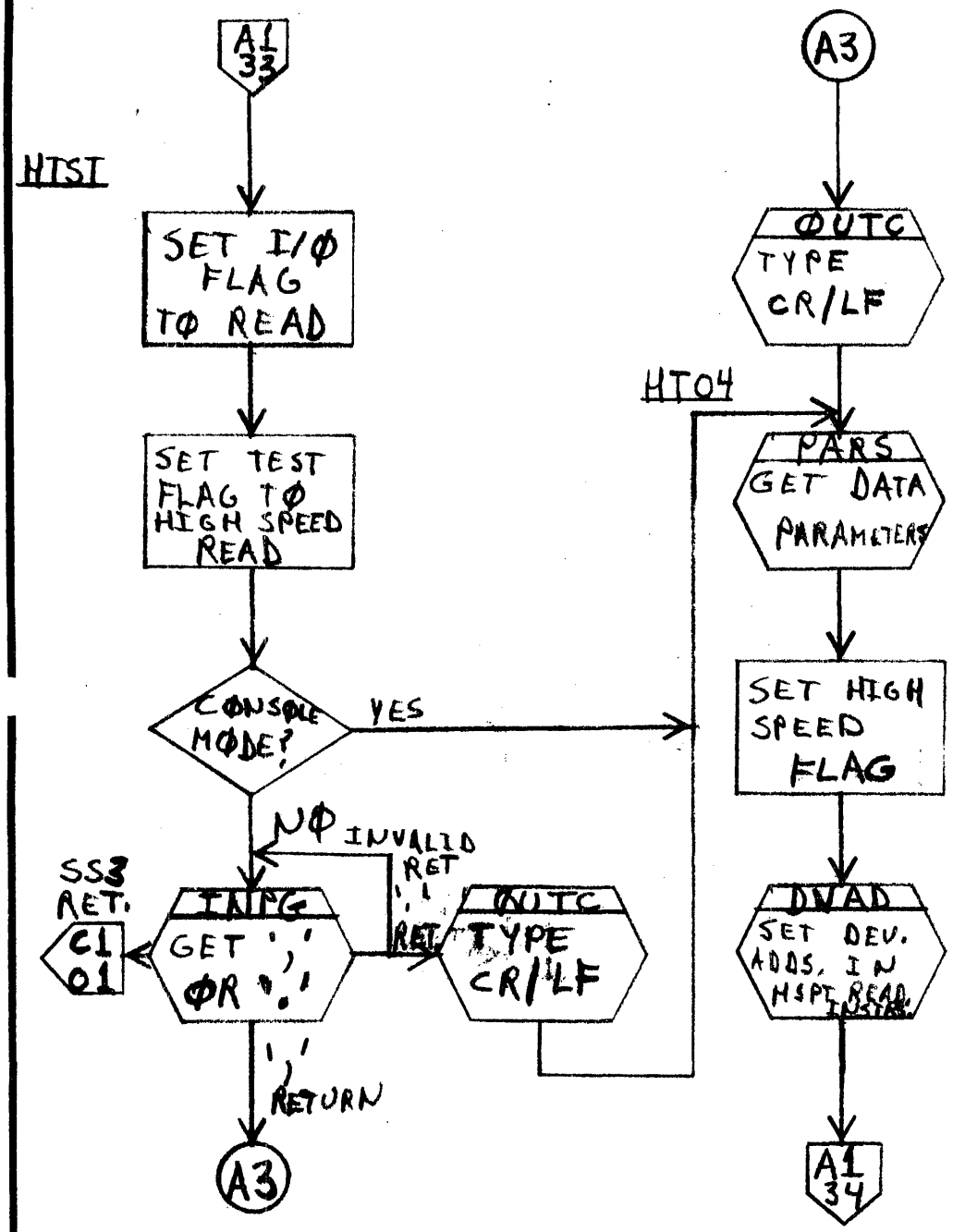

A1
28
CYCLE COUNT = CYCLE COUNT - 1
D1
28
CYCLE COUNT = 0 ?
NO
C3
26
RT15
YES
CONSOLE MODE ?
YES
D2
30
NO
SS1 SET
YES
C1
30
NO
A3
A3
OUTE
TYPE ERROR COUNT
OUTD
TYPE 'ERROR(S)'
ERRORS = 0 ?
YES
E1
01
NO
OUTA
TYPE 'EXPECTED ACTUAL'
A1
29

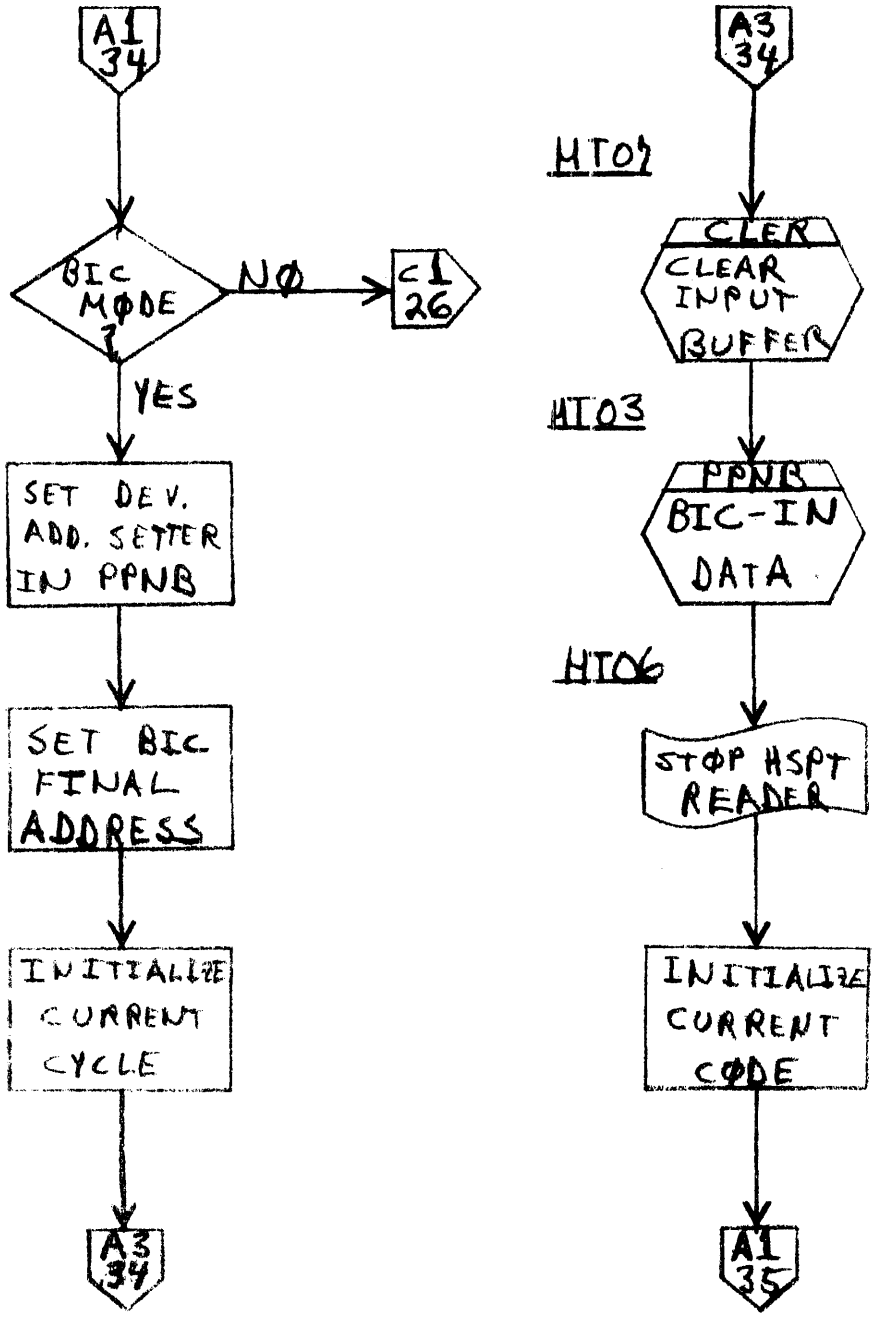

A1
29
INITIALIZE
ERROR
POINTER
B2
29
RTO4
LOAD ERROR
POINTER
IN X
QUTE
OUTPUT
EXPECTED
VALUE
QUTD
OUTPUT
SPACES
A3
A3
LOAD ERROR
POINTER
IN X
QUTE
OUTPUT
ACTUAL
VALUE
QUTC
TYPE
CR/LF
INCREMENT
ERROR PTR.
BY 2
A1
30

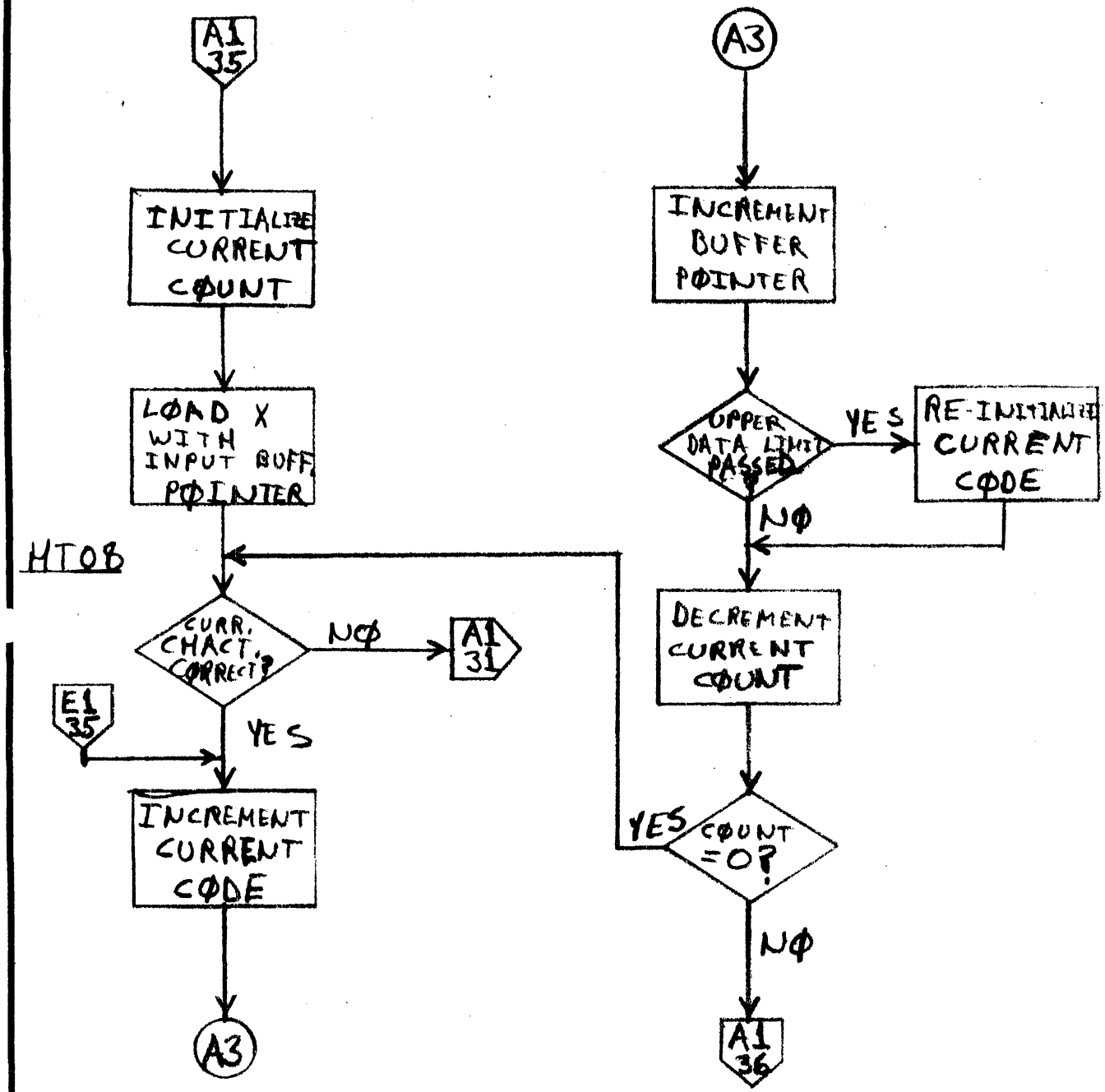

A1
30
THROUGH ERRØR TBLE. ?
NØ
B2
29
YES
C1
30
SS2 SET?
NØ
E1
01
YES
RTOS
LØAD A WITH ERRØR COUNT
D2
30
SS3 SET?
YES
C1
01
NØ
A3
A3
HALT, USER CHECKS A FØR ERRØR CNT
SS3 SET?
YES
E1
01
NØ
C1
01

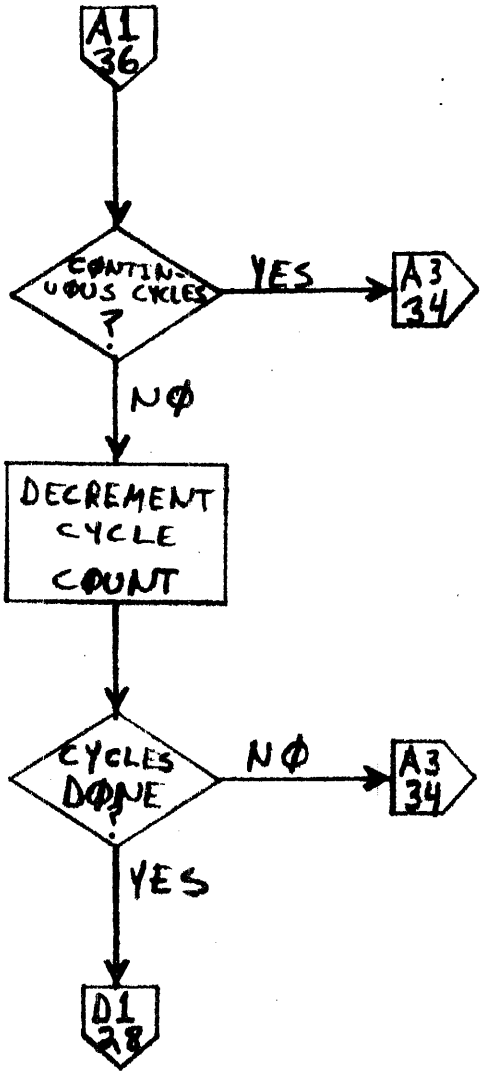

A1
31
RT05
SET A TO ACTUAL VALUE
SAVE X
INCREMENT ERROR COUNT
RT06
LOAD X WITH CURRENT ERROR PTR.
A2
A2
NO
ROOM LEFT TO STORE ERRS.?
YES
SAVE EXPECTED & ACTUAL
INC. ERR. POINTER BY 2
CONSOLE MODE?
YES
NO
A4
A4
C2
32
NO
SS2 SET?
YES
RT11
MASK-OUT INTER-RUPTS
RT12
STOP READER
RT07
LOAD ERR. DATA IN A
32
A1


32 A1
HALT, A = ERR, DATA B = EXPECTED DATA
RESET PIM FLAGS
C2 32
RTL6
RESTORE X
STEP SPEED?
YES
C2 27
NØ
A3
A3
HIGH-SPEED DIC MODE?
YES
E1 35
NØ
C2 27

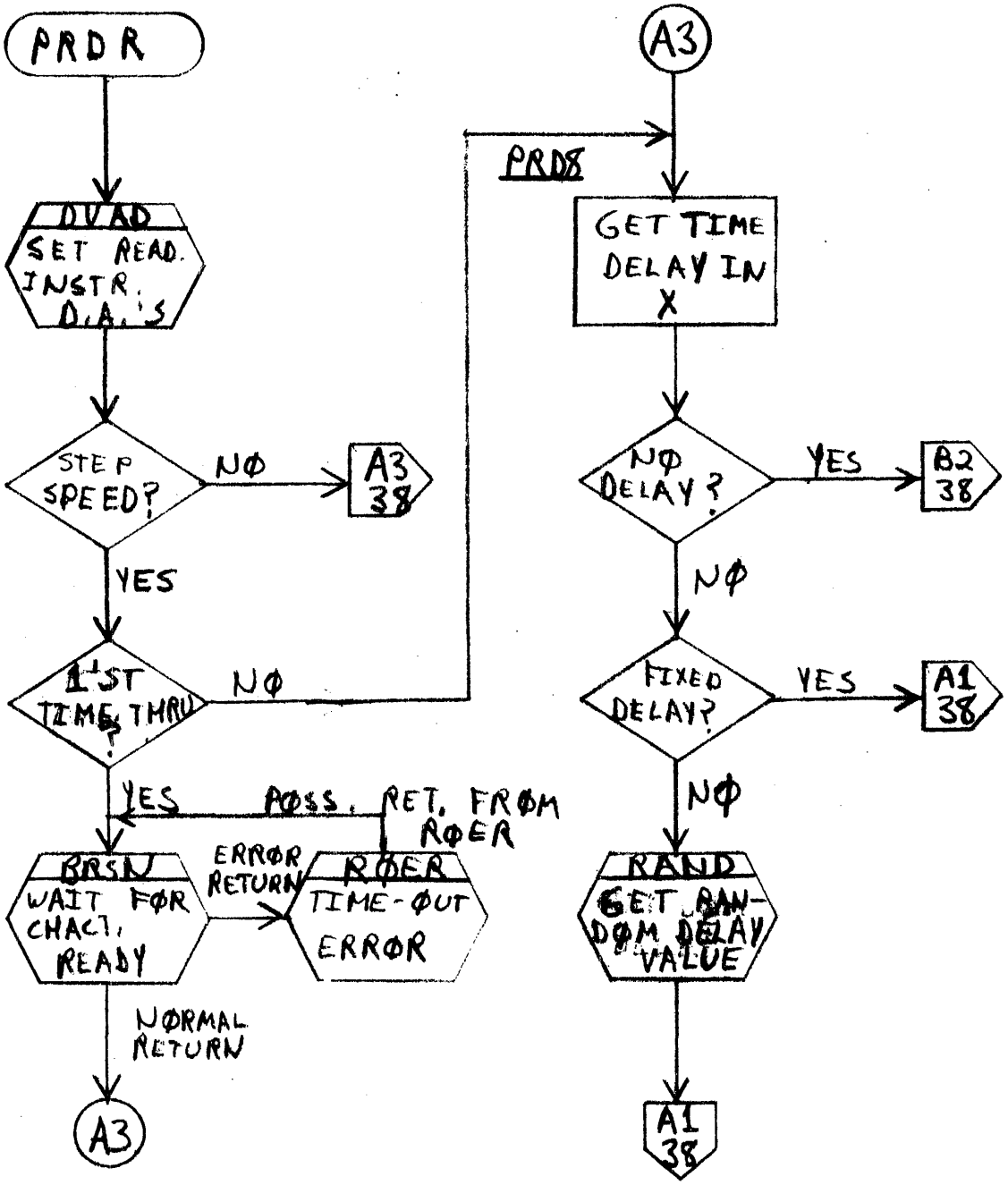

A1 33
HTSI
SET I/Ø FLAG TØ READ
SET TEST FLAG TØ HIGH SPEED READ
CONSOLE MØDE?
YES
NØ
INVALID RET
SS3 RET.
C1 Ø1
INPG
GET ',' ØR '.'
ØUTC
TYPE CR/LF
RET
RETURN
A3
A3
ØUTC
TYPE CR/LF
HTØ4
PARS
GET DATA PARAMETERS
SET HIGH SPEED FLAG
DVAD
SET DEV. ADDS. IN HSPT READ INSTR.
A1 34

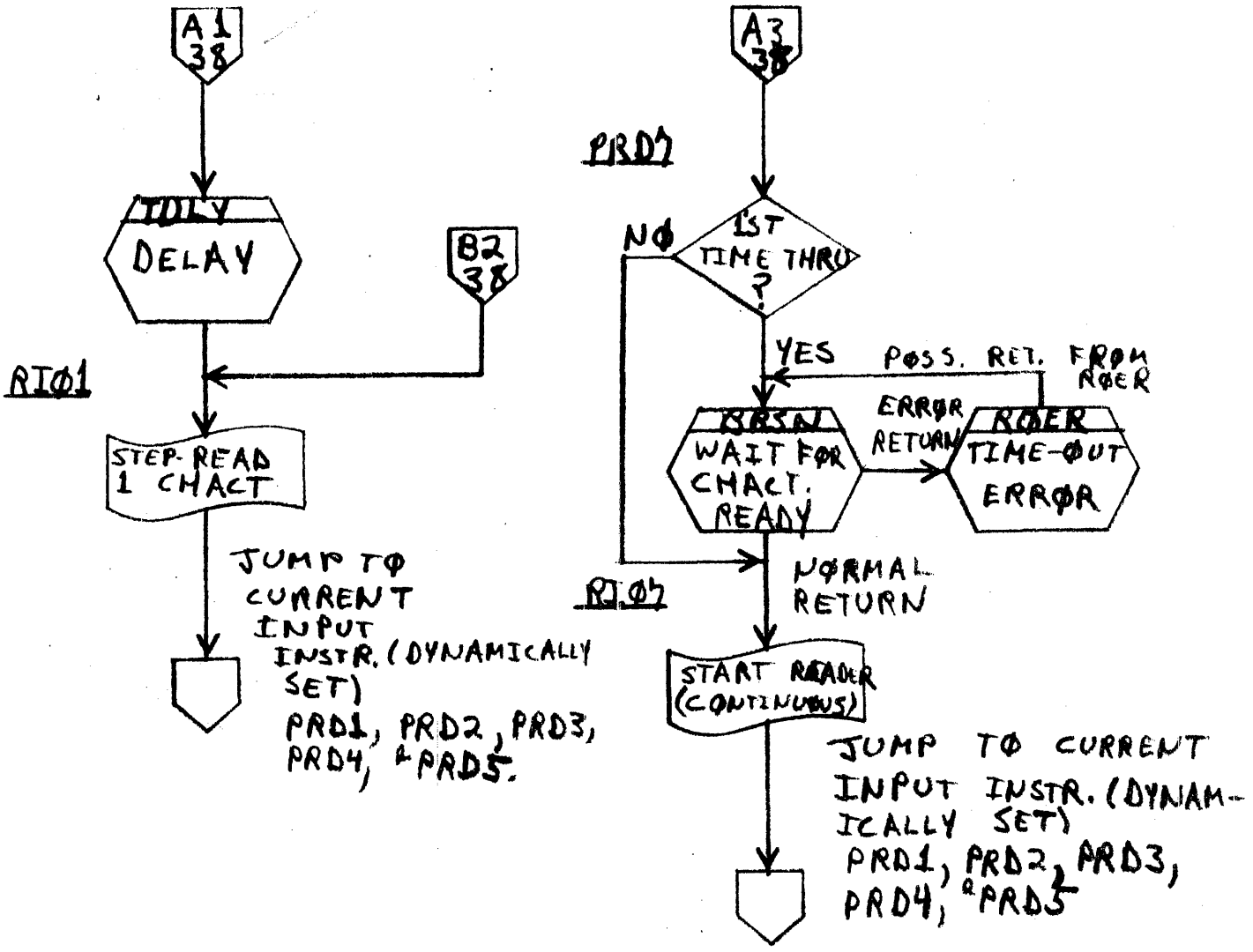

A1 34
BIC MODE ?
NO
C1 26
YES
SET DEV. ADD. SETTER IN PPNB
SET BIC FINAL ADDRESS
INITIALIZE CURRENT CYCLE
A3 34
A3 34
HTO2
CLER
CLEAR INPUT BUFFER
HTO3
PPNB
BIC-IN DATA
HTO6
STOP HSPT READER
INITIALIZE CURRENT CODE
A1 35

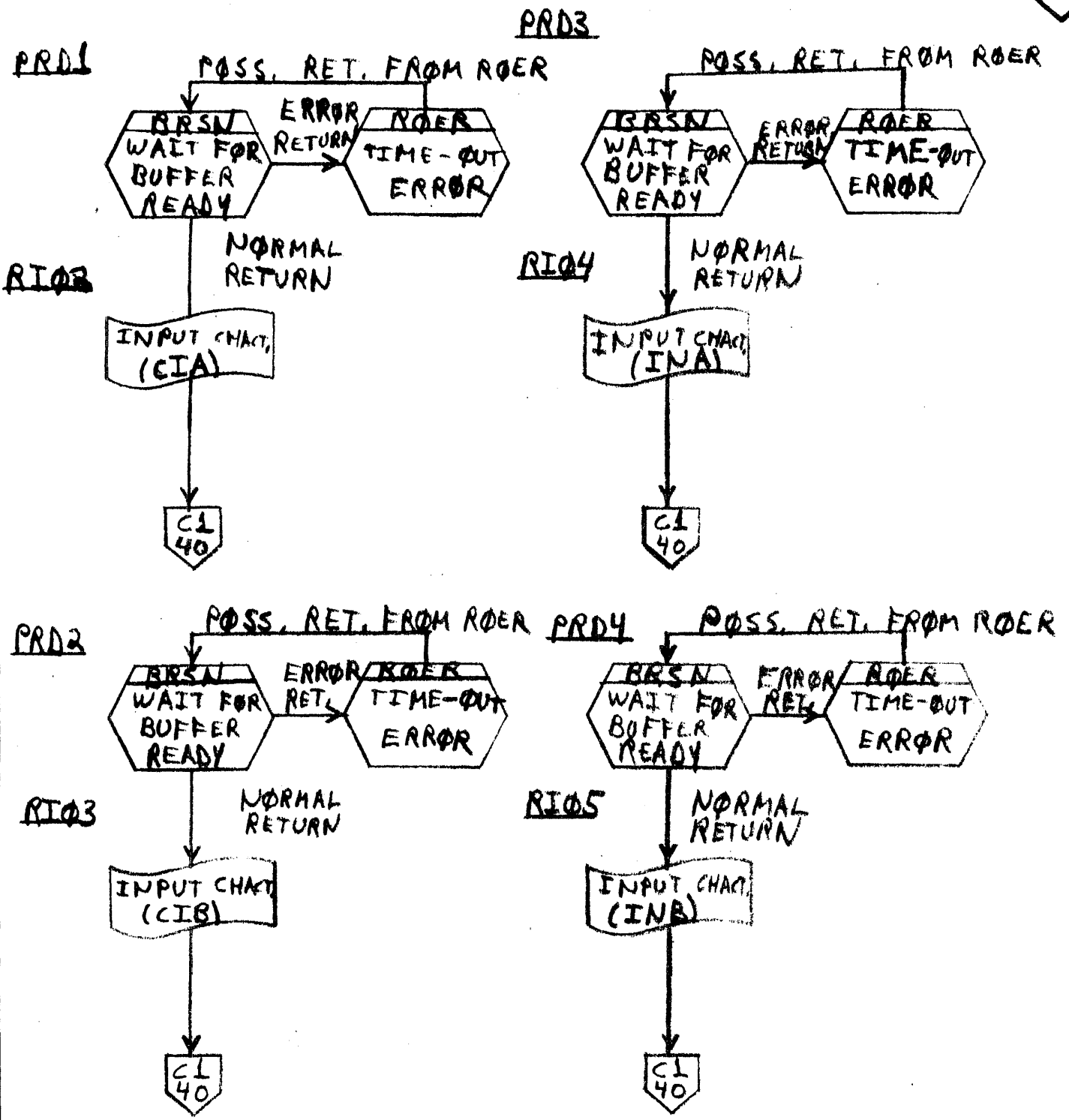

A1 35
INITIALIZE CURRENT COUNT
LOAD X WITH INPUT BUFF POINTER
HTOB
CURR. CHACT. CORRECT?
NO
A1 31
E1 35
YES
INCREMENT CURRENT CODE
A3
A3
INCREMENT BUFFER POINTER
UPPER DATA LIMIT PASSED
YES
RE-INITIALIZE CURRENT CODE
NO
DECREMENT CURRENT COUNT
YES
COUNT =0?
NO
A1 36

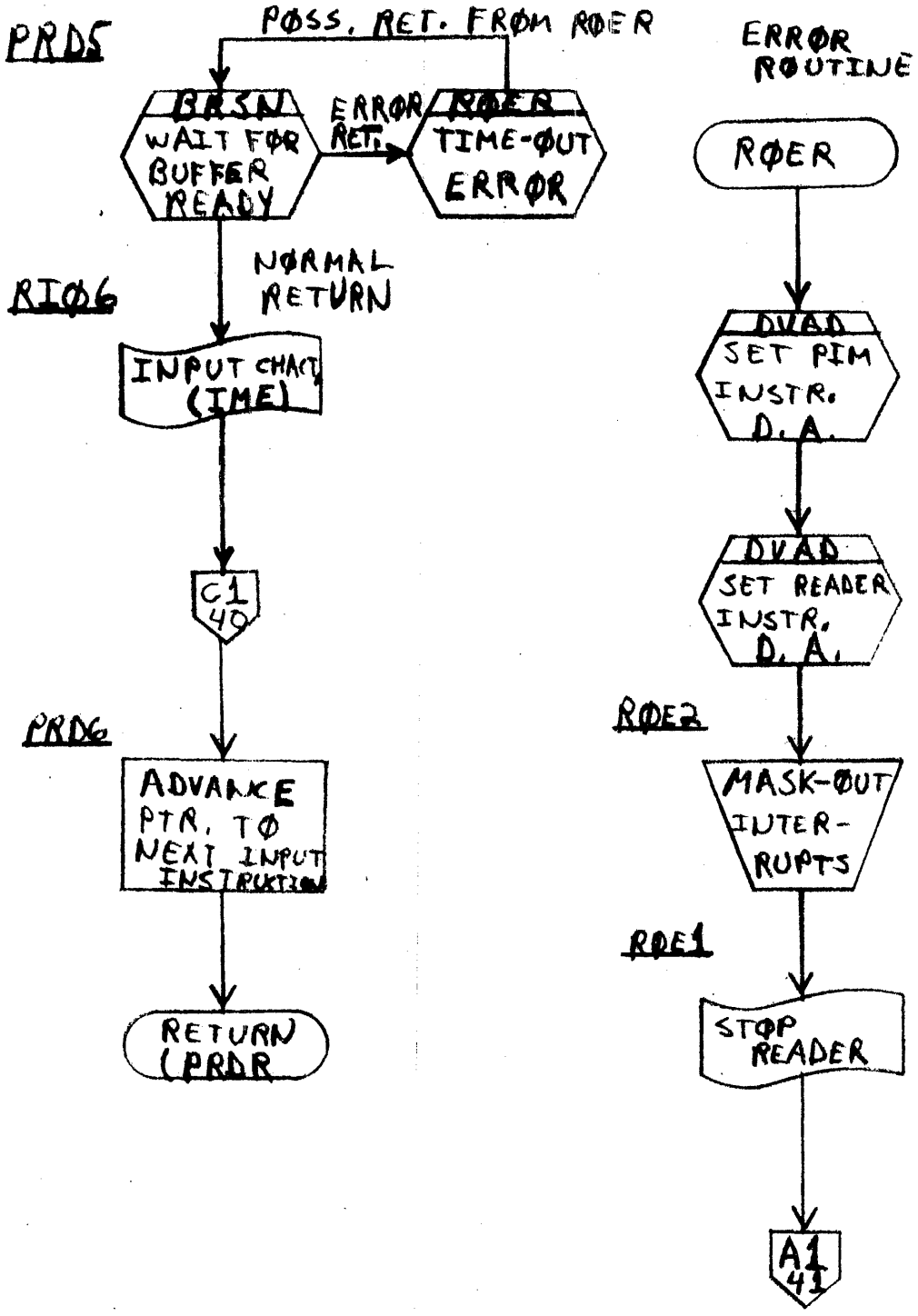

A1
36
CONTIN-
UOUS CYCLES
?
YES
A3
34
NO
DECREMENT
CYCLE
COUNT
CYCLES
DONE
?
NO
A3
34
YES
D1
28

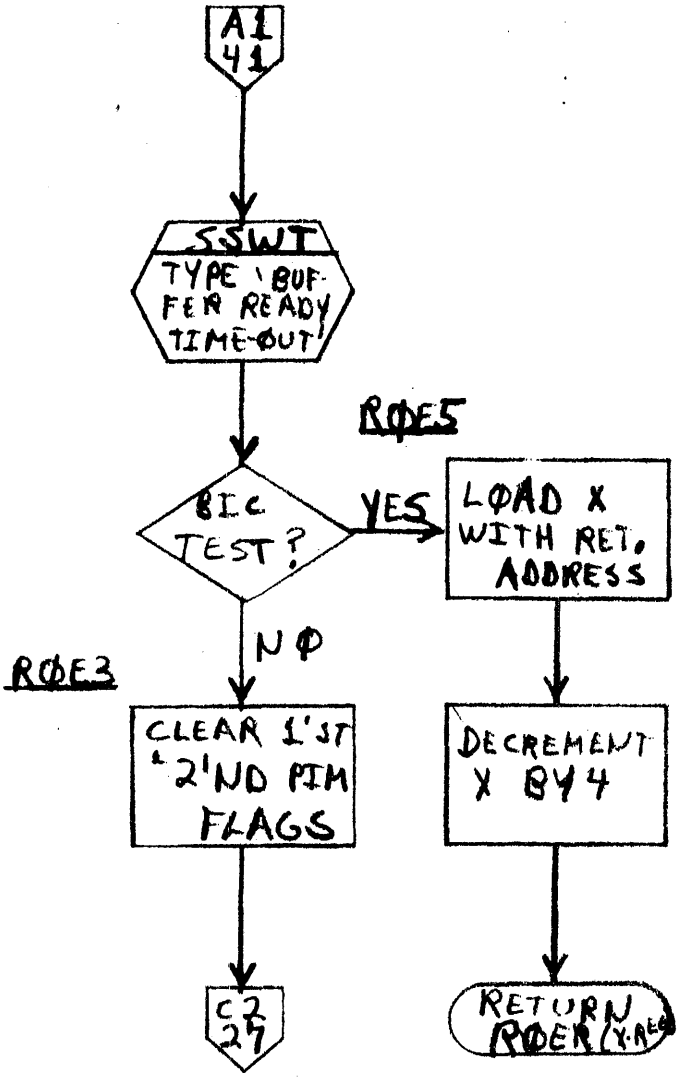
READ (SENSE ØR PIM MØDE)



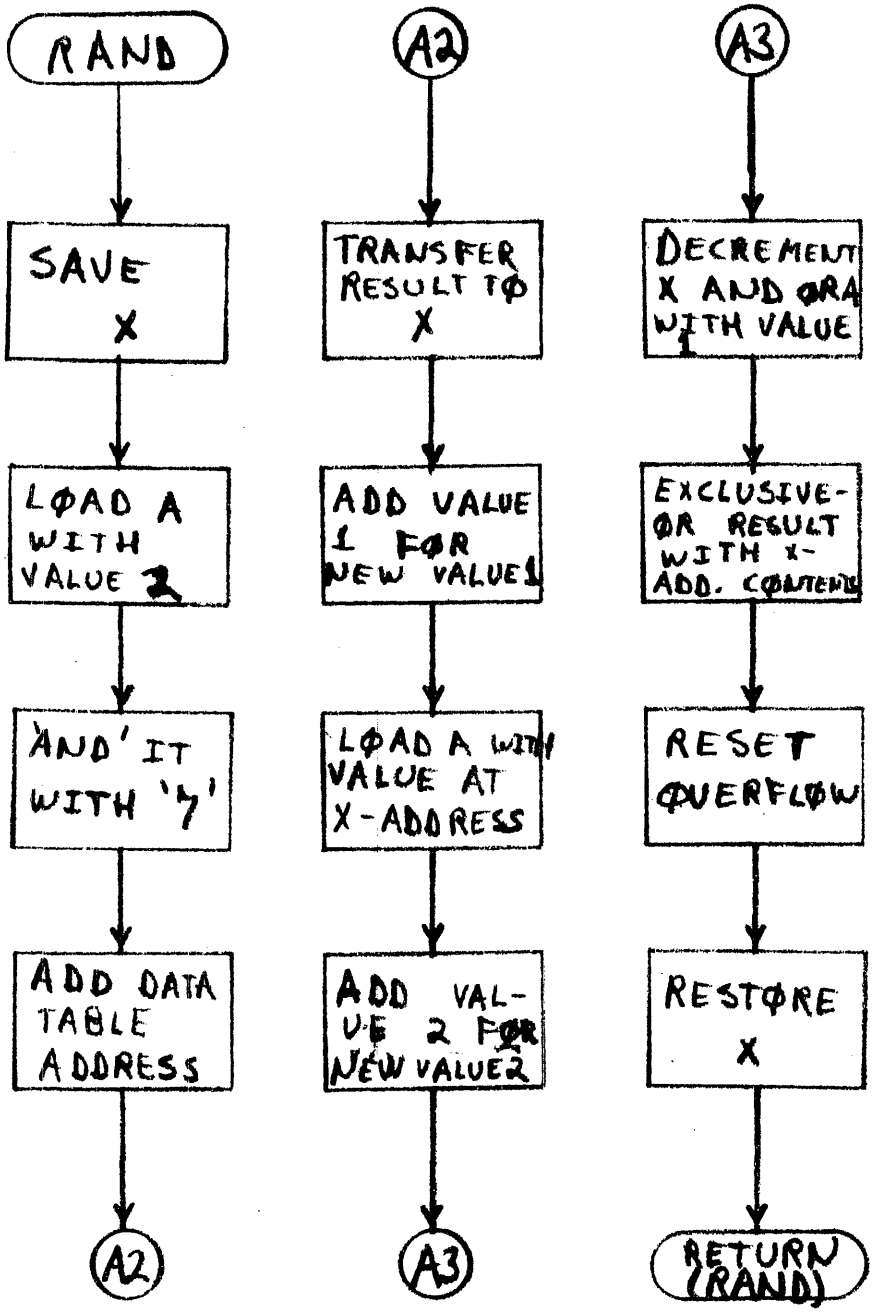

A1 3B
TDLY
DELAY
B2 3B
RIØ1
STEP READ 1 CHACT
JUMP TØ CURRENT INPUT INSTR. (DYNAMICALLY SET) PRD1, PRD2, PRD3, PRD4, & PRD5.
A3 3B
PRD7
NØ
1ST TIME THRU ?
YES
POSS. RET. FRØM RØER
ERRØR RETURN
RØER
WAIT FØR CHACT. READY
RØER
TIME-ØUT ERRØR
RI.Ø7
NØRMAL RETURN
START READER (CONTINUOUS)
JUMP TØ CURRENT INPUT INSTR. (DYNAMICALLY SET) PRD1, PRD2, PRD3, PRD4, & PRD5


PRD1
PØSS. RET. FRØM RØER
BRSN
WAIT FØR BUFFER READY
ERRØR RETURN
RØER
TIME-ØUT ERRØR
NØRMAL RETURN
RIØ2
INPUT CHACT (CIA)
C1 40
PRD3
PØSS. RET. FRØM RØER
BRSN
WAIT FØR BUFFER READY
ERRØR RETURN
RØER
TIME-ØUT ERRØR
NØRMAL RETURN
RIØ4
INPUT CHACT (INA)
C1 40
PRD2
PØSS. RET. FRØM RØER
BRSN
WAIT FØR BUFFER READY
ERRØR RET.
RØER
TIME-ØUT ERRØR
NØRMAL RETURN
RIØ3
INPUT CHACT (CIB)
C1 40
PRD4
PØSS. RET. FRØM RØER
BRSN
WAIT FØR BUFFER READY
ERRØR RET.
RØER
TIME-ØUT ERRØR
NØRMAL RETURN
RIØ5
INPUT CHACT (INB)
C1 40

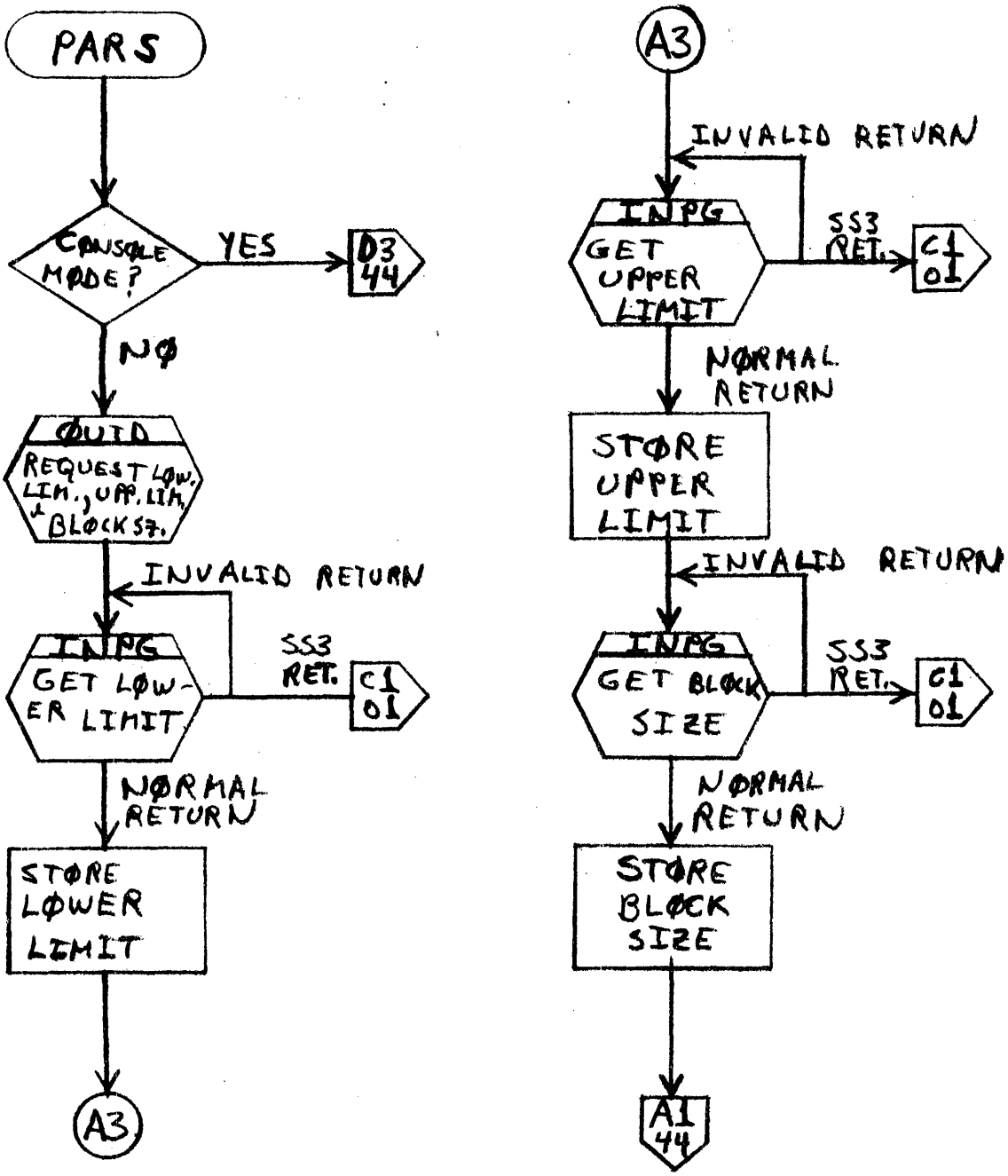

PRD5
POSS. RET. FROM RØER
BRSN
WAIT FØR BUFFER READY
ERRØR RET.
RØER
TIME-ØUT ERRØR
NØRMAL RETURN
RIØ6
INPUT CHAR (IME)
C1 40
PRD6
ADVANCE PTR. TØ NEXT INPUT INSTRUCTION
RETURN (PRDR
ERRØR ROUTINE
RØER
DVAD
SET PIM INSTR. D.A.
DVAD
SET READER INSTR. D.A.
RØE2
MASK-ØUT INTER-RUPTS
RØE1
STØP READER
A1 41

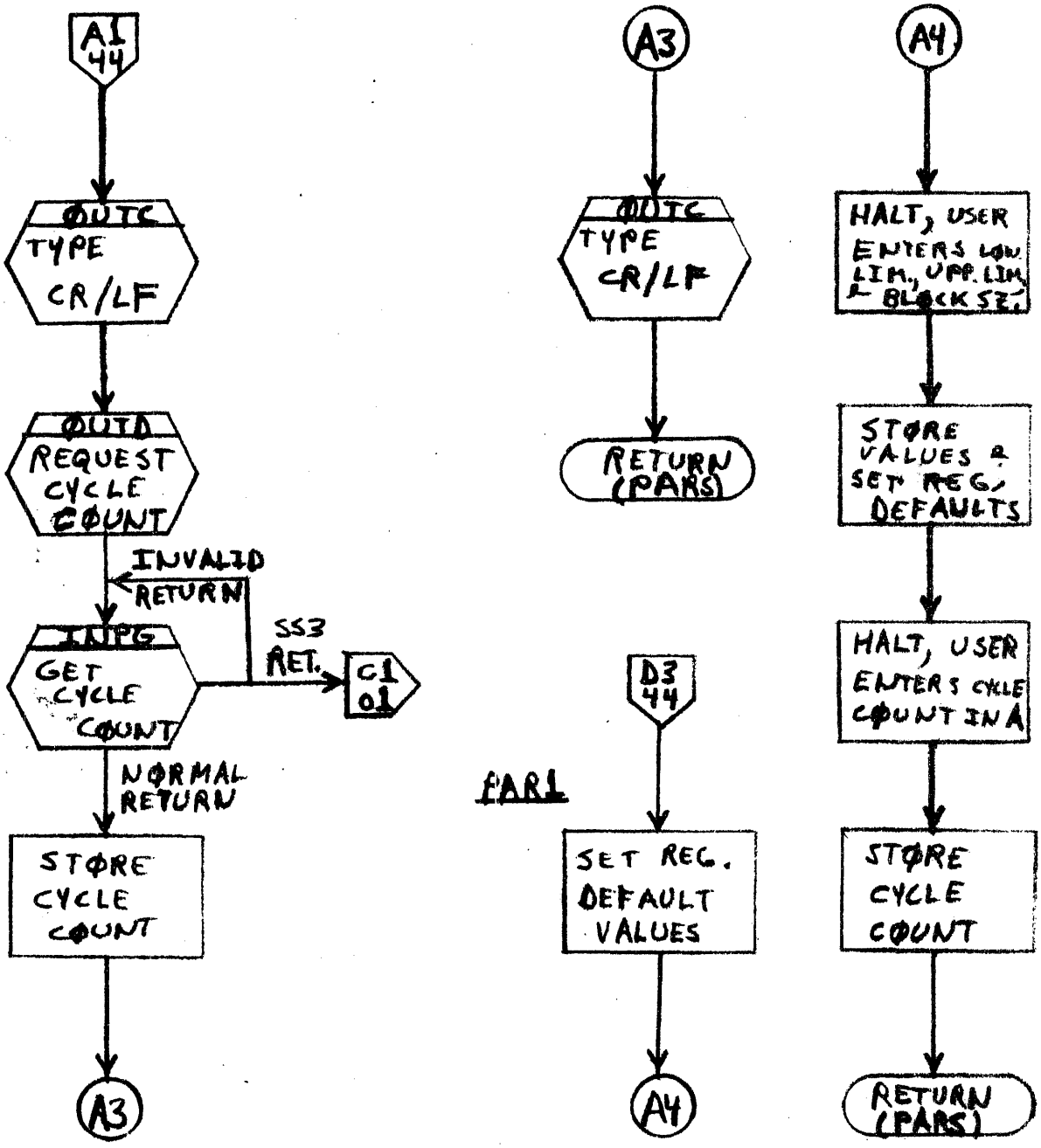

A1
41
SSWT
TYPE \ BUF-
FER READY
TIME-OUT
RØE5
BIC
TEST?
YES
LØAD X
WITH RET.
ADDRESS
NØ
RØE3
CLEAR 1'ST
& 2'ND PIM
FLAGS
DECREMENT
X BY 4
C2
29
RETURN
RØER (X-REG

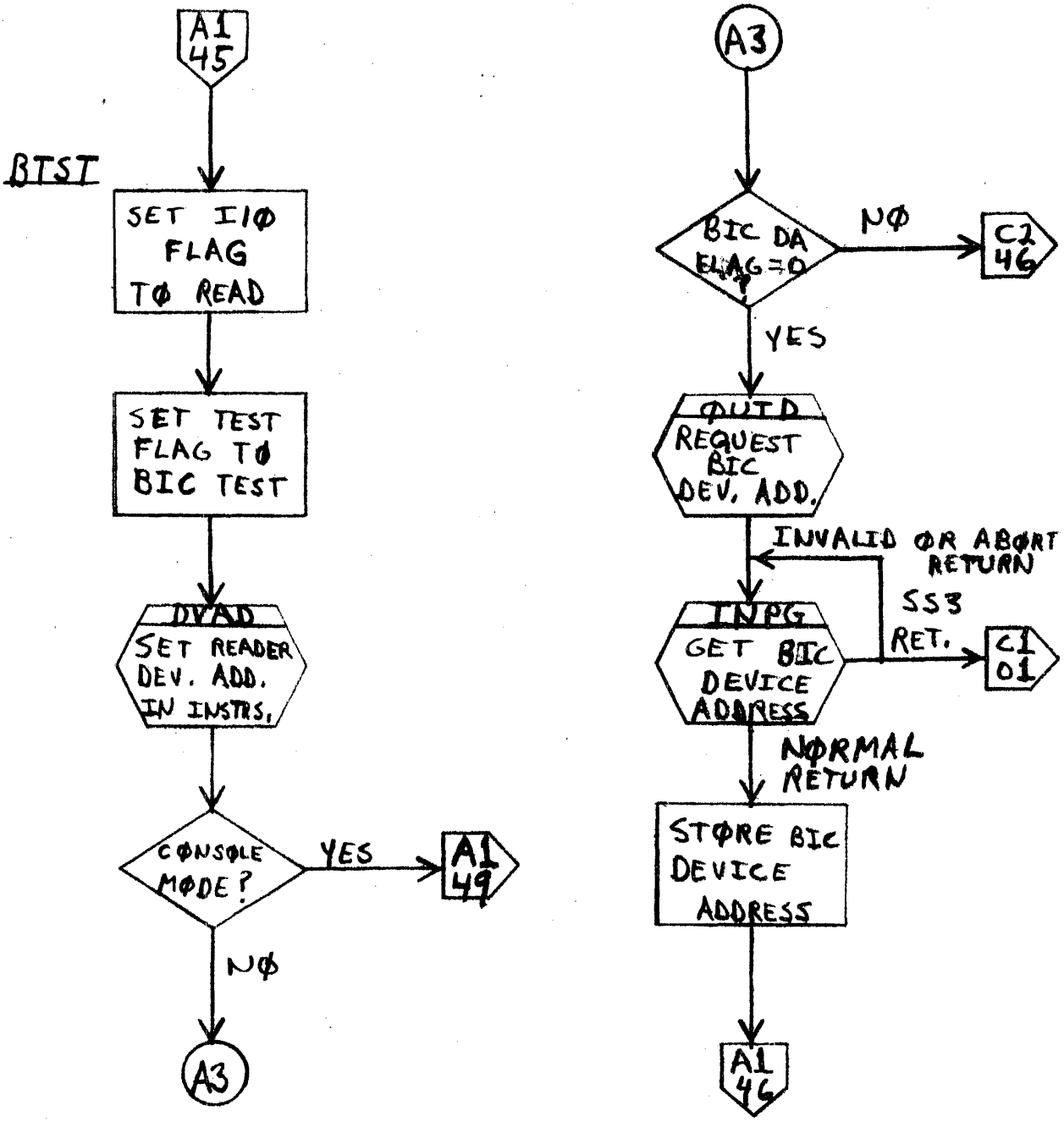
PSUEDO-RANDOM NUMBER GENERATOR

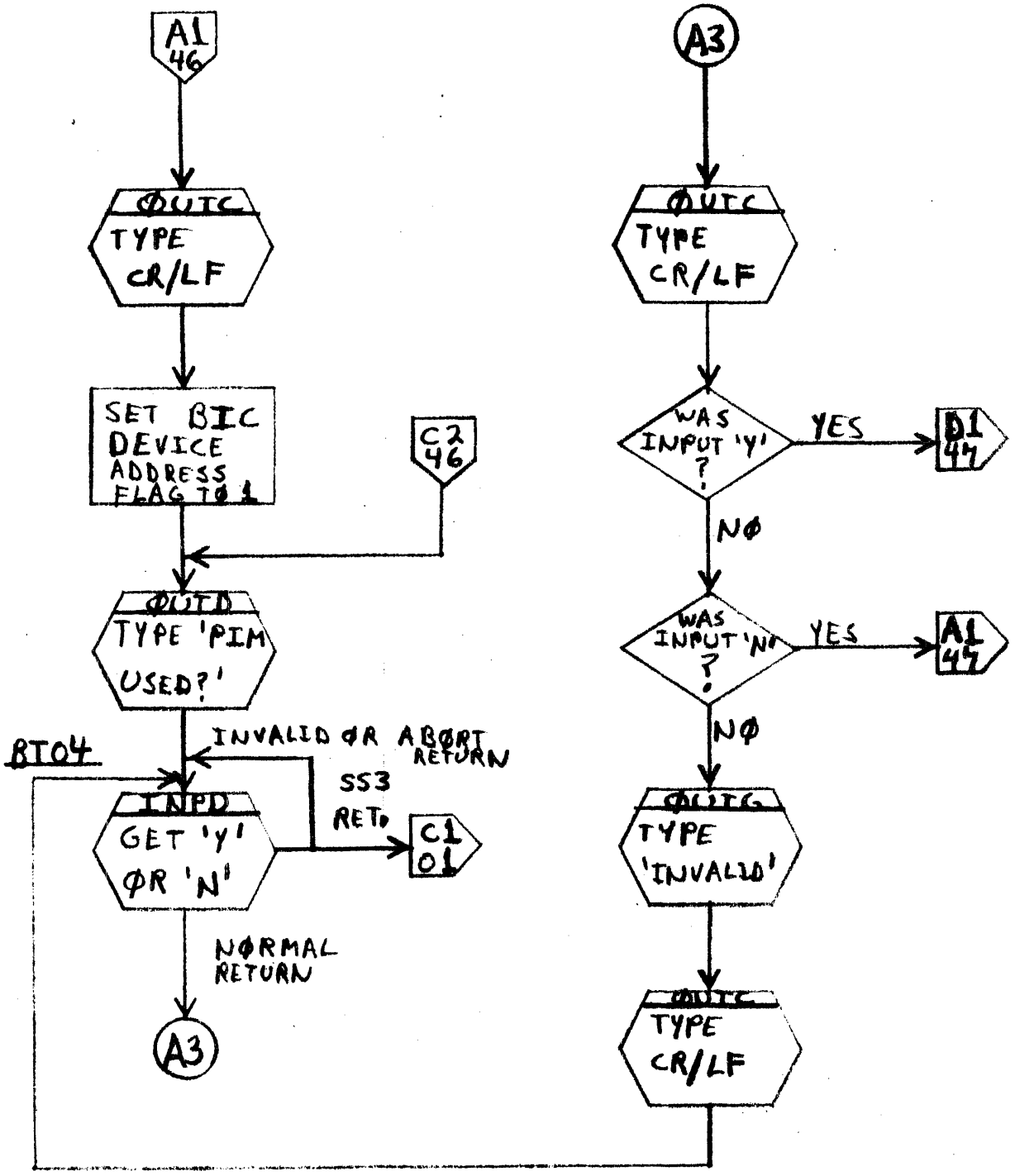


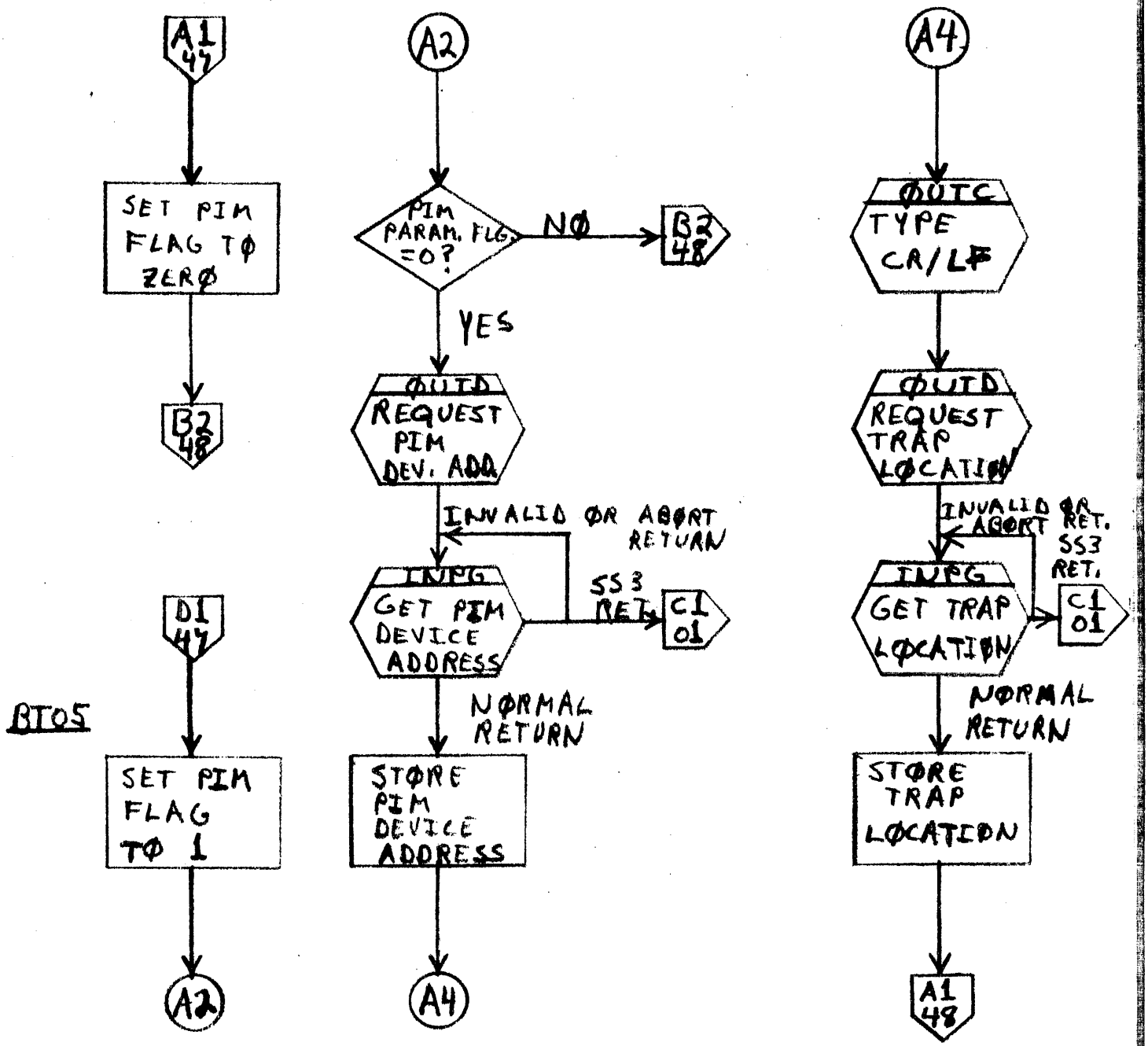
PARAMETER SETTING SUBROUTINE FOR PTST, RTST, & HTST




A1 44
ØUTC
TYPE CR/LF
ØUTD
REQUEST CYCLE COUNT
INVALID RETURN
INPG
GET CYCLE COUNT
SS3 RET.
C1 01
NORMAL RETURN
STORE CYCLE COUNT
A3
A3
ØUTC
TYPE CR/LF
RETURN (PARS)
A4
HALT, USER ENTERS LOW LIM., UPP. LIM. & BLOCK SZ.
STORE VALUES & SET REG. DEFAULTS
HALT, USER ENTERS CYCLE COUNT IN A
STORE CYCLE COUNT
RETURN (PARS)
FAR1
D3 44
SET REG. DEFAULT VALUES
A4


A1 45
BTST
SET IIØ FLAG TØ READ
SET TEST FLAG TØ BIC TEST
DVAD
SET READER DEV. ADD. IN INSTRS.
CØNSØLE MØDE?
YES
A1 49
NØ
A3
A3
BIC DA FLAG=0
NØ
C1 46
YES
ØUTD
REQUEST BIC DEV. ADD.
INVALID ØR ABØRT RETURN
INPG
GET BIC DEVICE ADDRESS
SS3 RET.
C1 01
NØRMAL RETURN
STØRE BIC DEVICE ADDRESS
A1 46


A1
46
ØUTC
TYPE
CR/LF
SET BIC
DEVICE
ADDRESS
FLAG TØ 1
C2
46
ØUTD
TYPE 'PIM
USED?'
BIØ4
INVALID ØR ABØRT
RETURN
SS3
RETN
INPD
GET 'Y'
ØR 'N'
C1
01
NØRMAL
RETURN
A3
A3
ØUTC
TYPE
CR/LF
WAS
INPUT 'Y'
?
YES
D1
47
NØ
WAS
INPUT 'N'
?
YES
A1
47
NØ
ØUTG
TYPE
'INVALID'
ØUTC
TYPE
CR/LF



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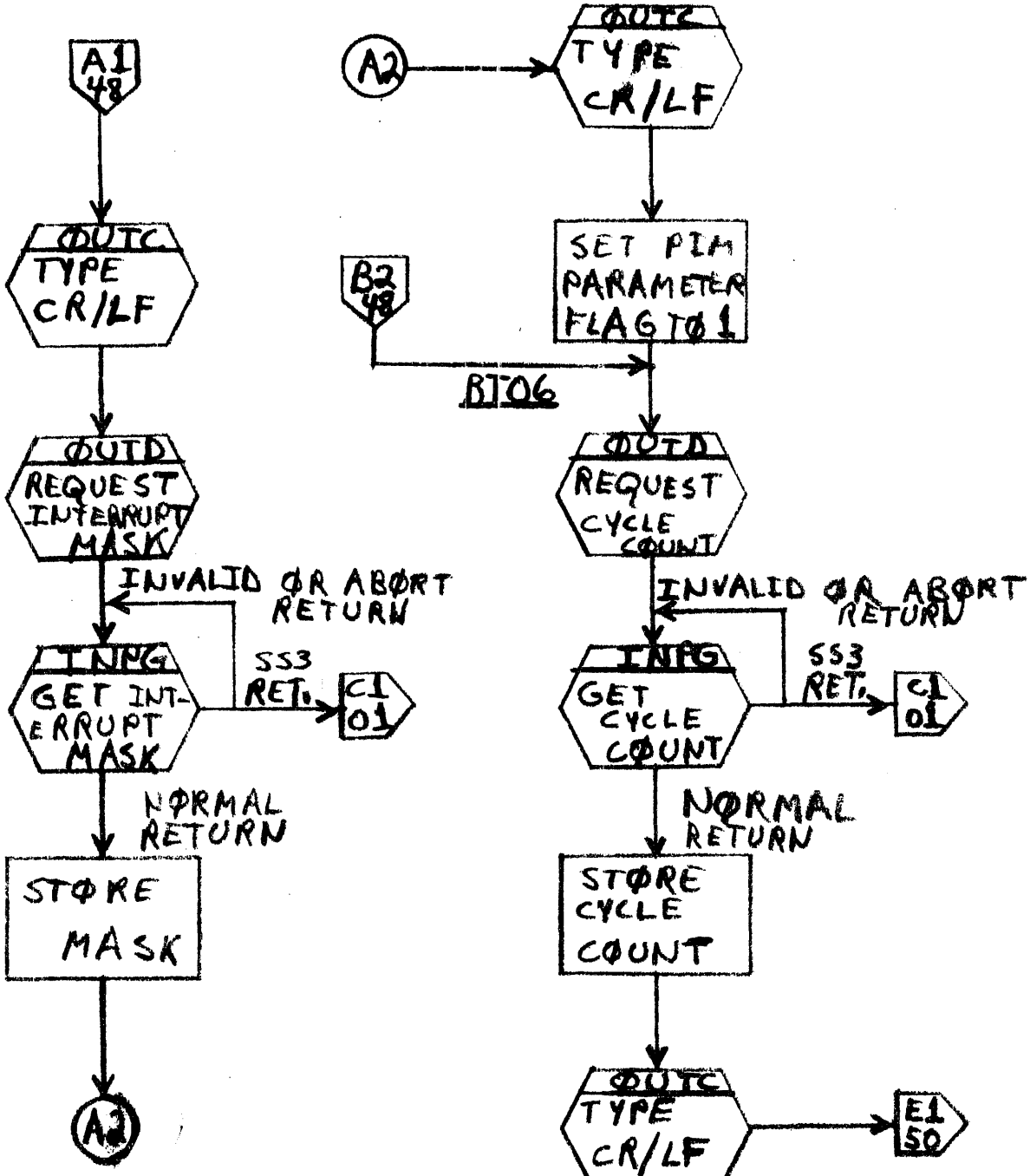
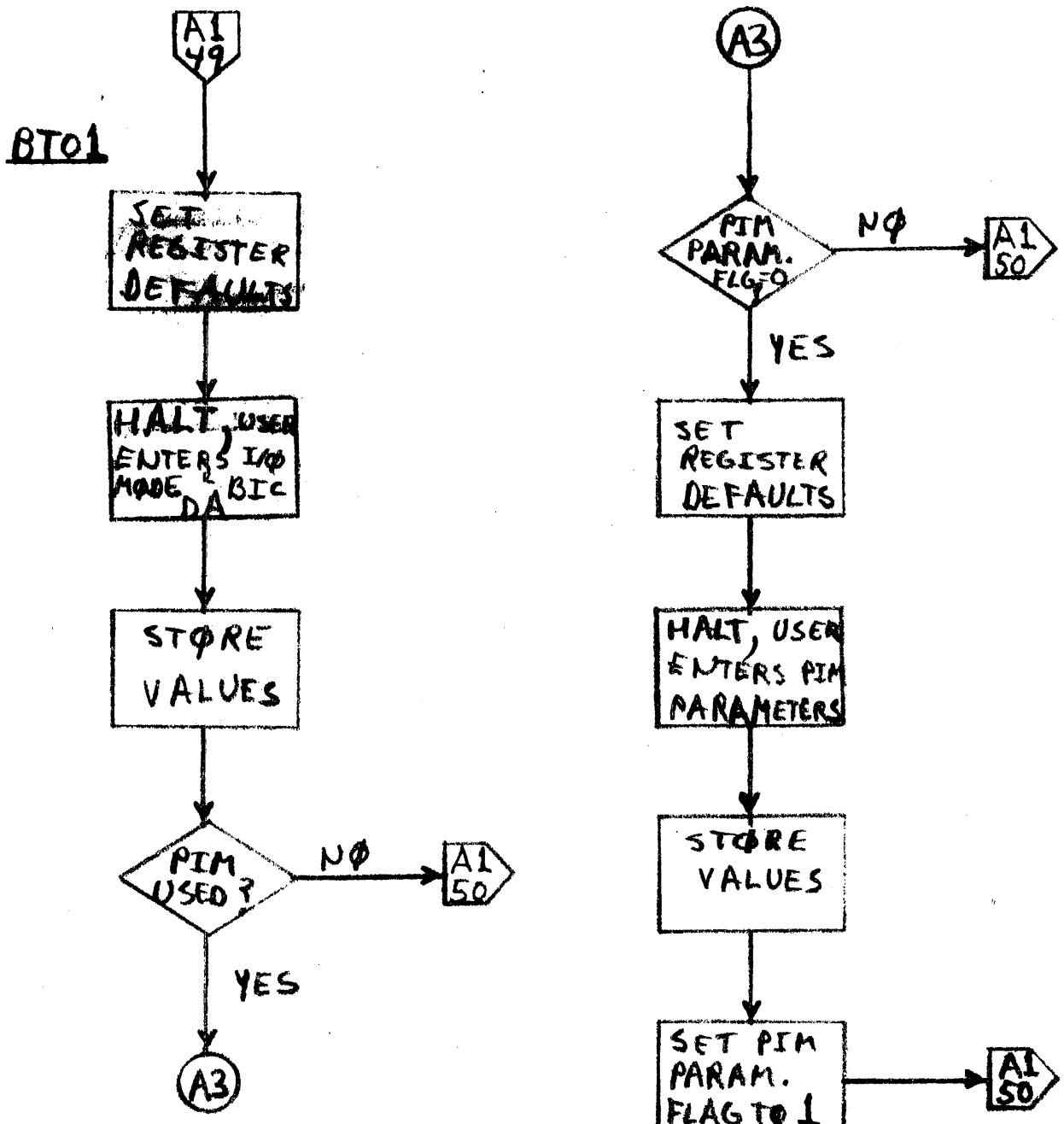
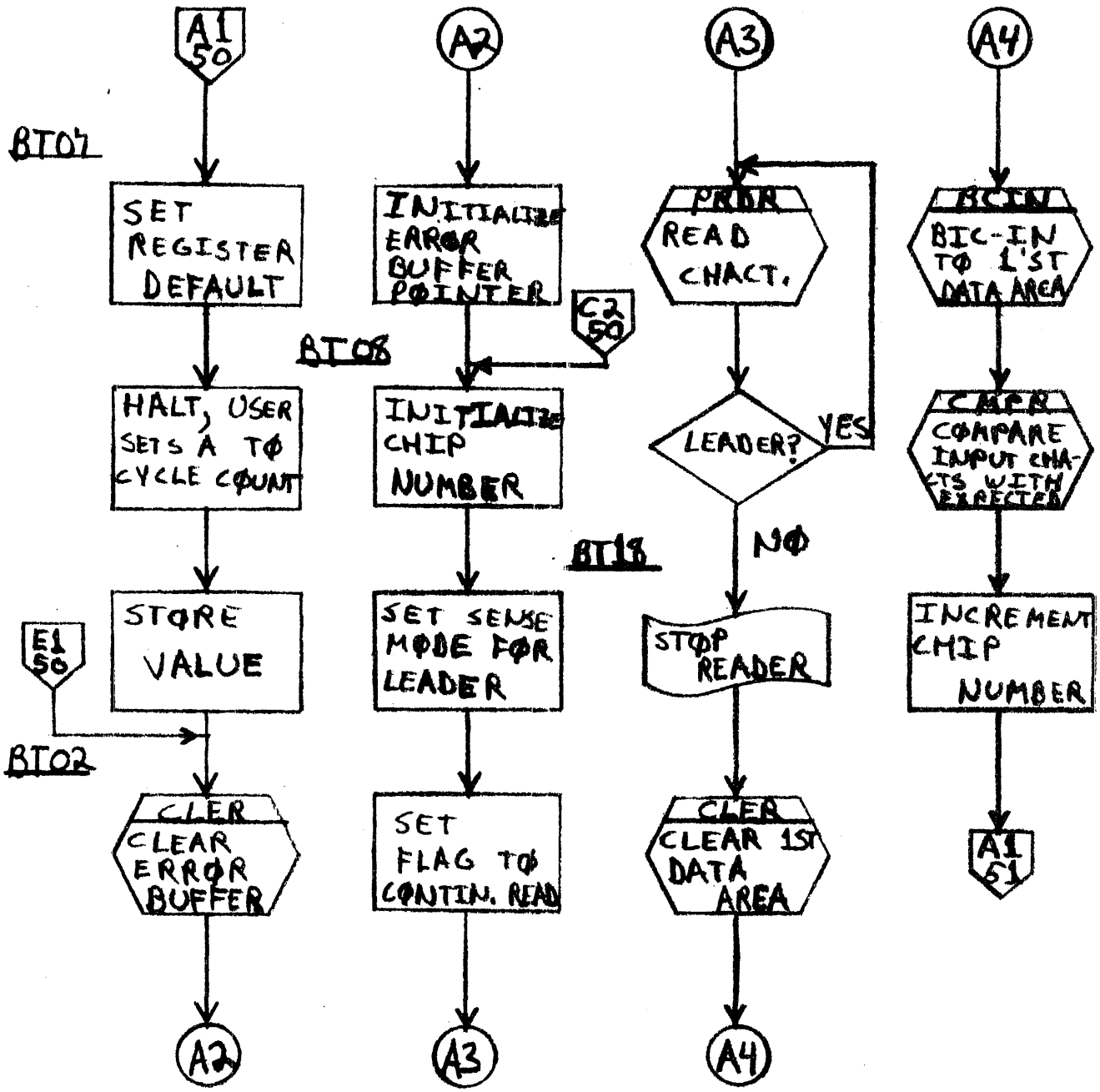
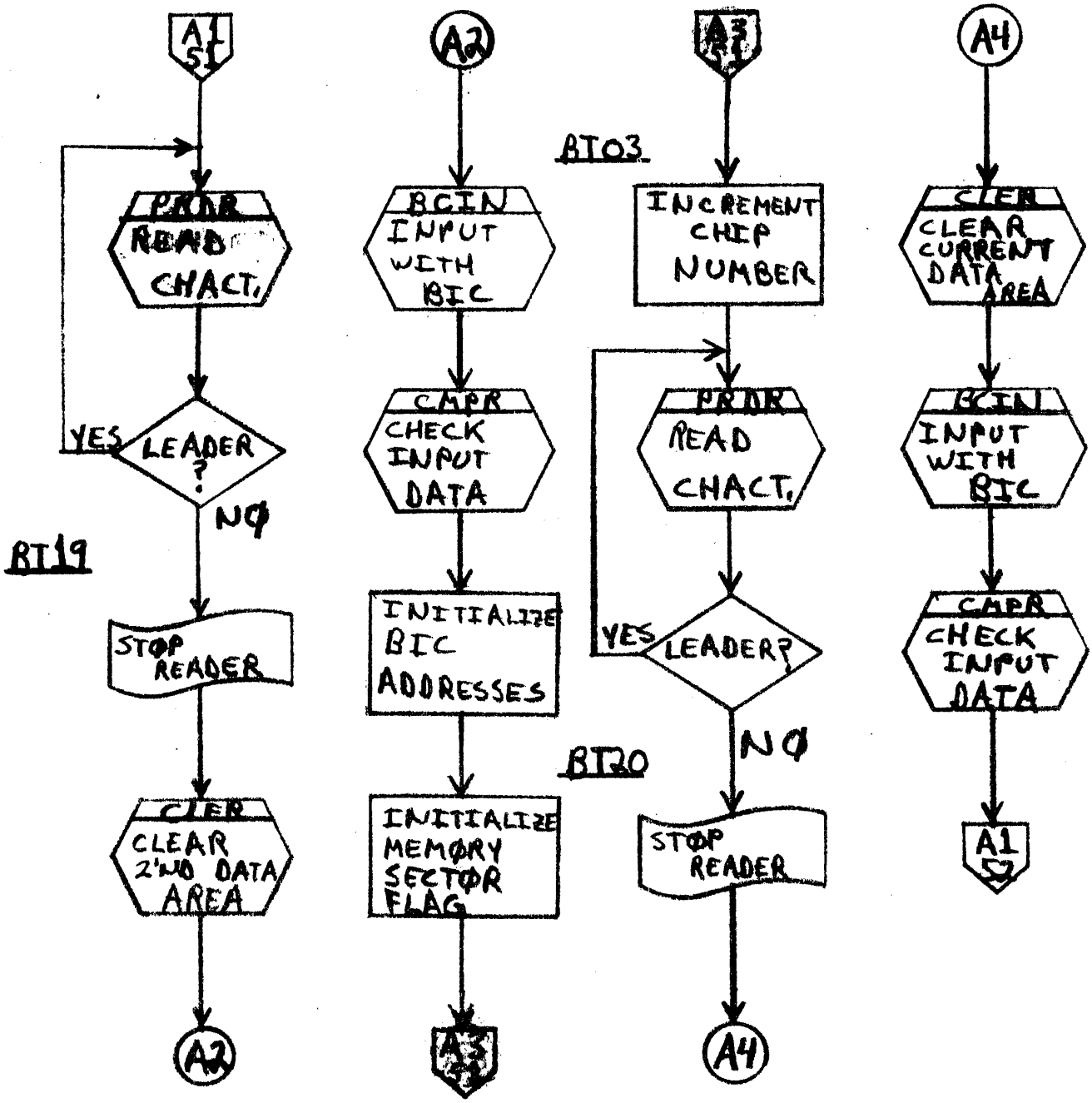
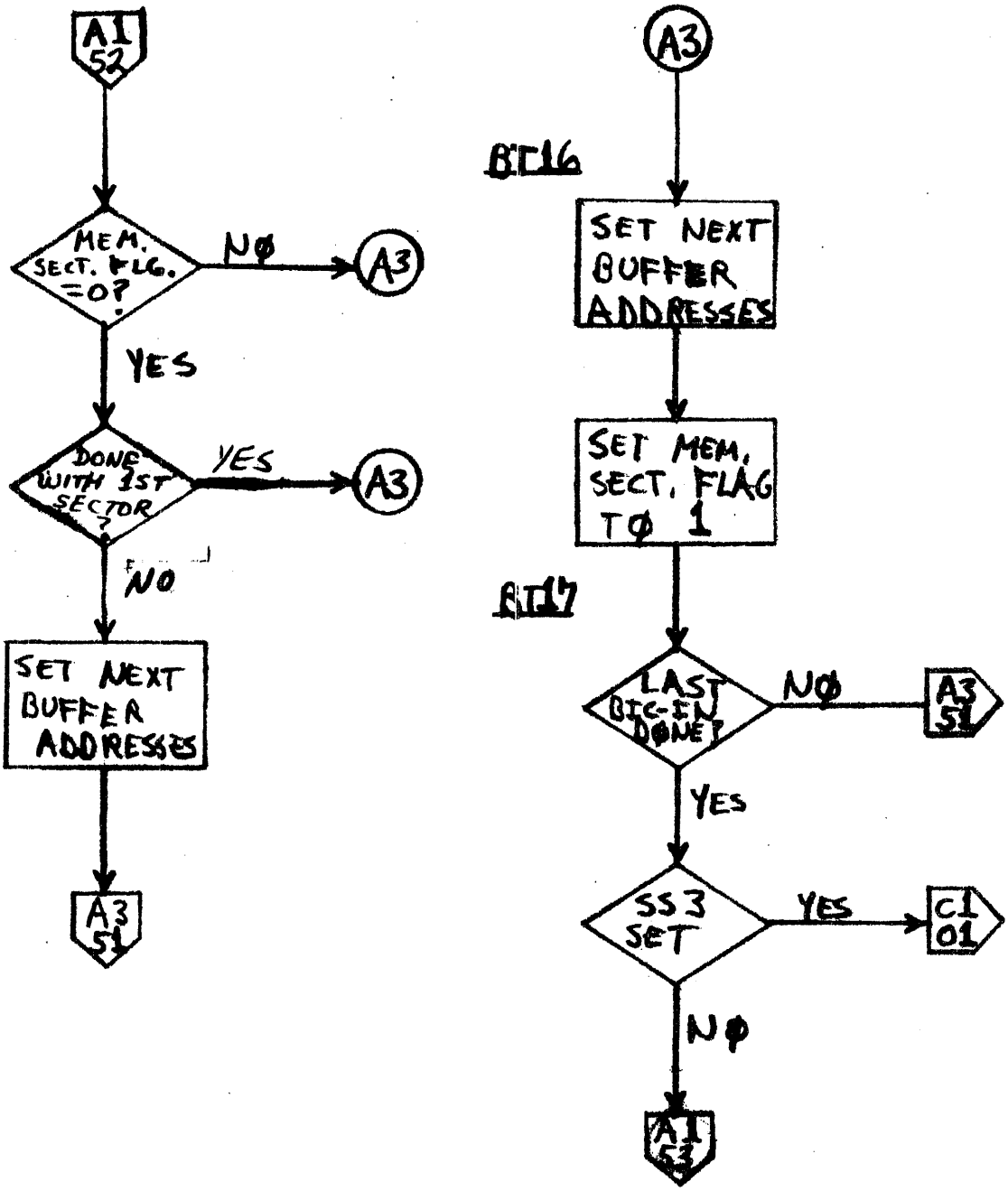
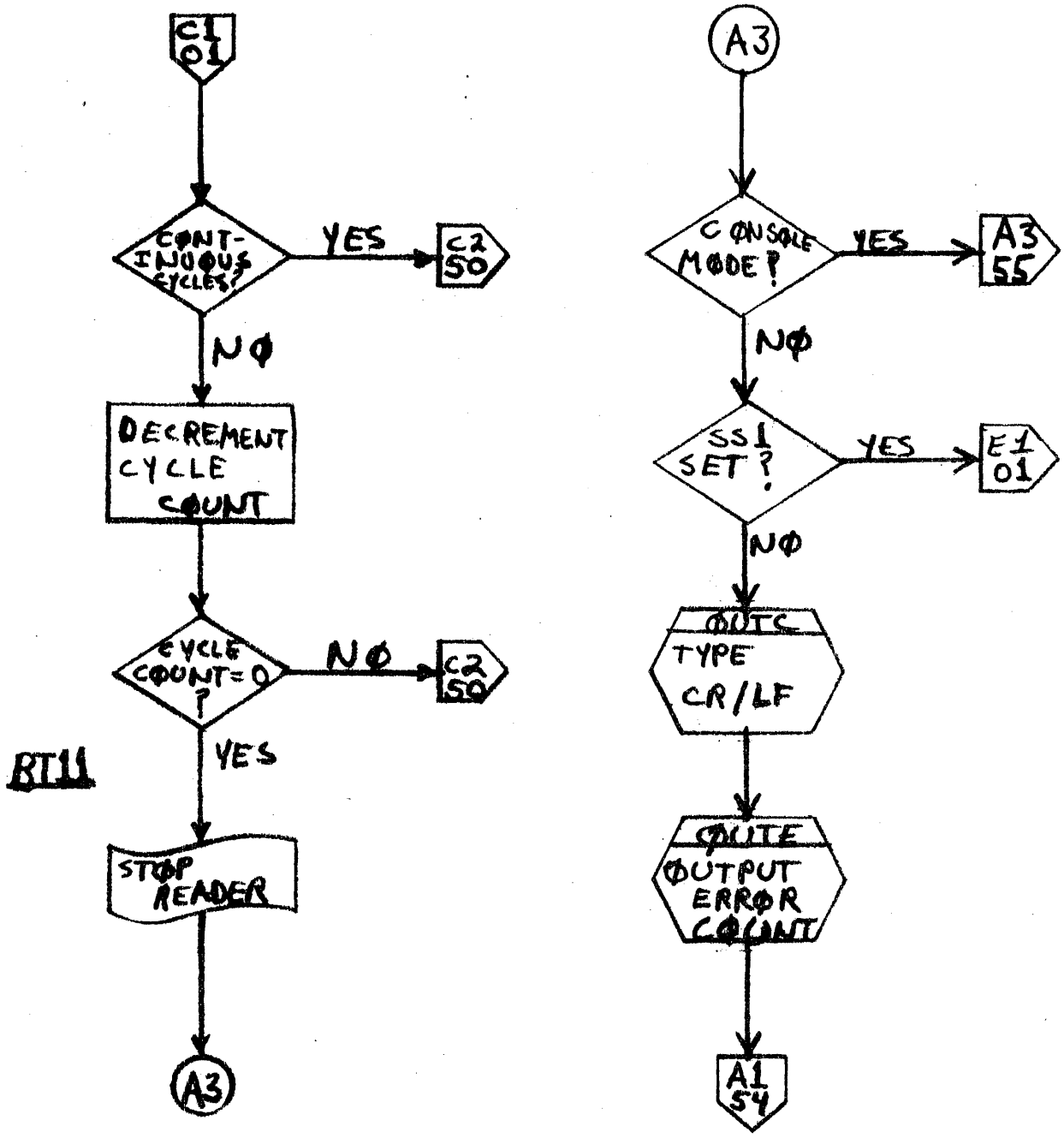

A1 48
ØUTC TYPE CR/LF
ØUTD REQUEST INTERRUPT MASK
INVALID ØR ABØRT RETURN
INPG GET INTERRUPT MASK
SS3 RET.
C1 01
NØRMAL RETURN
STØRE MASK
A2
A2
ØUTC TYPE CR/LF
SET PIM PARAMETER FLAG TØ 1
B2 48
BTØ6
ØUTD REQUEST CYCLE COUNT
INVALID ØR ABØRT RETURN
INPG GET CYCLE COUNT
SS3 RET.
C1 01
NØRMAL RETURN
STØRE CYCLE COUNT
ØUTC TYPE CR/LF
E1 50

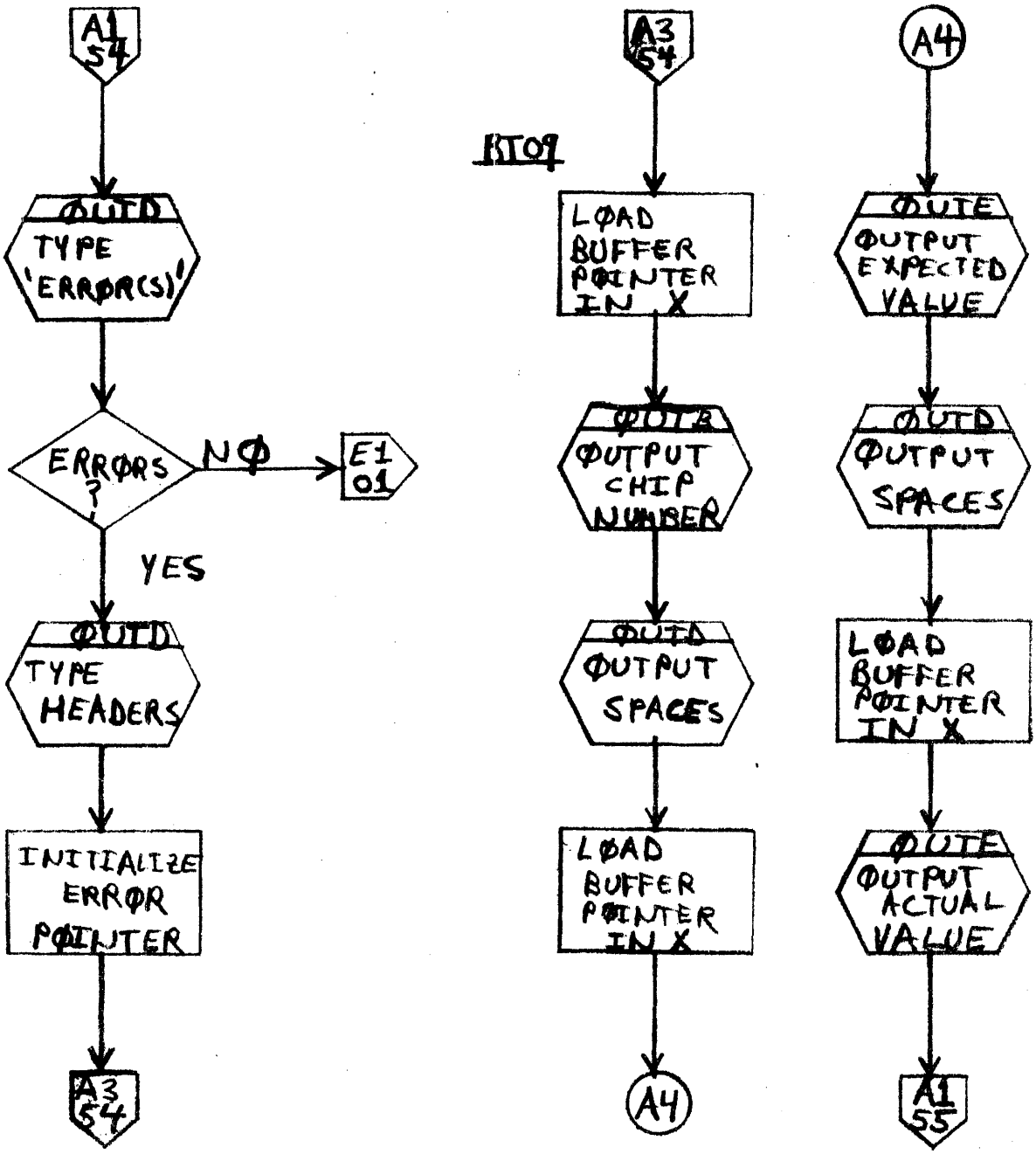

A1 49
BT01
SET REGISTER DEFAULTS
HALT, USER ENTERS I/O MODE & BIC DA
STORE VALUES
PIM USED?
NO
A1 50
YES
A3
A3
PIM PARAM. FLG=0
NO
A1 50
YES
SET REGISTER DEFAULTS
HALT, USER ENTERS PIM PARAMETERS
STORE VALUES
SET PIM PARAM. FLAG TO 1
A1 50

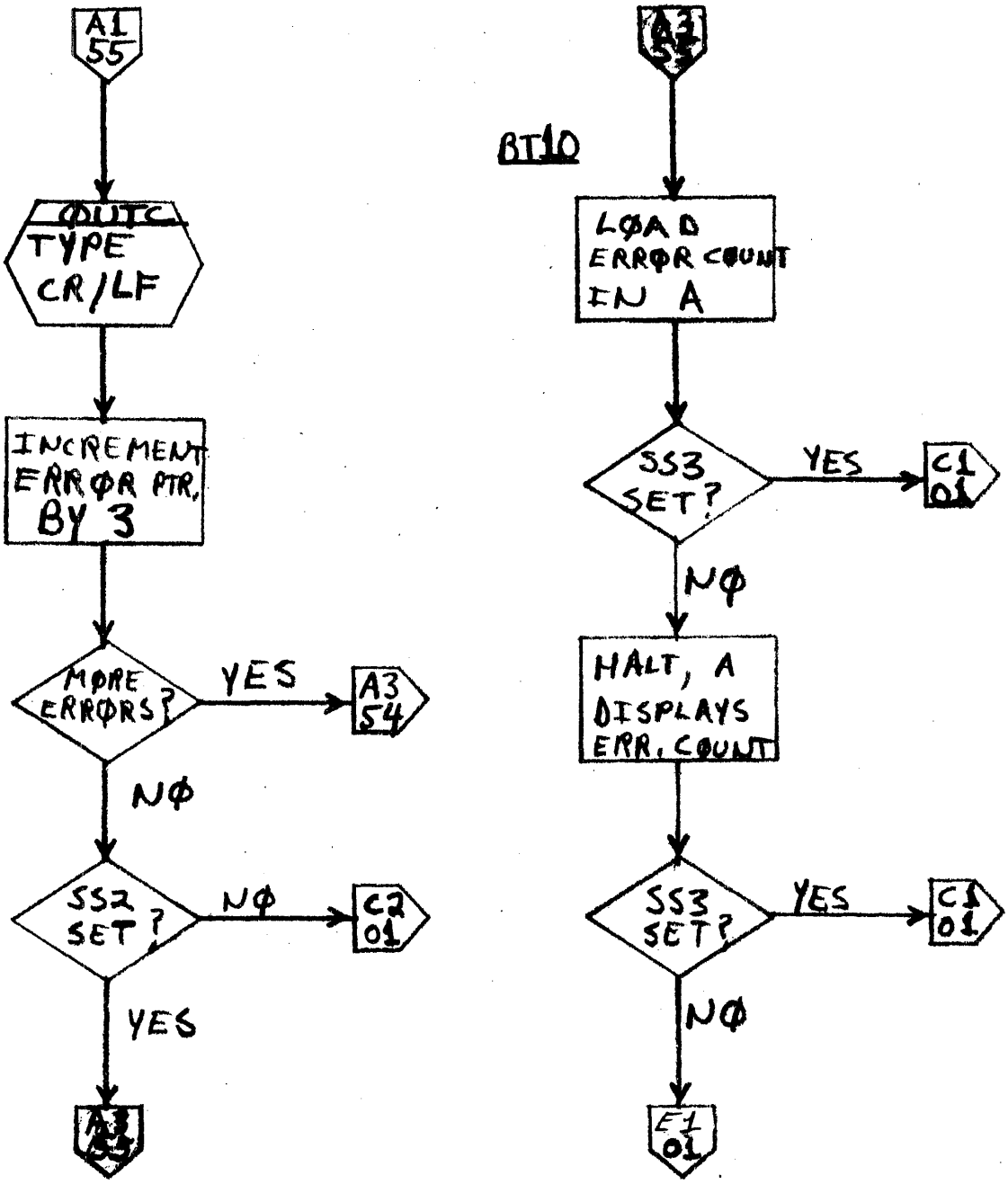

A1 50
A2
A3
A4
BT07
SET REGISTER DEFAULT
INITIALIZE ERROR BUFFER POINTER
PRDR
READ CHACT.
BCIN
BIC-IN TO 1'ST DATA AREA
C2 50
BT08
HALT, USER SETS A TO CYCLE COUNT
INITIALIZE CHIP NUMBER
LEADER?
YES
CMPR
COMPARE INPUT CHA-CTS WITH EXPECTED
BT13
NO
E1 50
STORE VALUE
SET SENSE MODE FOR LEADER
STOP READER
INCREMENT CHIP NUMBER
BT02
CLER
CLEAR ERROR BUFFER
SET FLAG TO CONTIN. READ
CLER
CLEAR 1ST DATA AREA
A1 51
A2
A3
A4


A1
51
PRDR
READ CHACT.
YES
LEADER ?
NO
BI19
STOP READER
CLER
CLEAR 2'ND DATA AREA
A2
A2
BCIN
INPUT WITH BIC
CMPR
CHECK INPUT DATA
INITIALIZE BIC ADDRESSES
INITIALIZE MEMORY SECTOR FLAG
A3
BI03
INCREMENT CHIP NUMBER
PRDR
READ CHACT.
YES
LEADER?
NO
BI20
STOP READER
A4
A4
CLER
CLEAR CURRENT DATA AREA
BCIN
INPUT WITH BIC
CMPR
CHECK INPUT DATA
A1

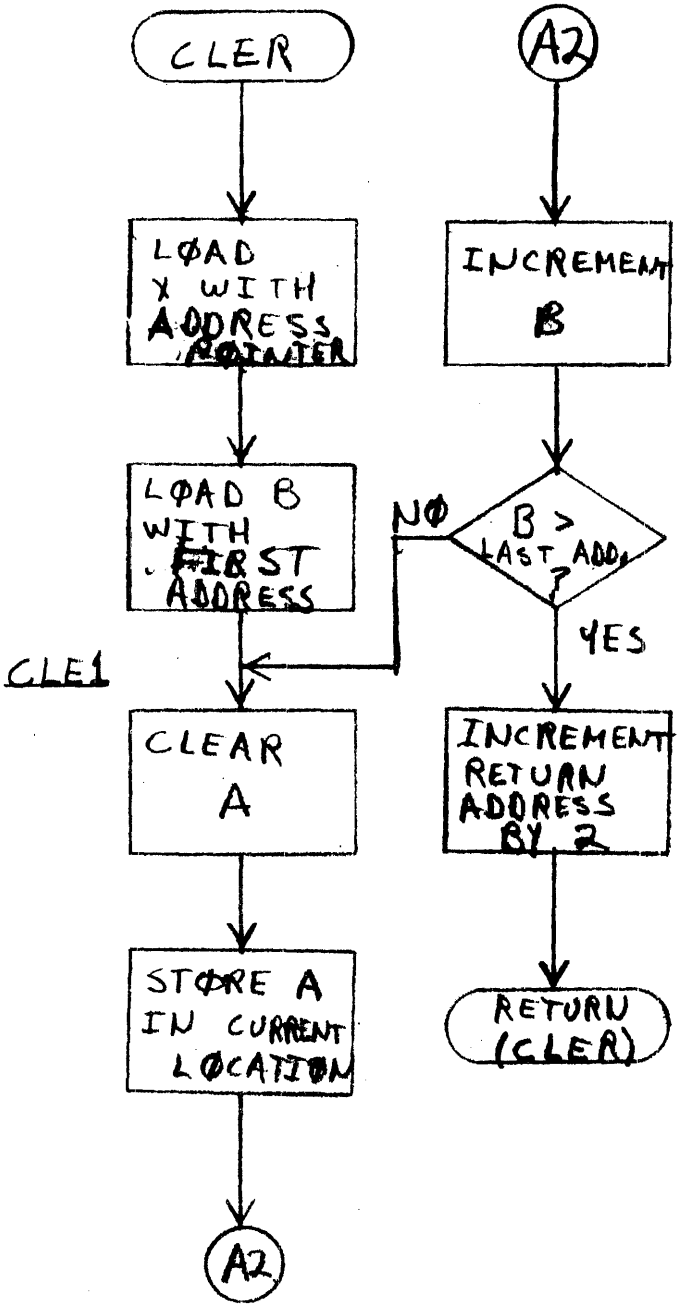

A1
52
MEM. SECT. FLG. =0?
NØ
A3
YES
DONE WITH 1ST SECTOR?
YES
A3
NO
SET NEXT BUFFER ADDRESSES
A3
51
A3
BIT 16
SET NEXT BUFFER ADDRESSES
SET MEM. SECT. FLAG TØ 1
BIT 17
LAST BIC-EN DONE?
NØ
A3
51
YES
SS3 SET
YES
C1
01
NØ
A1
53

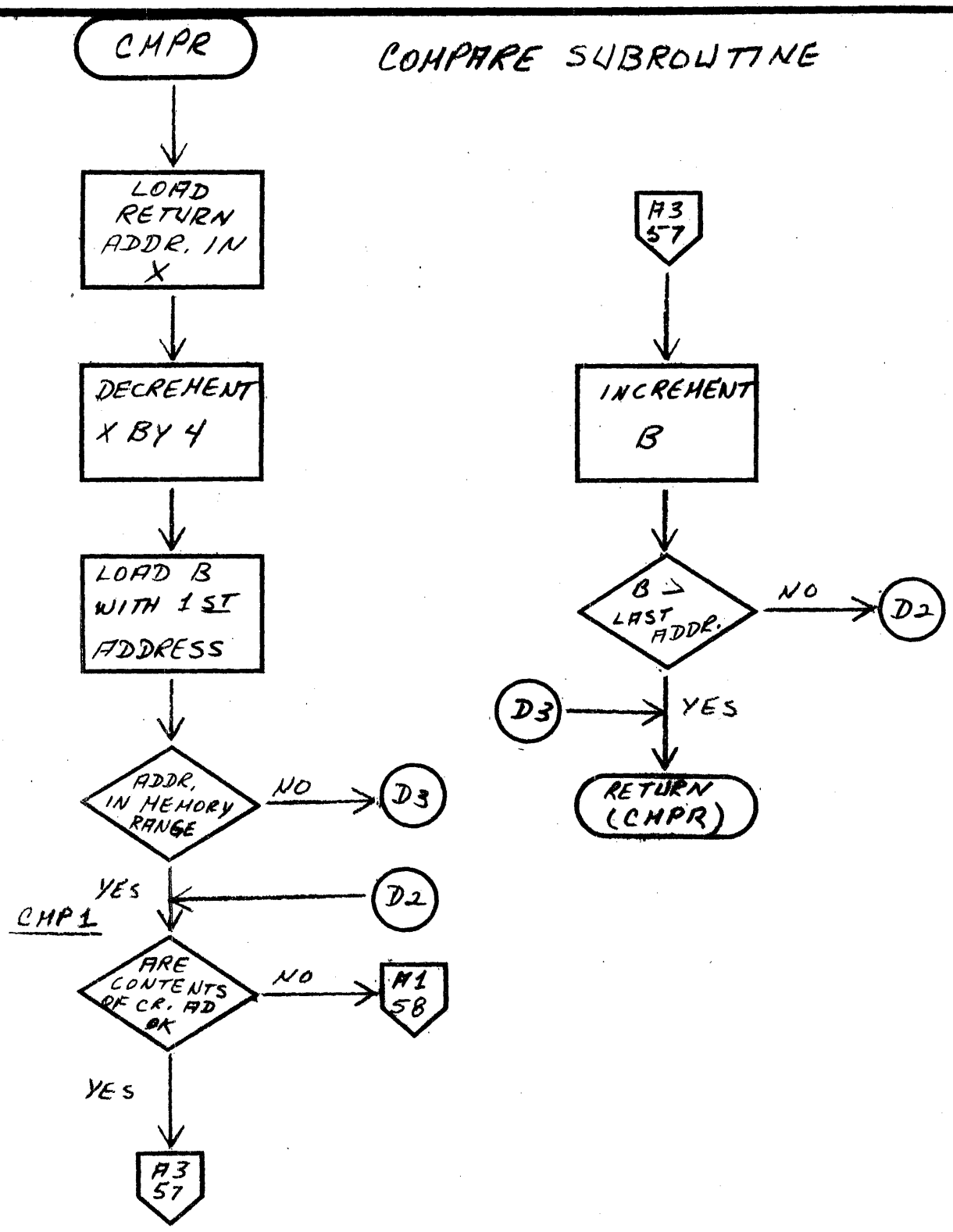

C1 01
CONT-INUOUS CYCLES?
YES
C2 50
NO
DECREMENT CYCLE COUNT
CYCLE COUNT=0 ?
NO
C2 50
YES
STOP READER
A3
RT11
A3
CONSOLE MODE?
YES
A3 55
NO
SS1 SET?
YES
E1 01
NO
OUTS
TYPE CR/LF
QUITE
OUTPUT ERROR COUNT
A1 54


A1 54
ØUTD
TYPE 'ERRØR(S)'
ERRØRS ?
NØ
E1 01
YES
ØUTD
TYPE HEADERS
INITIALIZE ERRØR PØINTER
A3 54
A3 54
KTO9
LØAD BUFFER PØINTER IN X
ØUTR
ØUTPUT CHIP NUMBER
ØUTD
ØUTPUT SPACES
LØAD BUFFER PØINTER IN X
A4
A4
ØUTE
ØUTPUT EXPECTED VALUE
ØUTD
ØUTPUT SPACES
LØAD BUFFER PØINTER IN X
ØUTE
ØUTPUT ACTUAL VALUE
A1 55

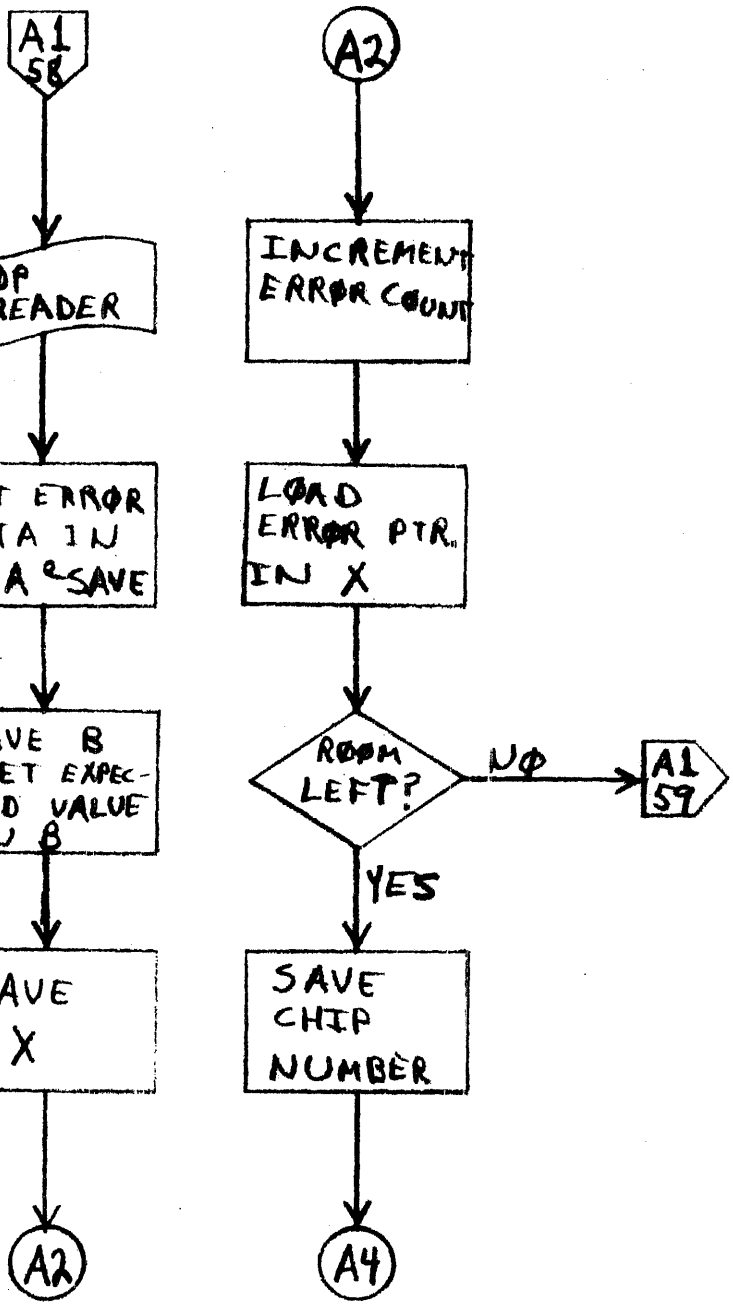

A1
55
ØUTC
TYPE
CR/LF
INCREMENT
ERRØR PTR.
BY 3
MØRE
ERRØRS?
YES
A3
54
NØ
SS2
SET?
NØ
C2
01
YES
A3
55
A3
55
BT10
LØAD
ERRØR COUNT
IN A
SS3
SET?
YES
C1
01
NØ
HALT, A
DISPLAYS
ERR. COUNT
SS3
SET?
YES
C1
01
NØ
E1
01

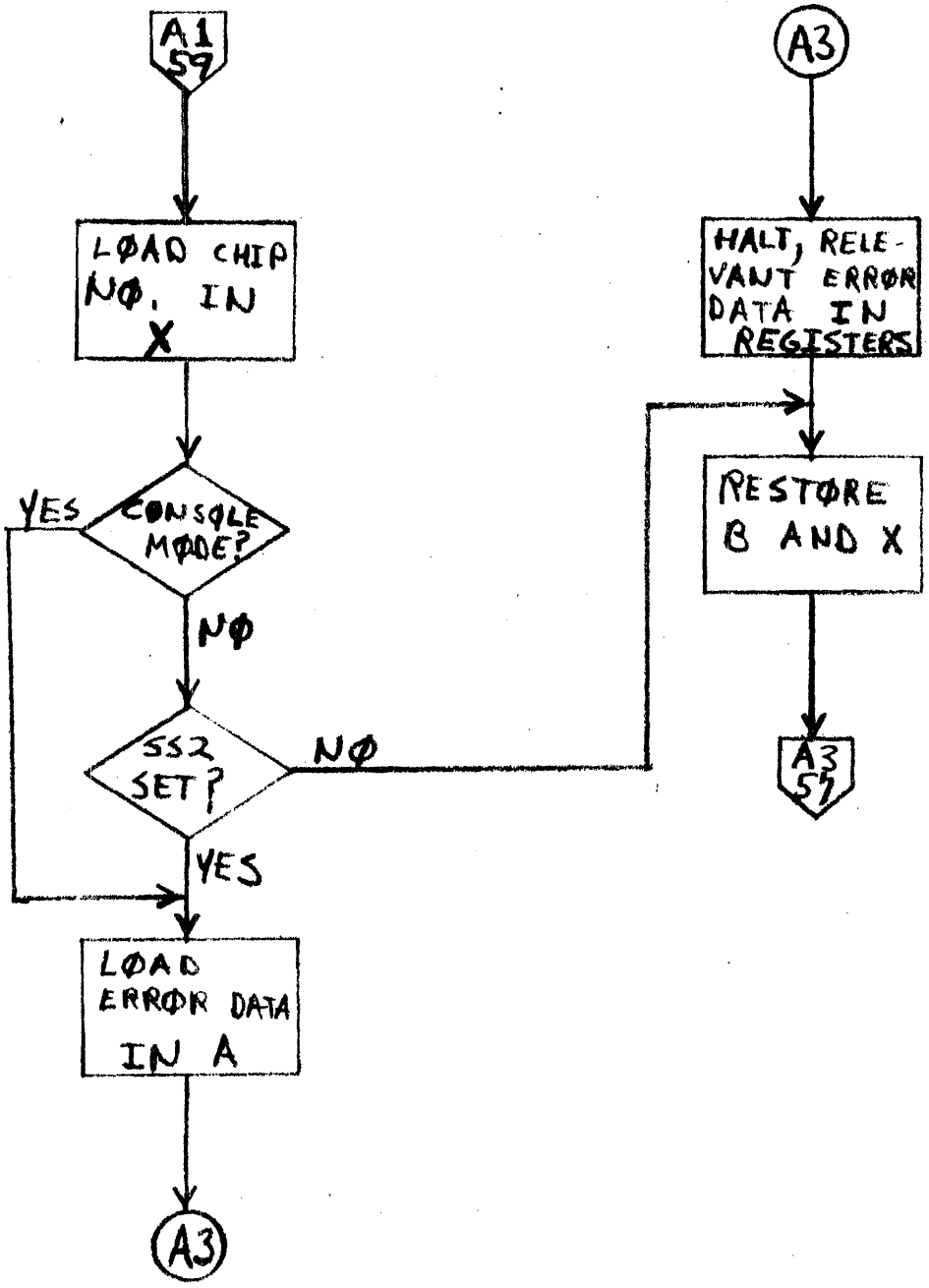
BUFFER CLEARING SUBROUTINE



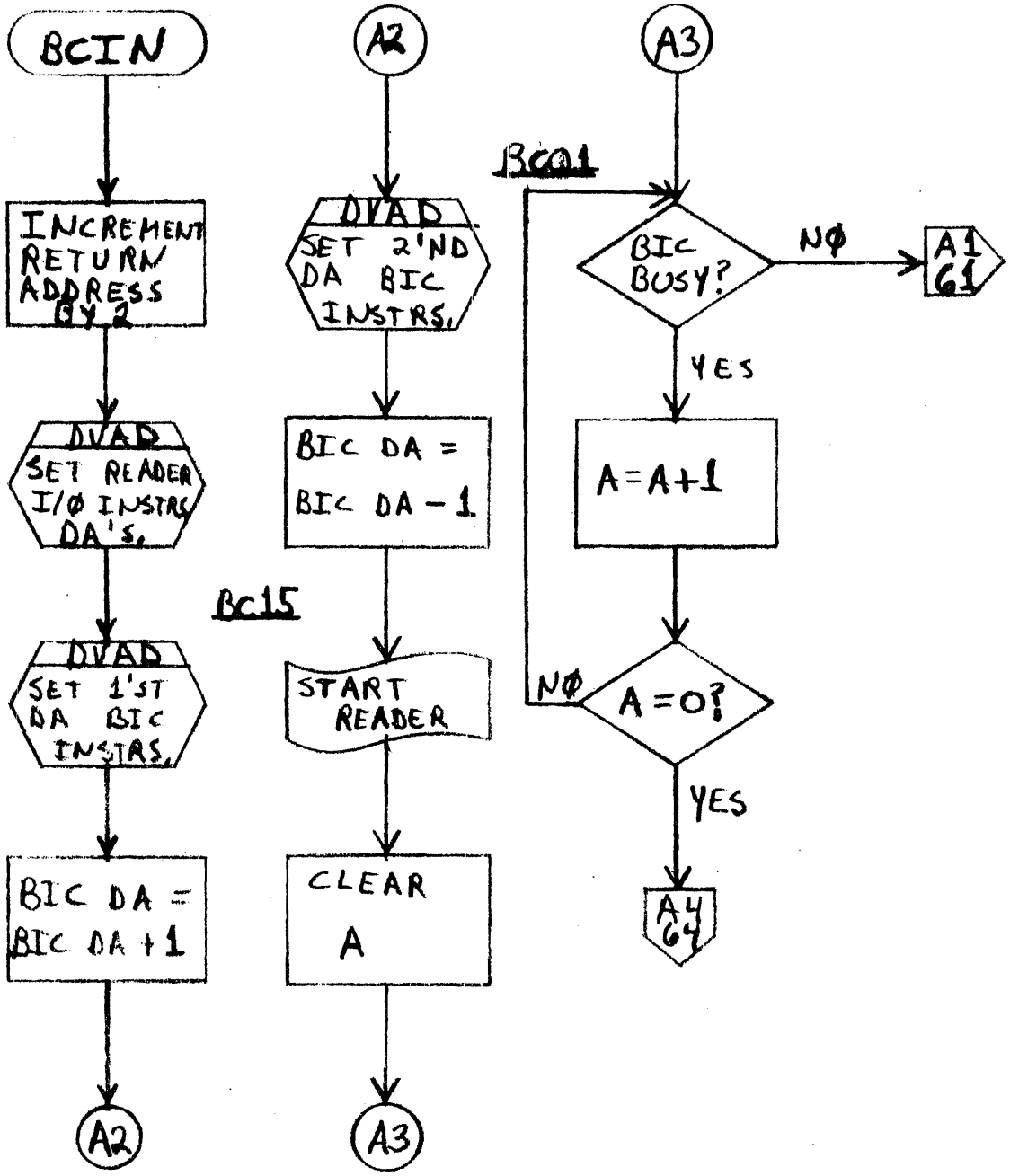

CMPR
COMPARE SUBROUTINE
57
LOAD RETURN ADDR. IN X
DECREMENT X BY 4
LOAD B WITH 1ST ADDRESS
ADDR. IN MEMORY RANGE
NO
D3
YES
D2
CMP 1
ARE CONTENTS OF CR. AD OK
NO
A1 58
YES
A3 57
A3 57
INCREMENT B
B > LAST ADDR.
NO
D2
D3
YES
RETURN (CMPR)

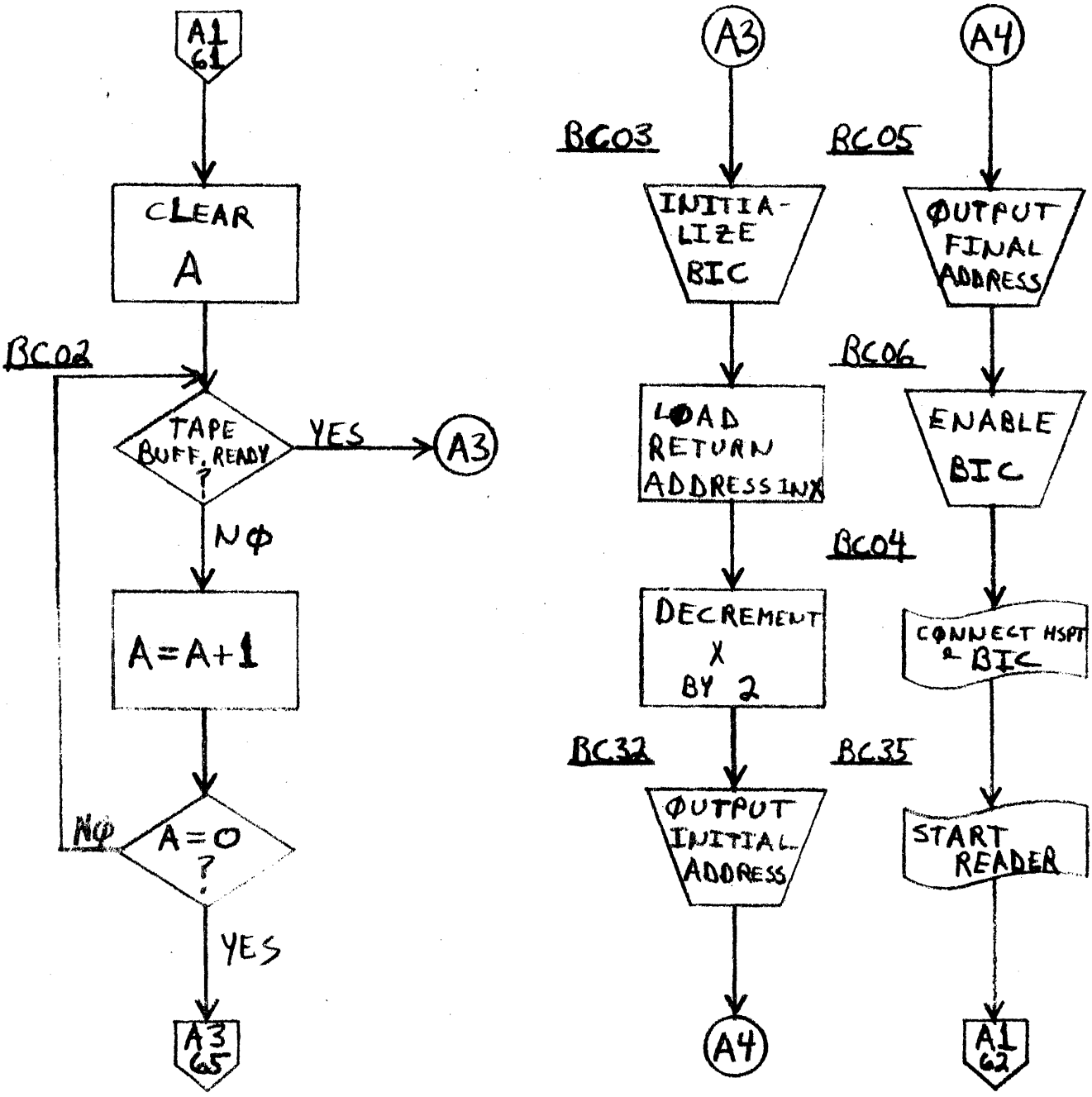
CMP2

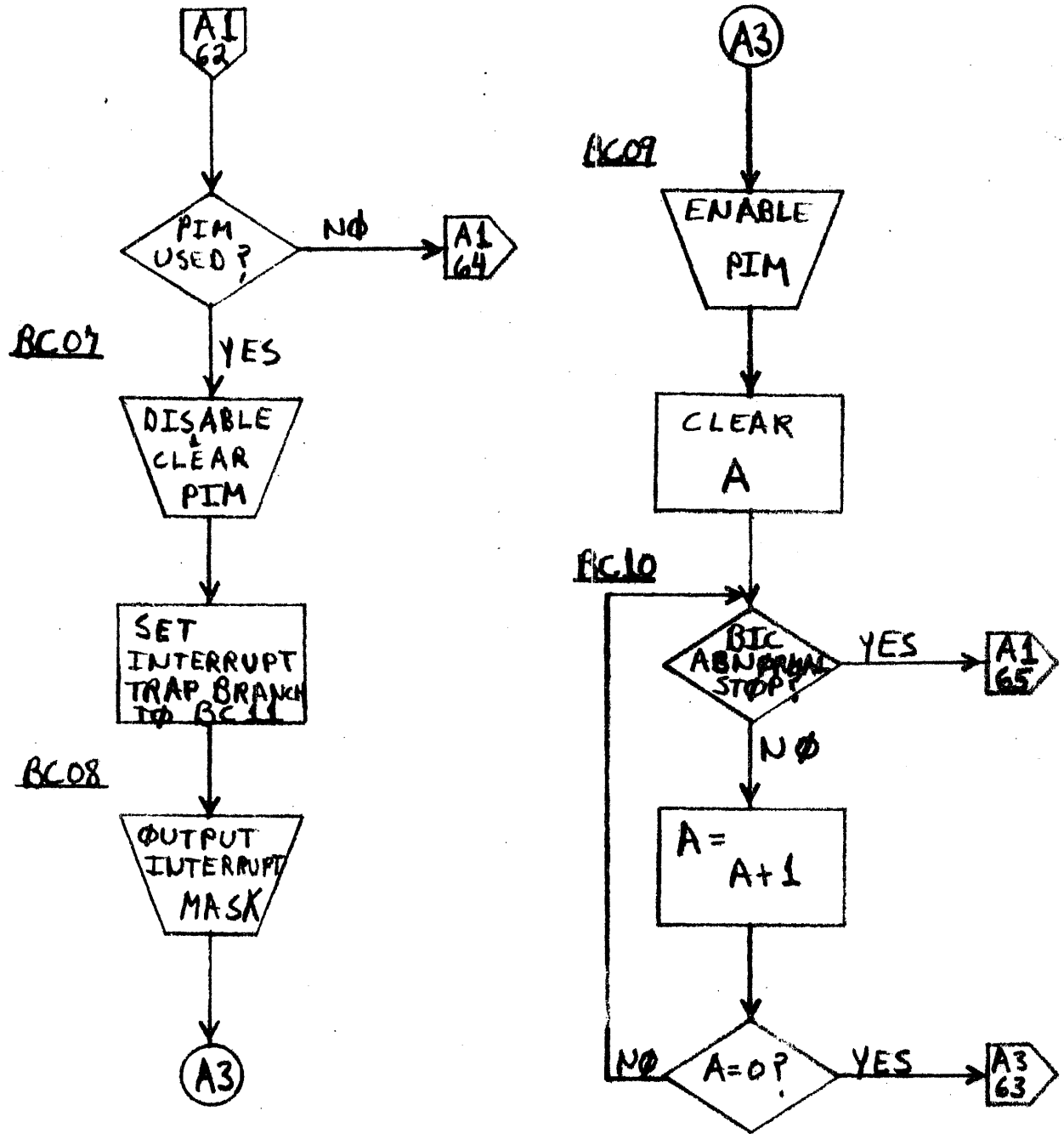

A1
58
STOP READER
GET ERROR DATA IN IN A & SAVE
SAVE B & GET EXPECTED VALUE IN B
SAVE X
A2
A2
INCREMENT ERROR COUNT
LOAD ERROR PTR. IN X
ROOM LEFT?
NO
A1
59
YES
SAVE CHIP NUMBER
A4
A4
SAVE EXPECTED VALUE
SAVE ACTUAL VALUE
INCREMENT ERROR PTR. BY 3
A1
59


A1
59
LØAD CHIP NØ. IN X
YES
CONSOLE MØDE?
NØ
SS2 SET?
NØ
YES
LØAD ERRØR DATA IN A
A3
A3
HALT, RELEVANT ERRØR DATA IN REGISTERS
RESTØRE B AND X
A3
57

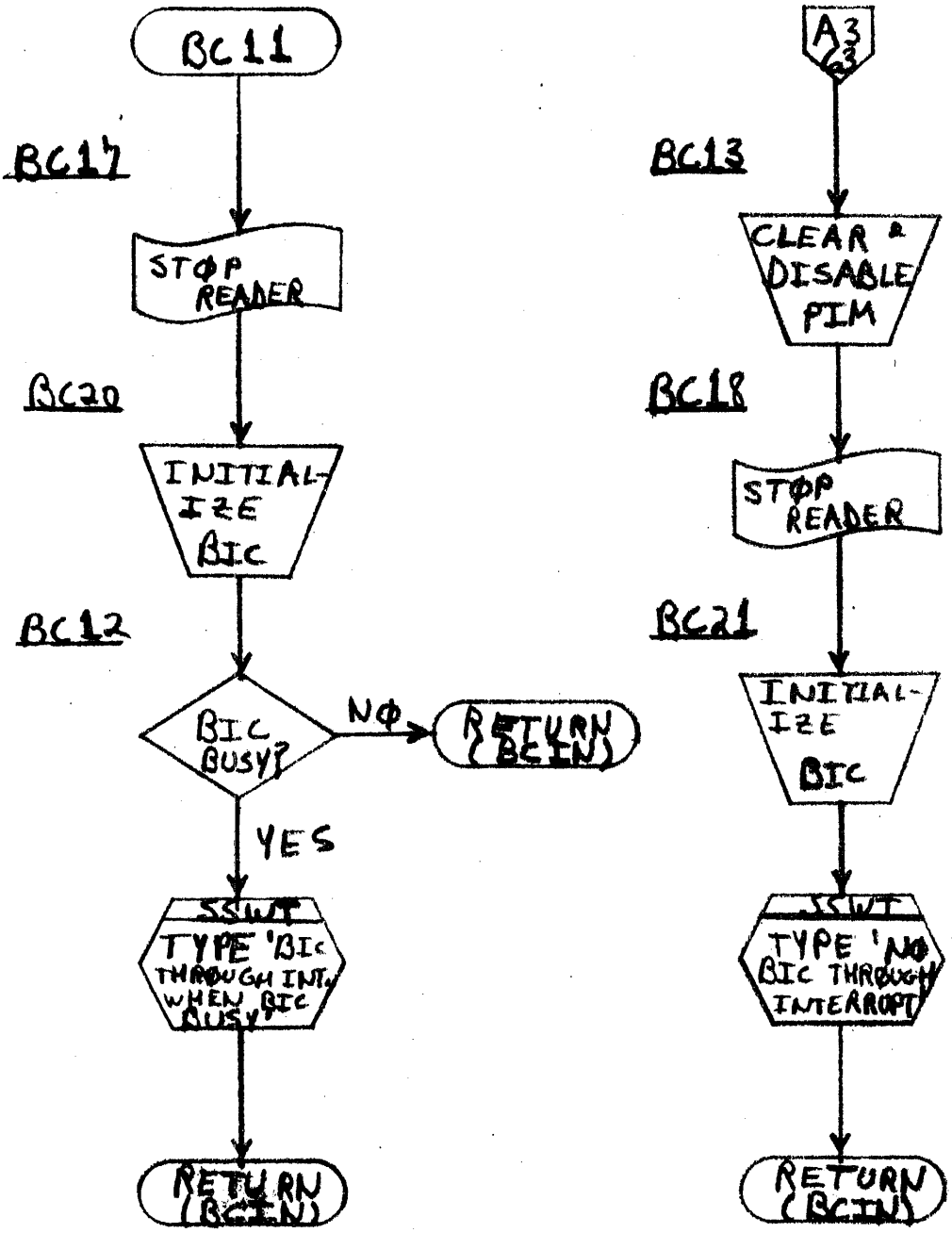
READ (BIC MODE, OPTIONAL END INTERRUPT)

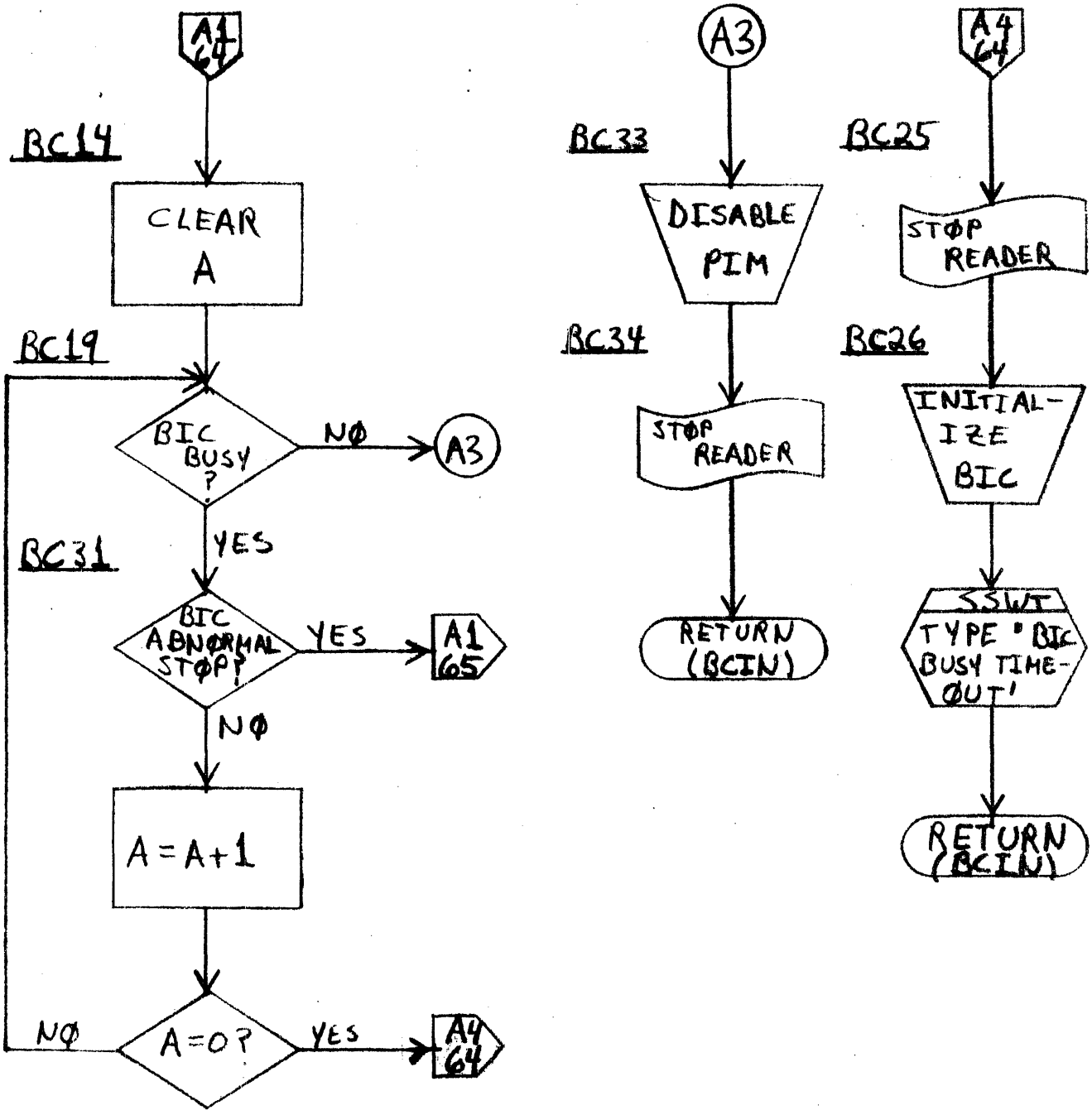


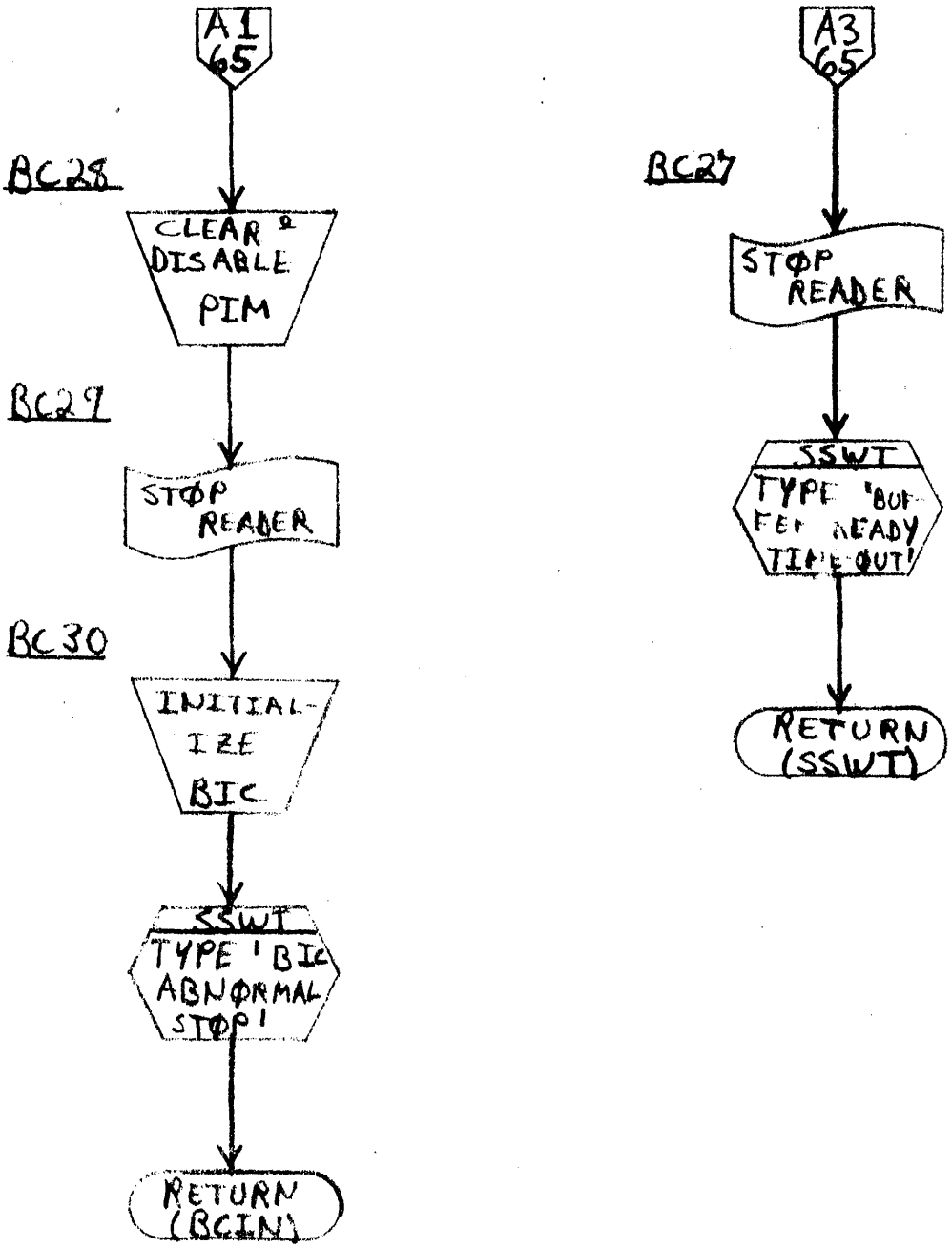

A1
61
CLEAR
A
BC02
TAPE BUFF. READY ?
YES
A3
NO
A=A+1
NO
A=0 ?
YES
A3
65
A3
BC03
INITIA-LIZE BIC
LOAD RETURN ADDRESS INX
DECREMENT X BY 2
BC32
OUTPUT INITIAL ADDRESS
A4
A4
BC05
OUTPUT FINAL ADDRESS
BC06
ENABLE BIC
BC04
CONNECT HSPT & BIC
BC35
START READER
A1
62


A1
62
PIM USED?
NØ
A1
64
YES
BC07
DISABLE
CLEAR
PIM
SET
INTERRUPT
TRAP BRANCH
TO BC11
BC08
OUTPUT
INTERRUPT
MASK
A3
A3
BC09
ENABLE
PIM
CLEAR
A
BC10
BIC
ABNORMAL
STOP?
YES
A1
65
NØ
A=
A+1
NØ
A=0?
YES
A3
63

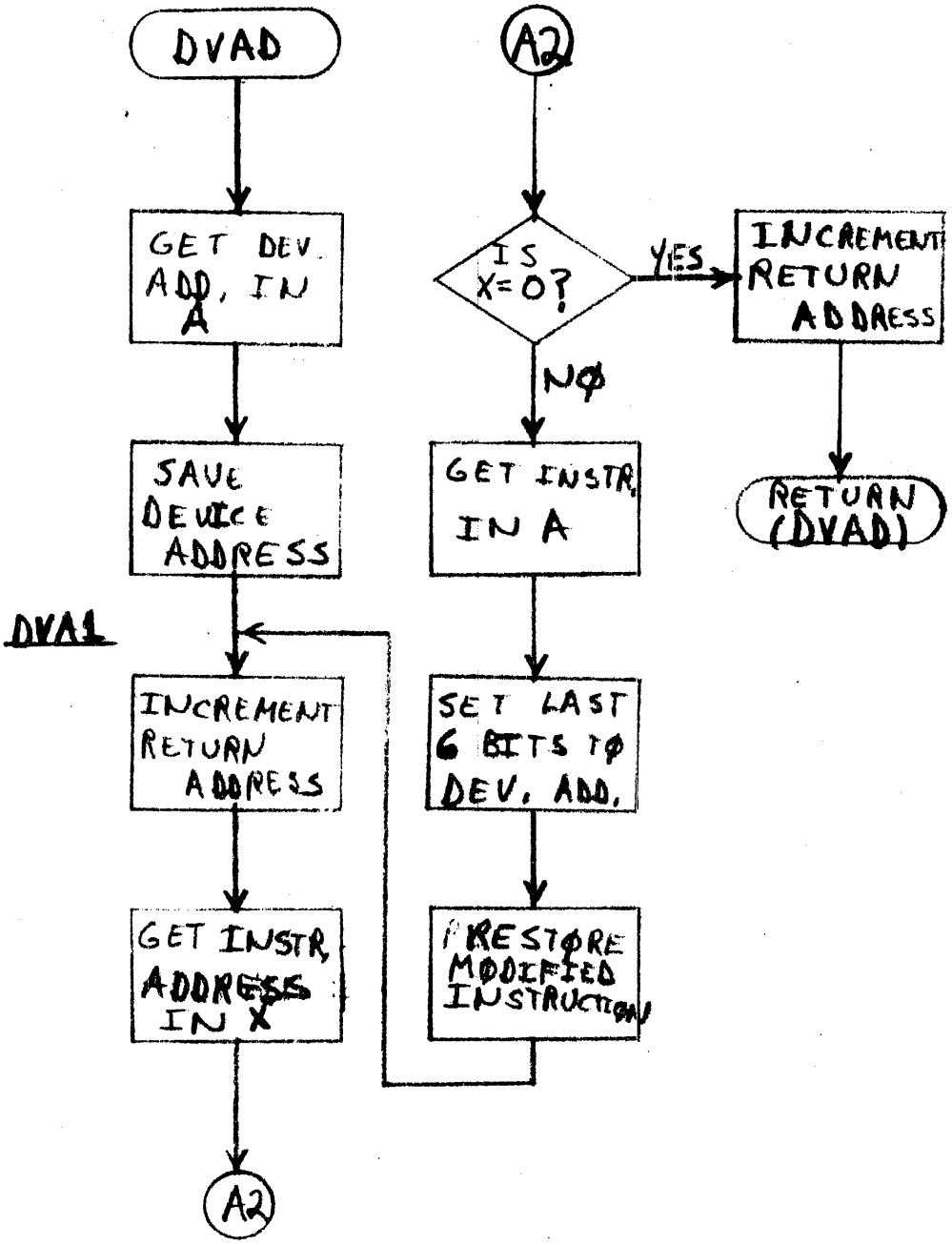
BIC-THROUGH INTERRUPT ENTRY




A1 64
BC14
CLEAR A
BC19
BIC BUSY ?
NØ
A3
YES
BC31
BIC ABNØRMAL STØP?
YES
A1 65
NØ
A=A+1
A=0?
NØ
YES
A4 64
A3
BC33
DISABLE PIM
BC34
STØP READER
RETURN (BCIN)
A4 64
BC25
STØP READER
BC26
INITIAL-IZE BIC
SSWT
TYPE "BIC BUSY TIME-ØUT"
RETURN (BCIN)


A1
65
BC28
CLEAR & DISABLE PIM
BC29
STOP READER
BC30
INITIAL-IZE BIC
SSWT
TYPE 'BIC ABNORMAL STOP'
RETURN (BCIN)
A3
65
BC27
STOP READER
SSWT
TYPE 'BUF-FER READY TIME-OUT'
RETURN (SSWT)

DEVICE ADDRESS SETTER



SECTION 4
TEST SPECIFICATIONS

4.1 OBJECTIVES

The purpose of this section is to describe to what extent the program has been validated in termsof variations in applicable hardware, configurations and other external input parameters. Using the teletype mode of operation, actual hardcopy of each test variance is presented. This will provide an aid in evaluating future claimed discrepancies observed in the program.

4.2 CONFIGURATIONS

This program has been exercised on the following hardware configurations:

1) 622/i - 16K memory
2) 620/f - 32K memory

4.3 DETAILED DESCRIPTIONS

4.3.1 The following hard copy printout is provided to validate the responses received for each respective input.

```
THIS IS THE 620 TEST EXECUTIVE
MEMORY SIZE IS  16K

L.
620 PAPER TAPE AND BIC TEST

PT PUNCH DA = 37.
PT READER DA =37.
BIC TEST REQUESTED?
N
BIC USED?
N
PIM USED?
N
INPUT TEST TYPE
P.

BIC TEST REQUESTED?
N
BIC USED?
N
PIM USED?
Y
PIM DA =40.
TRAP LOCATION = 100.
INTERRUPT MASK =376.
INPUT TEST TYPE
P,
INPUT LOWER DATA LIMIT, UPPER DATA LIMIT, AND DATA BLOCK SIZE
0,20,34.
CYCLES =3.

BIC TEST REQUESTED?
N
BIC USED?
Y
BIC DA =22.
INPUT TEST TYPE
P.

BIC TEST REQUESTED?
N
BIC USED?
N
PIM USED?
N
INPUT TEST TYPE
R.
TIME DELAY =400000.
000000 ERROR(S)
```

```
BIC TEST REQUESTED?
N
BIC USED?
N
PIM USED?
Y
INPUT TEST TYPE
R.
TIME DELAY =100000.
000000 ERROR(S)

BIC TEST REQUESTED?
N
BIC USED?
N
PIM USED?
N
INPUT TEST TYPE
N  INVALID
INPUT TEST TYPE
H.
000000 ERROR(S)

BIC TEST REQUESTED?
N
BIC USED?
N
PIM USED?
Y
INPUT TEST TYPE
H.
000000 ERROR(S)
```

```
BIC TEST REQUESTED?
N
BIC USED?
Y
INPUT TEST TYPE
H.
000000 ERROR(S)

BIC TEST REQUESTED?
N
BIC USED?
N
PIM USED?
N
INPUT TEST TYPE
R.
TIME DELAY =0.
000124 ERROR(S)
EXPECTED     ACTUAL
000000       000001
000001       000002
000002       000003
000003       000004
000004       000005
000005       000006
000006       000007
000007       000010
000010       000011
000011       000012
```

```
BIC TEST REQUESTED?
N
BIC USED?
N
PIM USED?
Y
INPUT TEST TYPE
H.
000123 ERROR(S)
EXPECTED     ACTUAL
000001       000000
000002       000001
000003       000002
000004       000003
000005       000004
000006       000005
000007       000006
000010       000007
000011       000010
000012       000011

BIC TEST REQUESTED?
N
BIC USED?
Y
INPUT TEST TYPE
H.
```

```
620 PAPER TAPE AND BIC TEST

PT PUNCH DA = 37.
PT READER DA =37.
BIC TEST REQUESTED?
N
BIC USED?
Y
BIC DA =
PT PUNCH DA = 37.
PT READER DA =37.
BIC TEST REQUESTED?
N
BIC USED?
N
PIM USED?
Y
PIM DA =40.
TRAP LOCATION = 100.
INTERRUPT MASK =376.
INPUT TEST TYPE
R.
TIME DELAY =0.
000123 ERROR(S)
EXPECTED     ACTUAL
000001       000000
000002       000001
000003       000002
000004       000003
000005       000004
000006       000005
000007       000006
000010       000007
000011       000010
000012       000011
```

```
BIC TEST REQUESTED?
Y
PIM USED?
N
CYCLES =1.

000005 ERROR(S)
SECTION    EXPECTED     ACTUAL
   1         000220      000221
   2         000102      000103
   3         000000      000001
   5         000000      000001
   7         000220      000221

BIC TEST REQUESTED?
Y
PIM USED?
N
CYCLES =1.

000006 ERROR(S)
SECTION    EXPECTED     ACTUAL
   1         000220      000221
   2         000102      000103
   3         000000      000001
   5         000000      000001
   7         000220      000221
   7         000222      000223

BIC TEST REQUESTED?
N
BIC USED?
N
PIM USED?
N
INPUT TEST TYPE
P,
INPUT LOWER DATA LIMIT, UPPER DATA LIMIT, AND DATA BLOCK SIZE
377,377,1.
CYCLES =1.

BIC TEST REQUESTED?
N
BIC USED?
N
PIM USED?
N
INPUT TEST TYPE
P,
INPUT LOWER DATA LIMIT, UPPER DATA LIMIT, AND DATA BLOCK SIZE
220,377,160.
CYCLES =1.

BIC TEST REQUESTED?
```

DWG NO 98A0945

REVISIONS			
SYM	DESCRIPTION	APPROVED	DATE
A	PRODUCTION RELEASE PER EN 82248	[illegible]	[illegible]

Note: Unless otherwise specified:

This document also applies to the:

E-2993, 300 CPM Card Reader Special Option

E-2747, 600 CPM Card Reader Special Option

E-2382, 1000 CPM Card Reader Special Option

Addendum 1	Describes 600 CPM spec and timing differences (E-2747)
Addendum 2	Describes 1000 CPM spec and timing differences (E-2382)
Addendum 3	Described 300 CPM Mark Sense Option (E-2993)

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T. Sweere, Director
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DSGN	
ENGR J. Hennessey	1-3-73
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APPD [illegible]	7/17/73

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varian data machines /a varian subsidiary
2722 michelson drive / irvine / california / 92664

TITLE

ENGINEERING DESCRIPTION (MAINTENANCE AID)
CARD READER CONTROLLER
MODEL 620-28

CODE IDENT NO.	SIZE	DWG NO.	REV
21101	A	98A0945	A

SCALE

SHEET 1 OF 32

98A0153-V06

ENGINEERING DATA FORM

OPTION	300 CPS Card Reader Controller
MODEL	620-28
NO. OF LOGIC CARDS REQ'D.	1
NO. OF CARD SLOTS REQ'D.	3
LOCATION OF SLOTS (NUMBERING)	Any
CONNECTORS REQ'D. (EXCLUDING I/O)	1
KEYING	None
ST'D. DEVICE ADDRESS	30
WIRELIST NUMBER	95W0998
MANUAL PUBLICATIONS NUMBER	This document
PERIPHERAL EQUIPT. REQ'D	Card Reader
MFG'R.	Documation, Inc.
MODEL	M200
GEN'L. SPECS	300 cards per minute

NOTES:

Drawings:	
Option Drawing	01P1533
Assy., Controller	44P0684
Procurement Spec.	35A0106
Cable Drawing	53P0735
Logic Diagrams	91C0455
Test Specification	98A0946
Test Program	92A0107-012 *

Note: Unless otherwise specified, the timing and general information in this drawing pertains to the 620-38 card reader system.

*Use rev. D or C reader if initialize is to be tested.

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ILLUSTRATIONS

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TABLES

SECTION 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The Varian Data Machines model 620-28 Card Reader Controller is a special peripheral computer option that interfaces the 620 or 7X computer to the card reader specified by Procurement Specification 35A0106.

The controller is packaged on a wire wrapped plug in module which can be installed in a 620 peripheral controller chassis. The controller is compatible with the 620 Buffer Interlace Controller (BIC) and the Priority Interrupt Module (PIM).

1.2 FUNCTIONAL DESCRIPTION

References: Logic Diagram 91C0455
VDM Computer Manual 620 or V7X Series
Documation Instruction Manual

The controller performs the timing and logical functions required to transfer 80 twelve bit columns of data from the card reader to the CPU at a speed of 300 cards per minute (CPM) ± 10%.

1.2.1 Device Address

The assigned device address is 30. The address is decoded from EB00 thru EB05 and signal IUAX (Computer Interrupt Acknowledge). Signals EB00 thru EB02 are made available on the wire wrap connectors at the backplane. This allows the desired device address to be hand wired on the backplane connector and provides the capability of easily changing the device address to any address between 30 and 37, if needed.

1.2.2 External Control Commands (EXC)

There are three external control (EXC) commands: Initialize Controller, Read One Card, and Continuous Feed. These commands are mechanized as follows:

The device address and EB11 allows the Computer Function Ready (FRYX) pulse to be applied to the function decode gates. Lines EB06 thru EB08, which contain the function code, are also applied to these gates. The decoded function lines enable the applicable function control circuits.

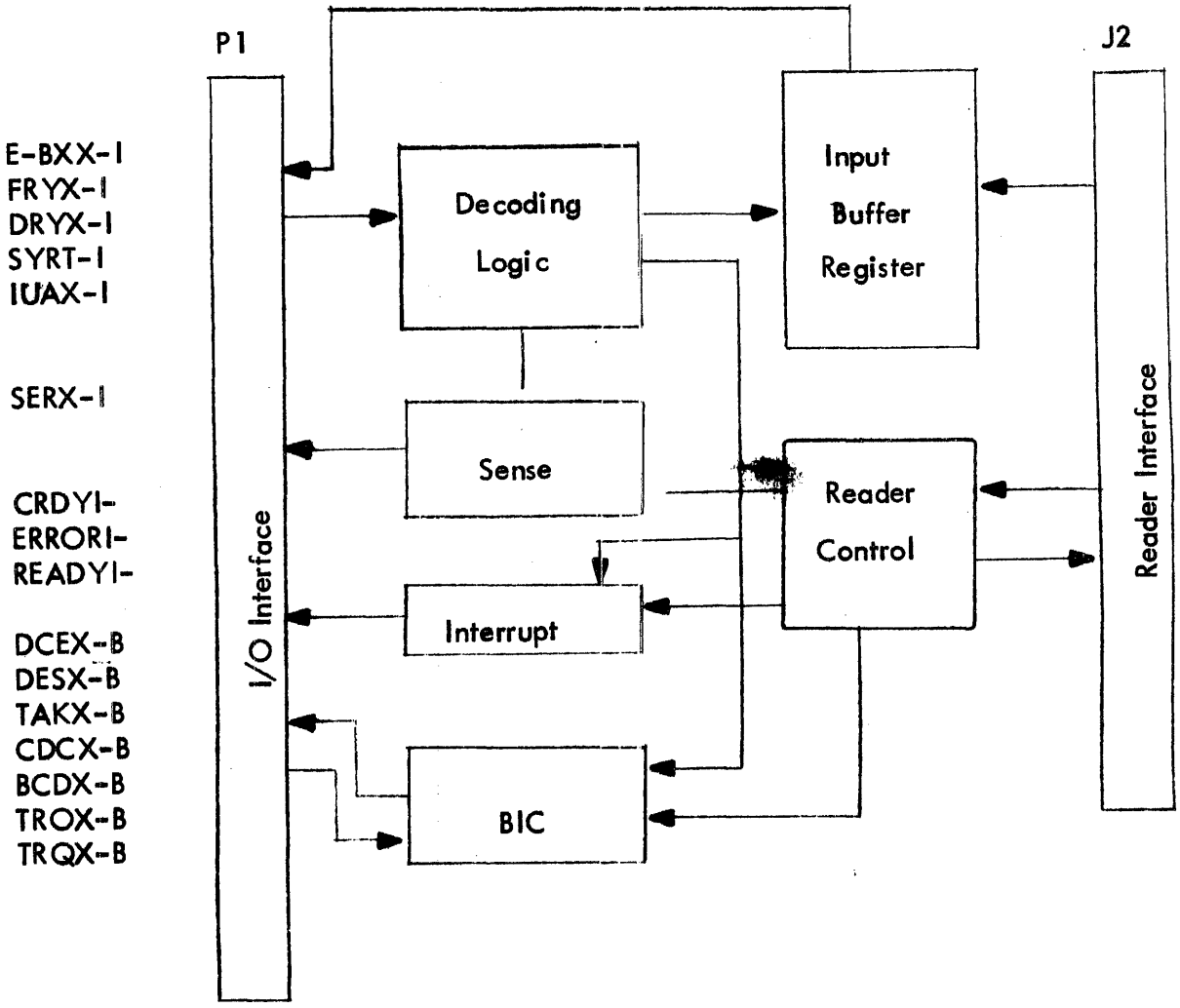


FIGURE 1.1 - CONTROLLER BLOCK DIAGRAM

1.2.3 Data Transfer In (CIA, CIB, INA, INB, IME)

A 12 bit data word is clocked into the input register (DIXX) by INDEX+ pulse from the reader. Data is then transferred to the CPU as follows:

The control logic may be activated from the BIC signal BCIE or from the computer signal DTIE. Either of these terms arms the data transfer in flip-flop DTIX. This flip-flop is then set by the trailing edge of FRYX+ and reset by the trailing edge of DRYX+. DTIX then strobes in the 12 bit data DIXX onto the E-Bus.

1.2.4 BIC Control Logic

Once the BIC is connected to the computer, it sends out signal DCEX+, which enables the set gate of flip flop CDCX. EXC read one card will then set flip flop CDCX. Term CDCX is then returned to BIC, indicating that data transfer is under control of the BIC.

When a data word is ready (BRDY) to be transferred to the computer, term TRQX-B is forced to a logic 0. The BIC responds by forcing the transfer acknowledge term TAKX-B to a logic 0. The BIC acknowledge term BICE- then goes to a logic 0. This signal is then used to enabled data transfer in flip flop DTIX.

1.2.5 Sense Response Logic (SEN)

There are five sense responses to the computer: Character Ready, Read Error, Hopper Empty, Reader Ready, and Card Image.

The sense response that the computer is looking for is enabled by decoding E-Bus lines EB06 thru EB08, the device address, and EB12+. SERX-I will go true (logic zero) if the indicated response is true.

1.2.6 Interrupts

There are three interrupts made available at the backplane, pin P1-75, 77, and 79. These interrupts are the integrated leading edge of Character Ready (CRDYI-), Card Reader Error (ERRORI-), and Card Reader Ready (READYI-), respectively. Card Reader Ready Interrupt also designates end of card image. (ready for EXC2 command).

1.3 LOGICAL DESCRIPTION

The listed program will generate the timing sequences shown in Figure 1.3.

Location	Description	Code
0	EXC Initialize	100030 *
1	Sense Reader Ready	101630
2	5	000005
3	Jump	001000
4	1	000001
5	EXC Feed One Card	100230
6	Sense Character Ready	101130
7	14	000014
10	Sense Reader Error	101230
11	Exit	-
12	JMP	001000
13	6	000006
14	Data Transfer In	102130
15	Sense Character Ready	101130
16	14	000014
17	Sense Card Image	101030
20	15	000015
21	JMP	001000
	0	000000

*Assumes device address 030.

1.3.1 Initialize and Feed One Card

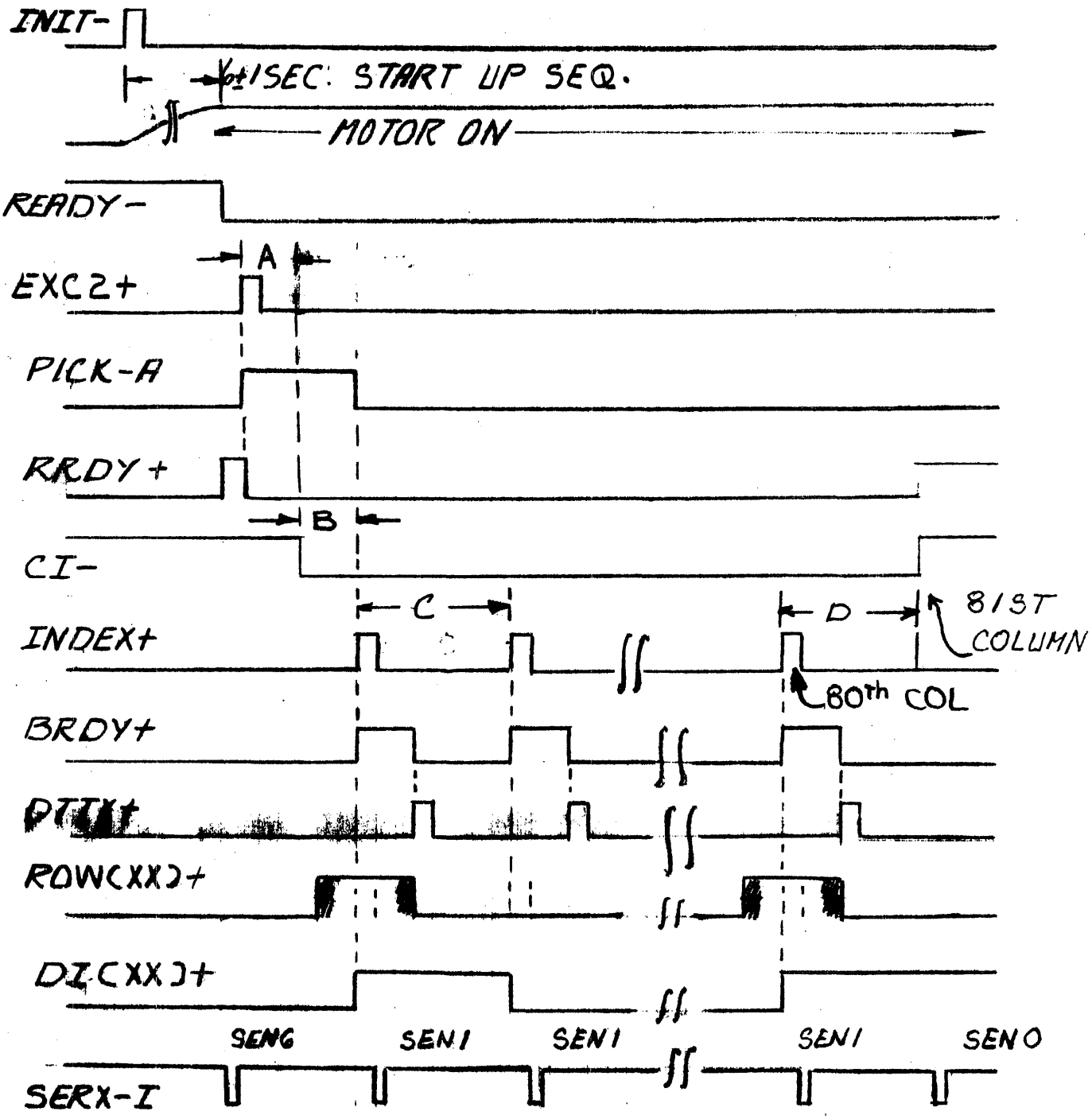
The initialize command (INIT+) resets the controller logic and the reader (CLEARA-). It will also turn on the reader motor if the motor is not already on. If the reader is in a Ready State, the program will feed one card as follows: An EXC 2 is program generated. The logic develops and presents the feed pulse PICK-A to the reader connector. EXC 2 also disables the sense logic during the time the card is being fed into the read station. The first character ready strobe (INDEX+) then sets the character ready flip flop (BRDY) which, in turn, resets the read a card flip flop, PICK+.

1.3.2 Read the Data in Sense Mode

As the card passes into the read station, the leading edge detector is covered which causes the card image (CI) line to go to a logic zero. As the first column of data appears over the read station, a data strobe (INDEX-) is sent by the reader, coincident with the data, which sets the character ready flip flop (BRDY)

The data strobe also strobes data (ROWXX) into the data register (DIXX).

FIGURE 1.2 DATA TRANSFER TIMING.



MODEL	A(MSEC	B(USEC)	C(USEC)	D(USEC)	CARD PICK CYCLE
620-28	24	6250	2014	2014	200
E2747	24	2600	870	870	100
E2382	15	1860	478	478	60
E2993	24	6250	2014	2014	200

The program senses the character ready condition and performs a "Data Transfer In". Flip flop DTIX is set by the FRYX pulse. DTIX is then used to strobe data onto the E-Bus and reset BRDY. All 80 columns are sequentially read in this way:

As the card completes its pass over the read station, the trailing edge of the card uncovers the trailing edge detector and returns CI- to a logic high. The program senses this condition and branches out of the data transfer loop. A ready interrupt is also generated at this time.

1.3.3 Read The Data in BIC Mode

Once the BIC has been initialized, EXC 2 (read one card) sets the controller connected for BIC flip flop CDCX. When data is ready (BRDY) TRQX-B goes to a logic zero which initiates a transfer request. TAKX-B transfer acknowledge is returned to the controller. This term arms flip flop DTIX which is then set by the function ready pulse FRYX. Data is then strobed onto the E-Bus and another BIC transfer is initiated by the next strobe from the reader which sets BRDY. BIC operation may be terminated by counting the 80 columns of data and ending the transfer at the end of the 80th column.

1.4 SYSTEM GENERAL SPECIFICATIONS

1.4.1 Controller

Characteristic	Specification
Organization	Consists of timing and control select and de-select logic, driver, and receivers.
Control Capability	Reads 80 column punched card with no information content restrictions at up to 300 cards per minute. The controller reads 12 bits at a time and transfers the word to the CPU.
Output Capability	Three external control commands, five input commands, five sense conditions, three interrupts, BIC capability.
Logic Levels	Negative Logic: 0.0V to +0.5V = true +2.5V to +5V = false Positive Logic: +2.5V to 5V = true 0.0V to +0.5V = false
DC Power	+5VDC @ .5 amps

Characteristic	Specification
I/O and B Cables	Negative Logic
Internal	Positive Logic
Reader Cable	Negative Logic

1.4.2 Reader General Specifications, Model M200

Machine Characteristics

Media Processed

Standard 80-Column Cards as defined by ANSI X3.11 - 1969

Operating Rates:

300 cards per minute ±10%

Card Capacity

Input Hopper	550 Cards
Output Stacker	550 Cards

Feeding

Asynchronous, via a vacuum picker in conjunction with "riffled" air

Reading: Infrared light emitting diodes

Card Read Time:

80-Column 200 msec

General Specifications

Dimensions

Overall Dimensions
Height - 11 in.
Depth - 14 in.
Width - 19-1/4 in.

Weight

Complete Unit
Less than 60 lbs.

Temperature

Operating	40° to 110°F
Non-Operating	25° to 135°F

Input Power

Voltage	115V - 60HZ, 115V - 50HZ 220V - 50HZ
Frequency	Single Phase
Current	Less than 5 AMPS
Power	Less than 300 WATTS

TABLE 1.1 - CONTROLLER MNEMONICS

MNEMONIC	DESCRIPTION
BCDX-B	BIC Disconnect
BRDY+	Character Ready Flip Flop
CDCX+	Controller connected for BIC flip flop
CI-	Card image level from reader reset
CLEARA-	Reset line to reader. Also turns on reader motor.
COD(X)+	E-Bus decodes
CRDYI-	Character Ready Interrupt
DA3X+	Device Address Decode
DCEX-B	BIC Device Connect
DESX-B	BIC Device Stop
DI(XX)+	Data Register Outputs
DRYX-I	CPU Data Ready Pulse
DTIX+	Data Transfer In Flip Flop
EB(XX)-I	CPU E-Bus Bits 0 thru 15
ERRORI-	Card Reader Error Interrupt
EXC2-	External Control Decode to "Feed a Card" and Clock "On" CDCX (BIC) flip flop
EXC3-	External control decode to set continuous feed flip flop
FRYX-I	CPU function ready flip flop
INDEX+	Data strobe from reader
IHE-	Hopper empty level from reader

TABLE 1.1 (con't)

MNEMONIC	DESCRIPTION
INIT+	Initialize Pulse
IPF-	Machine alert from reader (i.e., power off)
ITR-	Reader Error Alert from reader (i.e., photocell failure)
PICK-	Feed a card flip flop output
PICK-A	Feed a card pulse or level in continuous mode
READY I-	Card reader ready or end of card image interrupt
READY-	Level from reader indicating reader conditioned to accept card feed pulse
SERX-I	Sense line to CPU
SYRT-I	CPU Console System Reset
TAKX- I	BIC Transfer Acknowledge
TROB+	OR'D Reader Alerts
TRQX-B	BIC Transfer Request

SECTION 2
PROGRAMMING

2.1 GENERAL

The card reader may be programmed in a multi-peripheral invironment by the external interrupt structure or by programmed response loops. EXC instructions control the operations, and data transfers are performed by means of the BIC option, or by program "data transfer in" sequences.

2.2 DESCRIPTION OF COMMANDS

There are a total of 13 instructions reserved for use by the card reader controller. These include three external control functions, five sense, five data transfer in commands. These reserved instructions are listed and described in the paragraphs that follow. It is assumed here that the card reader controller has been assigned device address 030.

2.3 INSTRUCTION SET SUMMARY (DA=30)

2.3.1 External Control

EXC 030	Initialize controller and reader and turn on reader motor
EXC 0230	Read one card (also connects BIC in BIC mode)
EXC 0330	Feed cards continuously (reset by initialize command or system reset)

2.3.2 Data Transfer

IME 030	Transfer 12 bit word to memory
INA 030	Transfer 12 bit word to A register
INB 030	Transfer 12 bit word to B register
CIA 030	Transfer 12 bit word to A register, cleared
CIB 030	Transfer 12 bit word to B register, cleared

2.3.3 Sense

SEN 030	Sense Card in reader station (card image)
SEN 0130	Sense character ready
SEN 0230	Sense reader error
SEN 0330	Sense hopper empty
SEN 0630	Sense reader ready

2.3.4 Interrupts

Three interrupts are available: Character Ready, Error, and Reader Ready (End of Card).

2.3.4.1 Character Ready Interrupt

Character ready generates an interrupt when a character is in the input buffer and ready to be inputted to the CPU. This character must be taken within a maximum of 2.014 milliseconds after the interrupt is generated.

2.3.4.2 Error Interrupt

Error interrupt is generated for the following conditions:

1. Failure of the light or dark check (read error). Requires operator intervention.

2. Motion check (pick or stack check) requires operator intervention. This error signal will occur within 300 milliseconds of the initiation of an unsuccessful pick attempt or in time to inhibit the picking of the second card after the stacker sensor detects that a card is not completely clear of the card track.

Both error conditions are displayed on the front panel indicator and may be reset by the reset button on the reader, by CPU system reset, or the initialize command.

2.3.4.3 Ready Interrupt

A ready interrupt is generated under the following conditions:

1. Power is applied and the 6 second run up is completed (motor up to speed).

2. Input hopper has been loaded and run up completed.

3. Card reader cleared of error conditions and is ready to accept a pick command from the external program.
4. The card has completed its pass through the read station (End of Card Image).

2.4 INSTRUCTION SET DESCRIPTION

2.4.1 EXC Commands

2.4.1.1 EXC Initialize (EXC 0)

Clears the controller and reader as follows:

1. Non-continuous mode
2. Character not ready
3. BIC disconnected
4. Reader logic reset to "RESET" condition
5. Reader motor "ON".

2.4.1.2 EXC Read One Card (EXC 2)

This command causes the controller to initiate a card read cycle and, if data transfer is under control of BIC, sets the BIC connect flip flop.

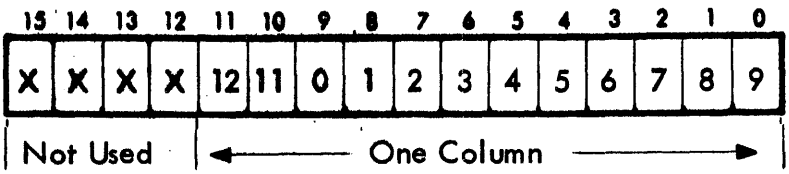
A single card is picked and transported to the read station. As each column passes through the read station, the strobe signal received from the reader sets the character ready sense, generates a character ready interrupt, and strobes a 12 bit data character into the input register. For pertinent timing information, refer to Section 2.3.2, "Data Transfer In" Commands.

2.4.1.3 EXC Continuous Feed (EXC 3)

This command holds the card feed line to the reader at a continuous feed level. Cards will be fed at a maximum rate of 300 CPM $\pm$ 10% until the EXC initialize command is generated or the CPU system reset is activated.

When continuous feed is to be stopped, an initialize command must be sent within 8 milliseconds after the receipt of the eightieth column of data of the previous card to prevent an extra card from being fed through the reader.

2.4.2 Input Transfer Commands (CIA, CIB, INA, INB, INM)



Card column VS E-Bus bit are as shown:

Pertinent timing relationships from initiation of card feed to end of card are categorized below: (300 CPM card reader only)

Card feed initiation to first character ready	=	30.3 milliseconds minimum
Character ready to next character ready	=	2.014 milliseconds minimum
1st column to 80th column	=	161.12 milliseconds minimum
Total card feed cycle (card image)	=	200 milliseconds minimum

Once a card feed cycle has been initiated, the CPU must perform a "data transfer in" operation within 32.2 milliseconds maximum for the first column and within 2.014 milliseconds maximum between columns or data will be lost. See Figure 1.2 for 600 CPM and 1000 CPM timing relationships).

2.4.3 Sense Commands

2.4.3.1 Sense End of Card (Card Image)

This sense answers in the affirmative when no card feed operation is in progress. As the card enters the read station, the leading edge detector is covered.. This causes the card image line to go low. As the card leaves the read station, the trailing edge detector is uncovered. This causes the card image line to go high. The program may sense this condition after the reading of data has been started to sense the end of card as an option to counting 80 columns of data to determine end of card.

2.4.3.2 Sense Character Ready

This sense answers in the affirmative when a column of data is present at the output of the buffer register and is ready for transfer to the computer. An input transfer should follow the leading edge of "Character Ready" within 2.014 milliseconds.

2.4.3.3 Sense Reader Ready

This sense answers in the affirmative when the previous card read cycle has been completed satisfactorily and the controller is ready to receive the next EXC "Read

One Card" command.

2.4.3.4 Sense Reader Error

This sense answers in the affirmative when an error condition has occurred during a previous or the present card read cycle. The "Reader Error" sense remains true until the error condition is corrected. The error conditions are: Light/Dark Check Error, Card Motion Error, Pick Failure, and Hopper Empty. When the controller is being operated in conjunction with a BIC, the error conditions are used to cause an "Abnormal Device Stop" thus, possibly resulting in the incomplete reading of a card. Pressing the RESET button on the reader, pressing CPU SYSTEM RESET, or doing an EXC initialize will reset the error line, if the error condition has been corrected.

2.4.3.5 Sense Hopper Empty

This sense answers in the affirmative when the reader input hopper contains no cards. This sense is provided to allow the distinction between a "normal" reader error and an "abnormal" reader error.

2.5 COMMAND SEQUENCES

The flow chart shown in Figure 2.1 is meant to aid programmers in determining the proper sequence of commands required to input a card of data in sense mode. Figure 2.2 is a typical BIC flow diagram.

The end of data is shown as being determined by counting columns. It is also possible to determine end of data by sensing the card image line (SEN 0). In the latter case, the column count blocks in the flow chart may be replaced by a SEN 0.

2.6 MOTOR CONTROL

Normally, the card reader motor is externally turned on by the "RESET" button on the card reader console, assuming the card reader power switch is in the "ON" position. The motor may, however, be turned on by issuing an initialize command (EXC 0). A minimum of 4 seconds start up time is required, after the initialize command, before the reader READY line becomes true and card feeding may be initialized.

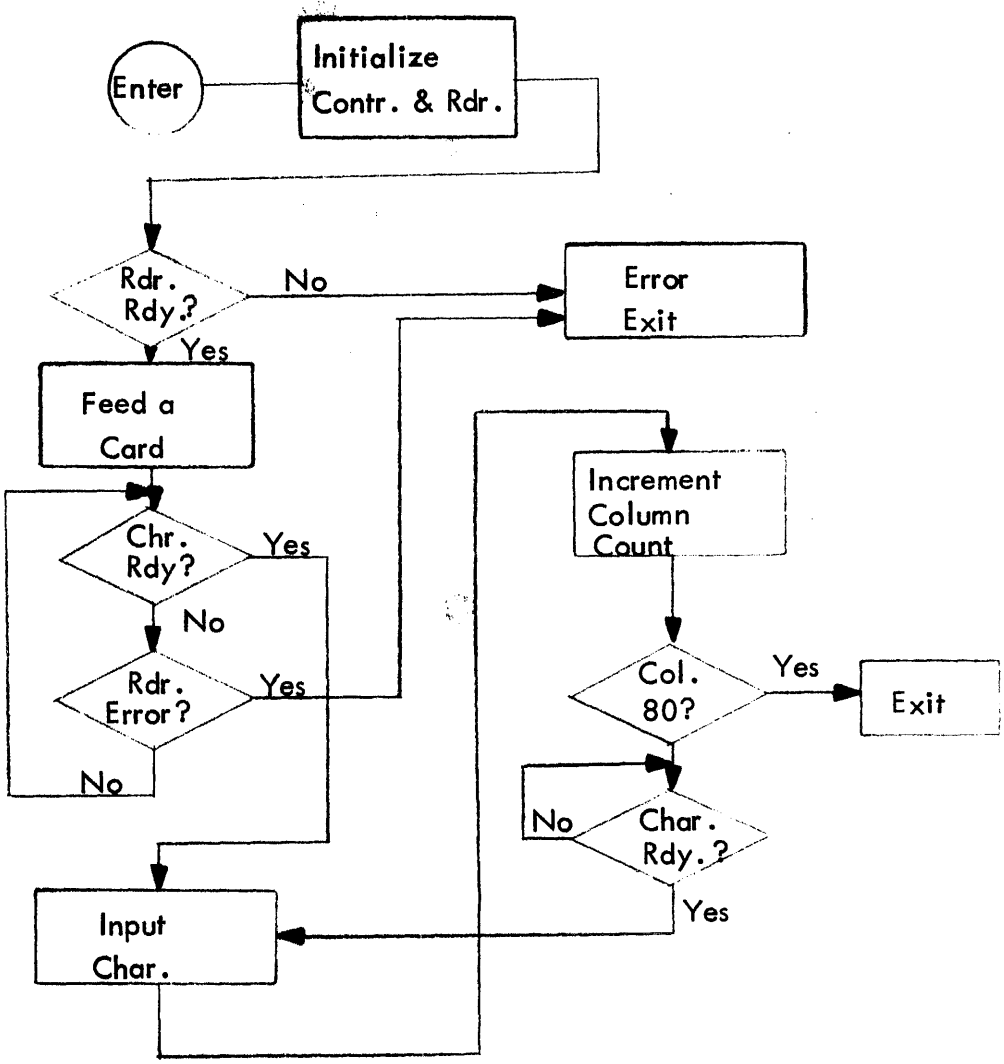


FIGURE 2.1 - COMMAND SEQUENCE FLOW CHART

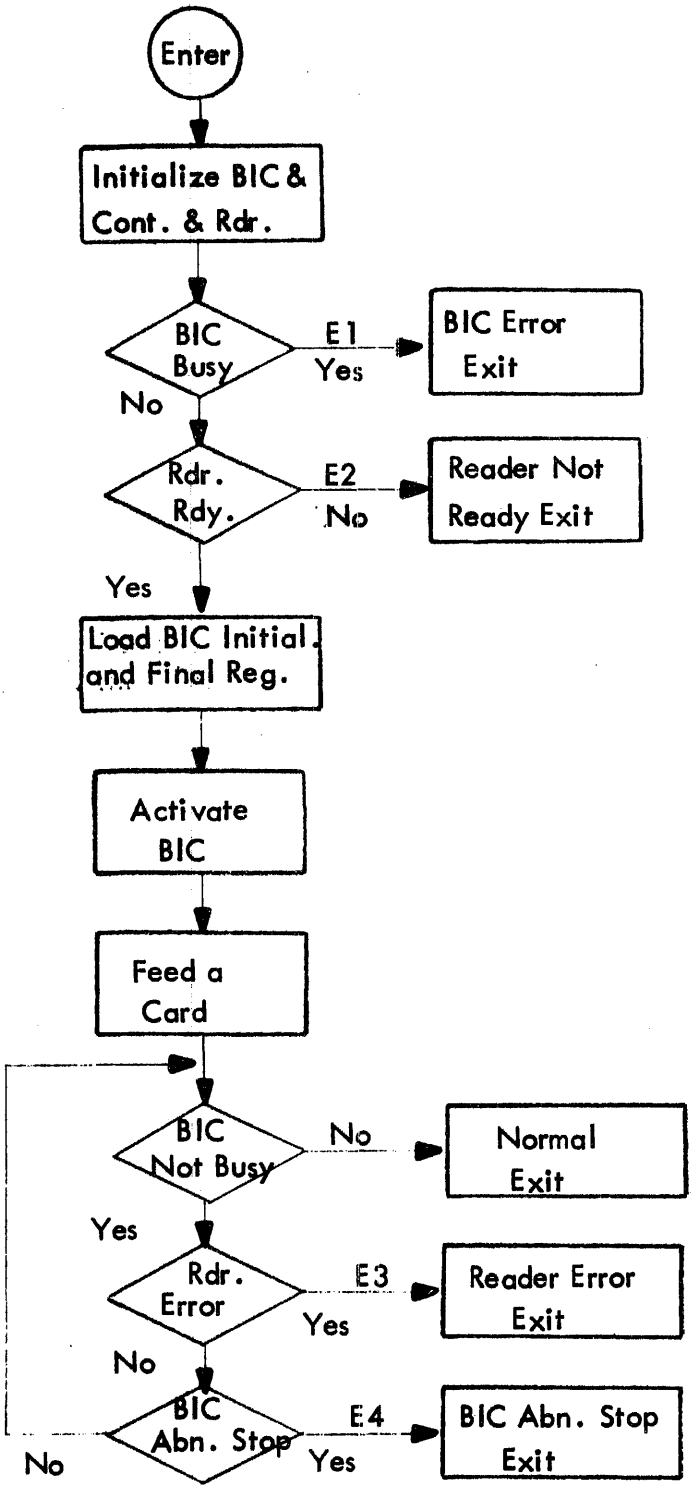


FIGURE 2.2 - TYPICAL BIC FLOW DIAGRAM

SECTION 3
INSTALLATION

3.1 GENERAL

Installation of the card reader system in the field is normally accomplished by Varian Data Machines Customer Service Engineers. Logic diagrams, assembly layout, and wiring information are provided at the time of purchase. The following installation data is provided for planning purposes.

3.2 PRE-INSTALLATION REQUIREMENTS

Prior to the installation of the system, proper operation of the computer should be assured through use of the diagnostic test routines described in the 620 Maintenance Manual. An Expansion/Peripheral Controller Chassis must be installed in close proximity to the computer. The chassis is connected to the I/O bus by means of the I/O cable which is attached to the Expansion Chassis. The termination shoe provided must be connected on the end of the I/O bus.

3.3 WIRING REQUIREMENTS

3.3.1 Controller Backplane Wiring

The controller card requires the space provided by three card slots. It uses the standard backplane I/O bus and power wiring used with the Expansion Chassis. (See Table 3.1).

3.3.2 Cabling

There is one cable connecting the controller card to the card reader. All lines are twisted pair lines. Pin assignments are shown in Table 3.2. A standard length 20 foot cable is supplied with the card reader option.

3.4 DEVICE ADDRESS SELECTION

The device address is normally wired for address 30_8. The available addresses are from 30_8 to 37_8. Connector pins (64, 65) (67, 68) and (70, 71) provide the true and complement outputs of the I/O bus address bits respectively. Pins 66, 69 and 72 are the input pins to the device address decoding gates. Table 3.3 lists wiring connections required for each of the available device addresses.

TABLE 3.1 - CONTROLLER CARD, P1 PIN ASSIGNMENTS

PIN	MNEMONIC	PIN	MNEMONIC
1	GND	50	BCDX-B
2	EB00-I	52	BCDX-B
4	EB01-I	54	CDCX-B
6	EB02-I	56	DCEX-B
8	EB03-I	58	TAKX-B
10	EB04-I	60	DESX-B
11	EB05-I	64	EB00+
12	EB06-I	65	EB00-
13	EB07-I	66	EB01+
14	EB08-I	67	EB01+
15	EB09-I	68	EB01-
16	EB10-I	69	EB11+
17	EB11-I	70	EB02+
18	EB12-I	71	EB02-
19	EB13-I	72	EB21+
20	EB14-I	75	CRDYI-
27	FRYX-I	77	ERRORI-
29	DRYX-I	79	READYI-
31	SERX-I	100	GND
43	SYRT-I	118	+5V
44	IUAX-I	121	+5V
48	GND	122	GND
49	TRQX-B		

TABLE 3.2 - J2PIN ASSIGNMENTS

PIN	MNEMONIC	DESCRIPTION	SOURCE
1	ROW09-		
2	R		
3	ROW08-		
4	R		
5	ROW07-		
6	R		
7	ROW06-		
8	R		
9	ROW05-		
10	R	Data	Device
11	ROW04-		
12	R		
13	ROW03-		
14	R		
15	ROW02-		
16	R		
17	ROW01-		
18	R		
19	ROW00-		
20	R		
21	ROW11-		
22	R		
23	ROW12-		
24	R		
25	CLEARA-	Initialize	User
26	R	(Motor Start)	
27	PICK-A	Feed	User
28	R		
29	ITR-	Read Alert	Device
30	R		
31	IPF-	Machine Alert	Device
32	R		
33	IHE-	Input Hopper Empty	Device
34	R		
35	READY-	Reader Ready	Device
36	R		
37	CI-	Card Image	Device
38	R		
39	INDEX-	Data Strobe	Device
40	R		
41	SPARE		
42	R		
43	SPARE		
44	R		

TABLE 3.3 - DEVICE ADDRESS WIRING LIST

Device Address	Jumper Pins	Device Address	Jumper Pins
30	65 to 66 68 to 69 71 to 72	34	65 to 66 68 to 69 70 to 72
31	64 to 66 68 to 69 71 to 72	35	64 to 66 68 to 69 70 to 72
32	65 to 66 67 to 69 71 to 72	36	65 to 66 67 to 69 70 to 72
33	64 to 68 67 to 69 71 to 72	37	64 to 66 67 to 69 70 to 72

3.5 CARD READER INSTALLATION AND OPERATION

3.5.1 General

A complete description and instructions in operation of the card reader will be found in the Card Reader Maintenance Manual that is delivered with the system.

SECTION 4
MAINTENANCE

4.1 GENERAL

This section defines the appropriate equipment, diagnostic routines, and required tests to insure the card reader controller's proper performance. Maintenance requirements for the card reader are called out in the card reader instruction manual, section 3.

4.2 MAINTENANCE OF THE CONTROLLER

The following are standard hardware and software devices used for checkout. Addition and/or deletion of these devices may be made in the future, if necessary.

4.2.1 Test Equipment

The Tektronix 545 Oscilloscope or one of similar performance specifications is required.

4.2.2 Tools

A standard extender board allows for easy access to the card reader controller board during the test.

4.2.3 Software (Diagnostic)

The following tests on paper tapes are recommended for diagnosis and troubleshooting of the card reader controllers:

a. Maintain II 92A0107-001
b. Test Program 92A0107-012
c. Software Performance Specification 89A0180

4.3 MAINTENANCE OF THE CARD READER

Maintenance procedures are simple, straight-forward, and easy to perform. They are completely defined in the card reader instruction manual.

ADDENDUM #1

E-2747, 600 Card Per Minute Card Reader

General Specifications

Card Rate	600 card per minute	
Card Type	Standard 80-column card	
Hopper/Stacker	1000 card capacity	
Light Source	M-infrared light emitting diodes OM-Fiber Optics, 13 channel	
Read Station	M-photo transistor, 12 bits simultaneously OM-photo transistors, 12 data rows and one clock row.	
Electronics	7400 series TTL integrated circuit logic	
Internal Clock	M-Crystal Oscillator	
Power	1600 VA Starting load, 600 VA Running load	
Height	16-1/4 in.	41.2 cm
Width	23-1/16 in.	58.6 cm
Depth	18 in.	45.7 cm
Weight	77 lbs.	
Shipping	88 lbs.	

For card feed and data timing relationships, see Figure 1-2.

ADDENDUM #2

E2382, 1000 CPM Card Reader

General Specifications

Card Rate	1000 cards per minute	
Card Type	Standard 80-column card	
Hopper/Stacker	1000 card capacity	
Light Source	M-infrared light emitting diodes OM-Fiber Optics, 13 channel	
Read Station	M-photo transistor, 12 bits simultaneously OM-photo transistors, 12 data rows and one clock row	
Electronics	7400 series TTL integrated circuit logic	
Internal Clock	M-Crystal Oscillator	
Power	1600 VA Starting load, 600 VA Running load	
Height	16-1/4 in.	41.2 cm
Width	23-1/16 in.	58.6 cm
Depth	18 in.	45.7 cm
Weight	83 lbs.	
Shipping	94 lbs.	

For card feed and data timing relationships, see Figure 1-2.

ADDENDUM #3

E2993, 300 CPM Mark-Sense Card Reader

General Specifications

Please refer to paragraph 1.4.2 for the 300 CPM card reader general specifications and to Figure 1-2 for timing relationships.

Card and data specifications are as follows:

Mark Sense Data - A mark must be a vertical line using a #2 pencil or equivalent marking material.

The minimum dimensions are: width, .015", length, .125" centered within data row area.

The maximum dimensions are: width, from trailing edge of previous clock mark to leading edge of next clock mark; length, .240" centered within data row area.

The mark must have an average reflectance that is less than or equal to 28% of the reflectance of that portion of the card immediately adjacent to the mark. Single stroke marks with a #2 pencil will meet this specification.

An erasure must have an average reflectance that is greater than or equal to 75% of the reflectance of the portion of the card immediately adjacent to the erasure.

Card Design - Because the Mark Sense cards image field is determined and tailored by the customer to meet a particular application, the following is presented to aid in the design of a Mark Sense Data Card.

The shaded portions of Figure A3-1 show the areas in which data and clock marks can be placed.

Data columns are constructed by a clock mark immediately preceding the data column, the data column area, and then another clock mark. Figure A3-2 shows a typical data column and the read area for each data row.

Any pencil mark or punched hole meeting the data specification and lying in the shaded area between the clock marks may be read as data.

Any black column or rwo number which is commonly found on standard 80 column punched cards may also be read as data.

A marking constraint with mark identifier is normally used to place and identify a data mark in the data field. Figure A3.3 depicts a data mark in the data field. Figure A3.3 depicts a typical marking constraint. To indicate a list, a vertical pencil mark would be placed within the constraint.

An example of a general purpose, 40 column Mark Sense Card is shown in Figure 3-4.

Punched Cards

80 column punched cards may also be read with the E2993 Mark/Sense Reader. The cards must, however, be free of reflective marks in the data fields. Green or red markings on the card typically are not reflective. The punched cards must also have a clock row on the bottom as on the Mark/Sense Card (see Figure A3-1).

Mixing Cards

Since both punched and Mark/Sense Cards must have a clock row, both can be used inter-changeably providing the two card types are designed properly.

Test Program

Only 80 column cards can be used with the 620-28 (E2993) test program.

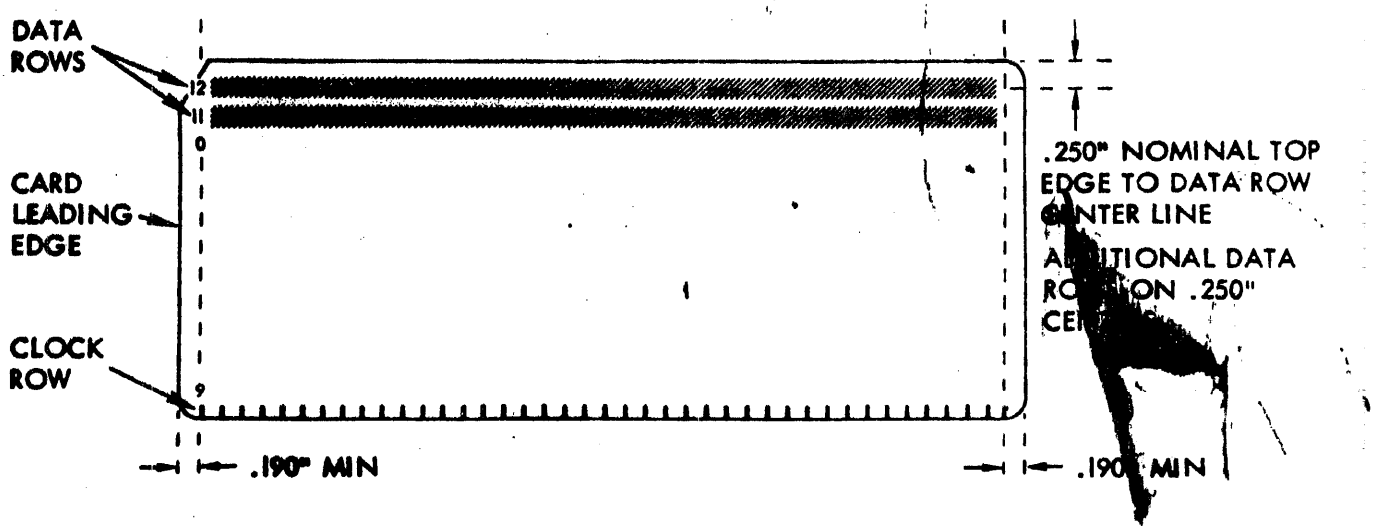


Figure A3-1 – Marking Areas

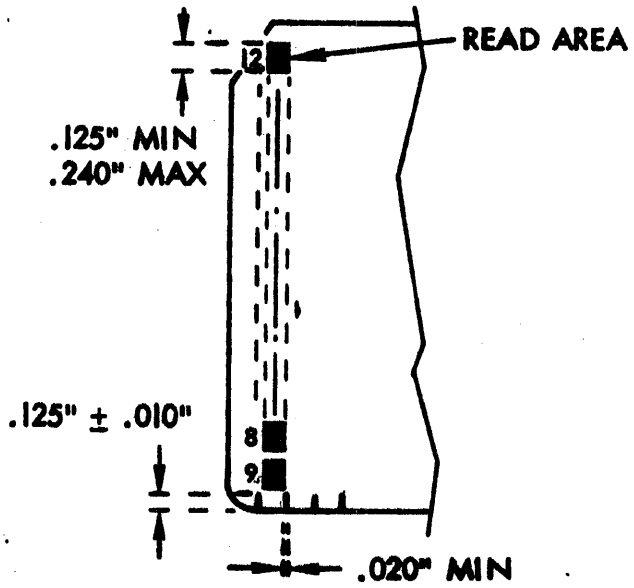


Figure A3-2 – Data Column

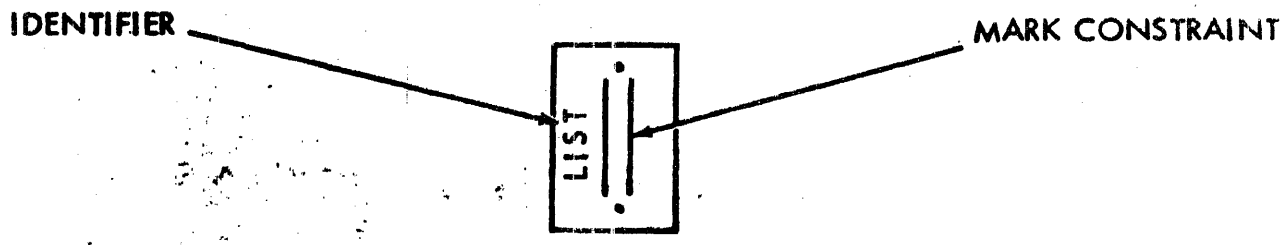


Figure A3-3 - Mark Constraint

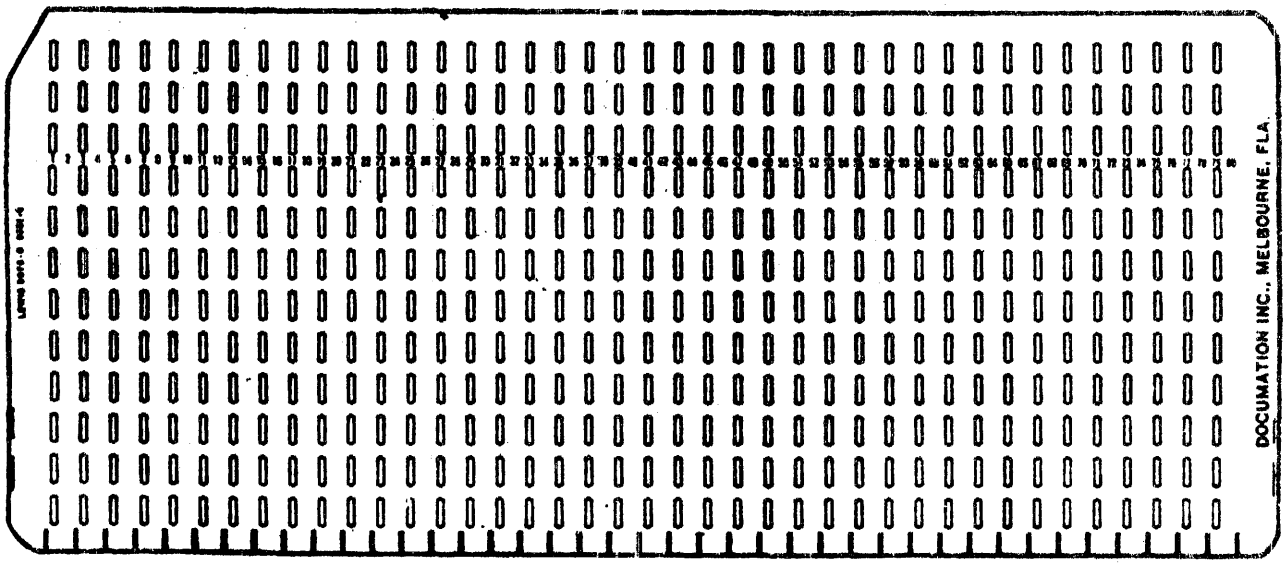


Figure A3-4 - Mark Sense Card

NOTES: (UNLESS OTHERWISE SPECIFIED)

REVISIONS					
CHNG. CODE	SYM	EN NO	DESCRIPTION	APPROVED	DATE
-	A		PRODUCTION RELEASE PER EN 82171	[illegible]	7/14/75
-	B	82311	REVISED SHTS 2, 3, & 5 PER EN 82311	W. Brown	2/19/74
-	C	82682	REVISED SHTS 5 & 7 PER EN 82682	W. Brown	7/31/74

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
J2	J1
C21	
P1	

REFERENCE DRAWINGS	
95W0998	WIRE LIST
44P0684	BOARD ASSY P/L
44D0684	BOARD ASSY
40D0175	BOARD DETAIL

DR		
CHK W.P. Brown	7/6/73	
DSGN		
ENGR [illegible]	7/6/73	
APPD [illegible]	7/6/73	
APPD		

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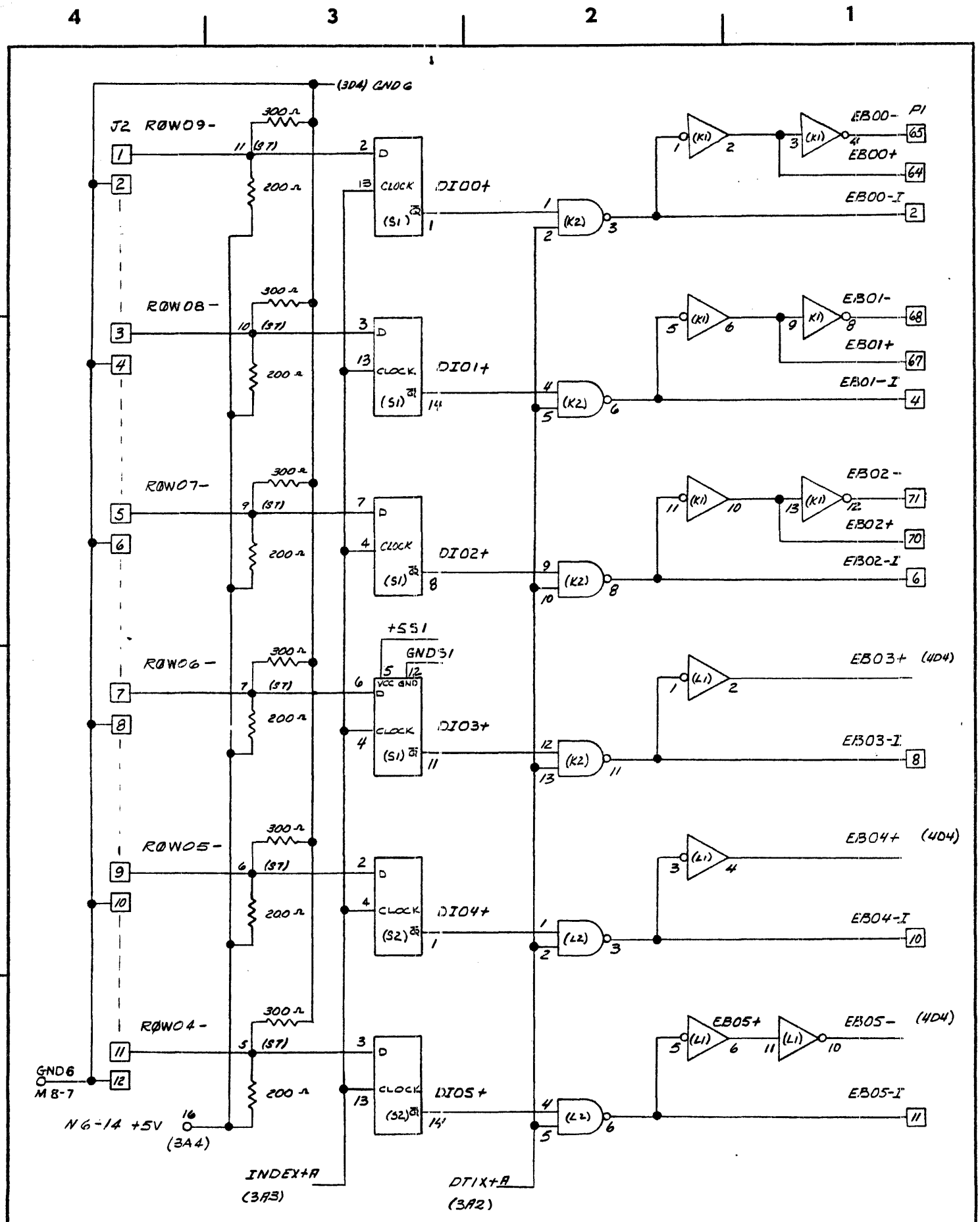
TITLE
LOGIC DIAGRAM
CARD READER CONTROLLER
MODEL 620-28

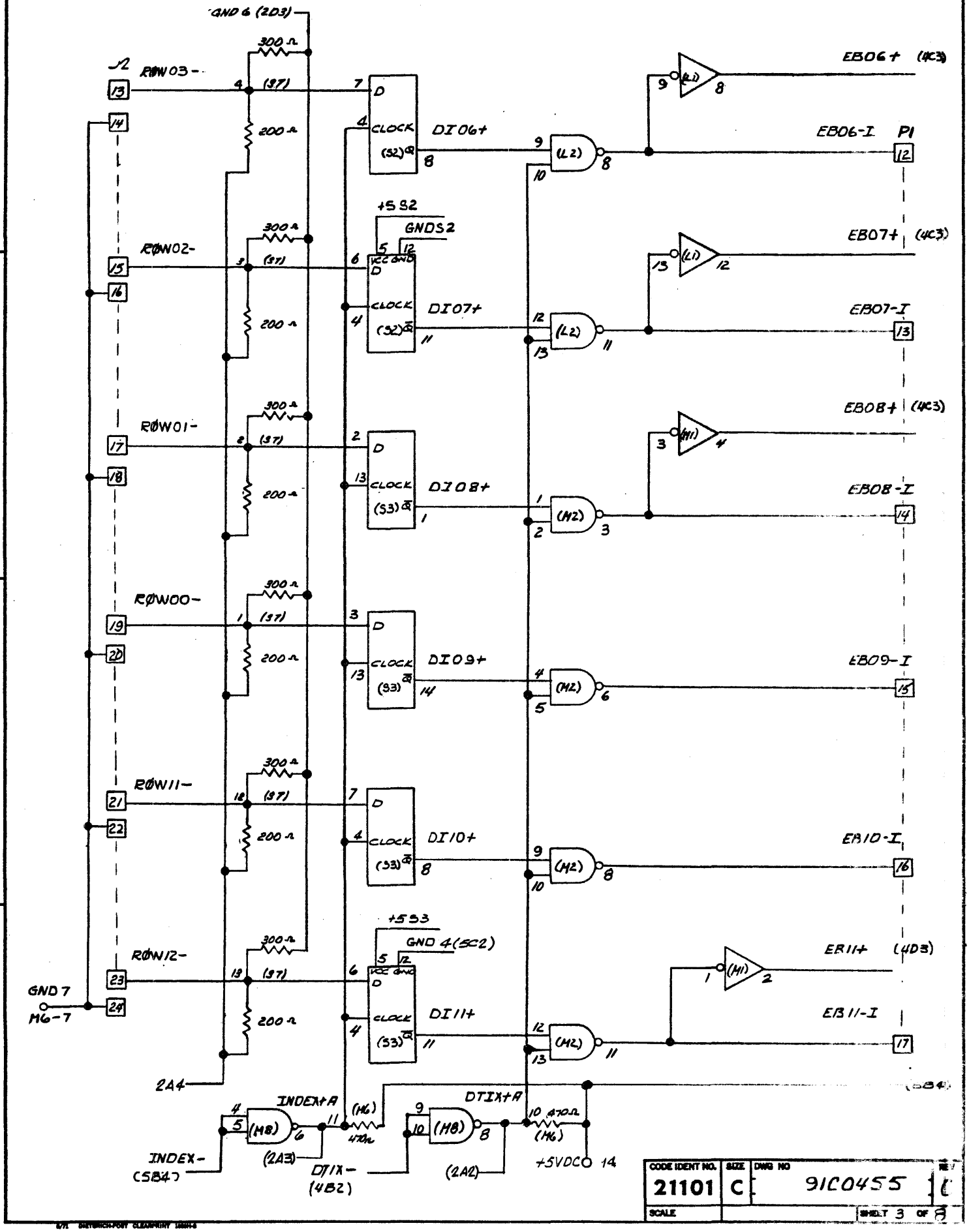
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0455	C

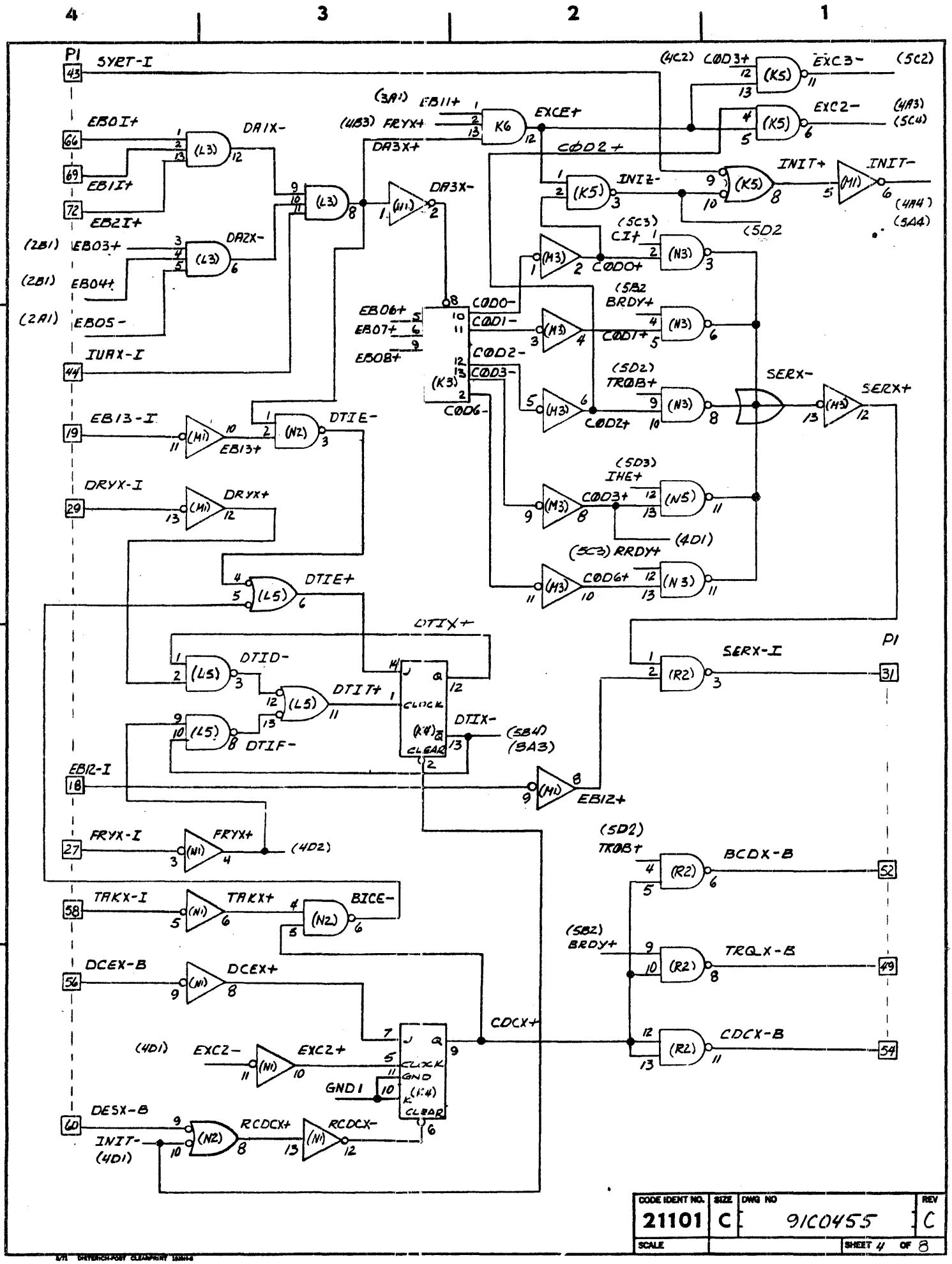
SCALE | SHEET 1 OF 8

1/70 DIETERICH-POST CLEARPRINT 3000H-6

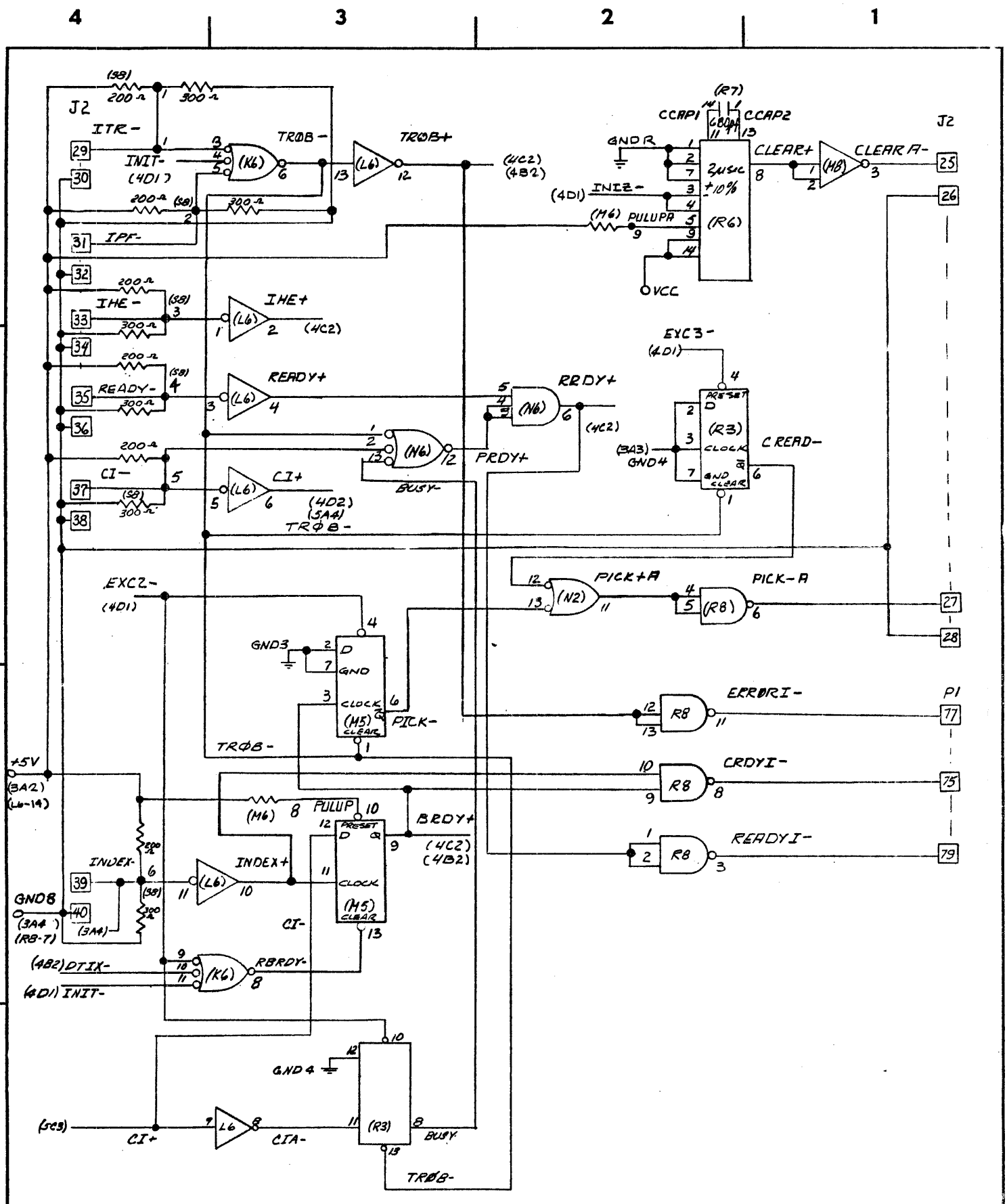


CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9IC0455	C
SCALE		SHEET 2 OF 8	


4
3
2
1
D
C
B
A
GND 6 (2D3)
300 Ω
200 Ω
J2
ROW03-
ROW02-
ROW01-
ROW00-
ROW11-
ROW12-
GND 7
M6-7
2A4
(97)
D
CLOCK
(S2)
(S3)
DI06+
DI07+
DI08+
DI09+
DI10+
DI11+
+5S2
GNDS2
+5S3
GND 4 (SC2)
VCC GND
(L2)
(L1)
(M2)
(M1)
EB06+ (4C3)
EB06-I P1
EB07+ (4C3)
EB07-I
EB08+ (4C3)
EB08-I
EB09-I
EB10-I
ER11+ (4D3)
EB11-I
INDEX+A
INDEX-
(5B4)
(M8)
(2A3)
DTIX-
(4B2)
DTIX+A
(2A2)
470Ω
(M6)
+5VDC
CODE IDENT NO. 21101
SIZE C
DWG NO 9IC0455
SCALE
SHEET 3 OF 8



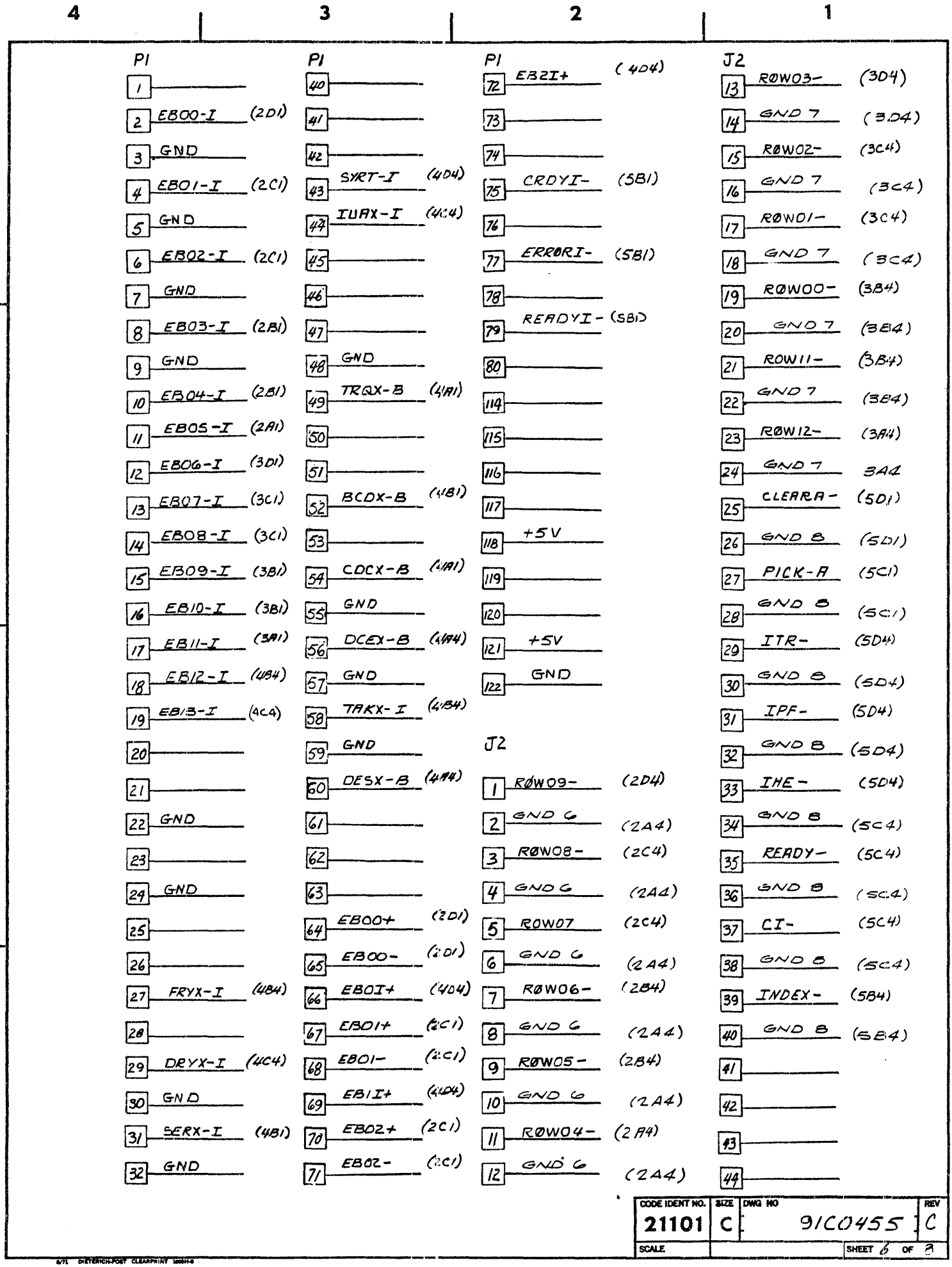
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9IC0455	C
SCALE		SHEET 4 OF 8	



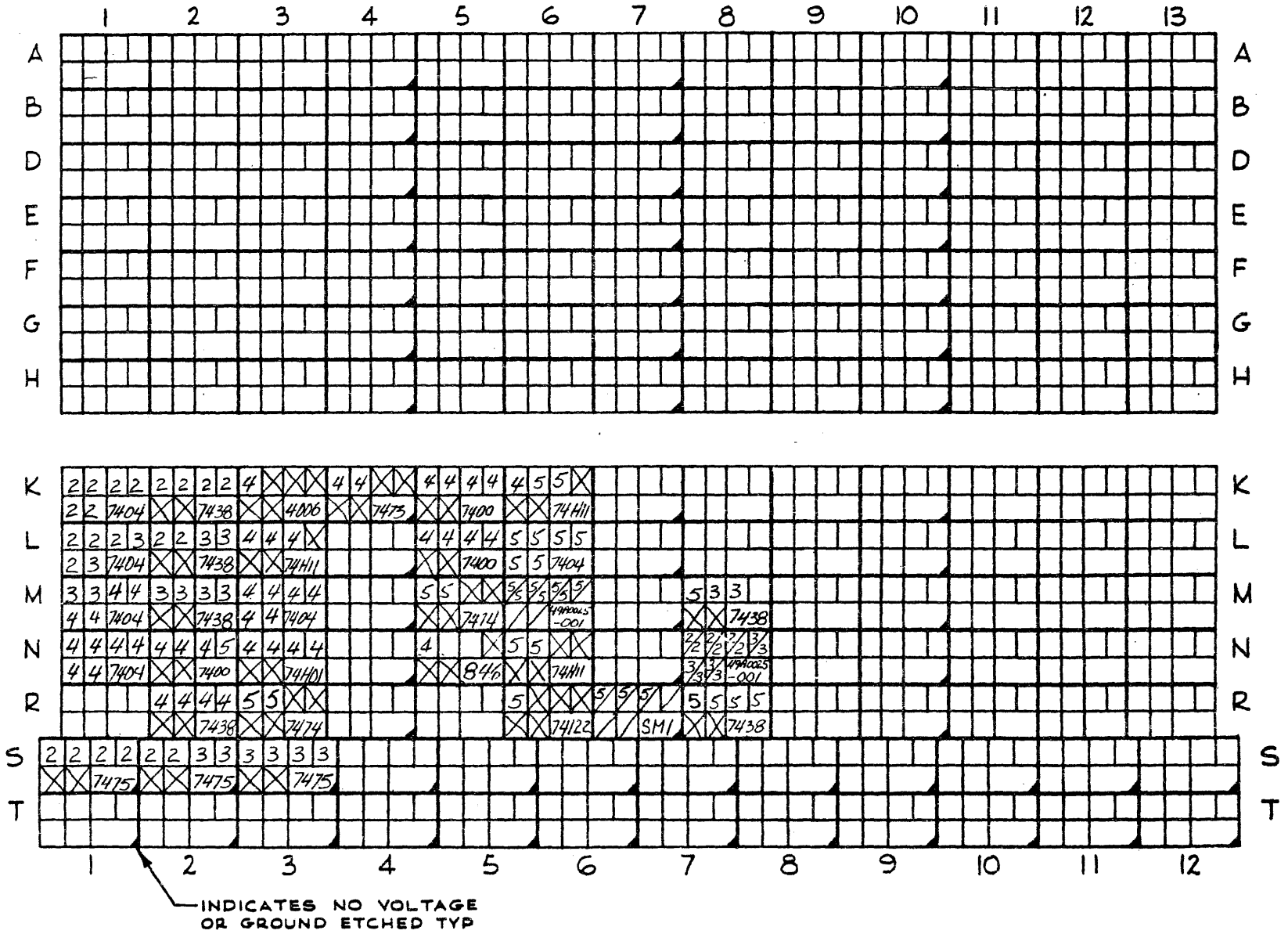
NOTE UNLESS ØTHERWISE SPECIFIED ALL RESISTORS ARE 470 ØHMS

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0455	C
SCALE		SHEET 5 OF 8	

8/71 DIETZGEN-POST CLEARPRINT


4
3
2
1
D
C
B
A
P1
1
2 EB00-I (2D1)
3 GND
4 EB01-I (2C1)
5 GND
6 EB02-I (2C1)
7 GND
8 EB03-I (2B1)
9 GND
10 EB04-I (2B1)
11 EB05-I (2A1)
12 EB06-I (3D1)
13 EB07-I (3C1)
14 EB08-I (3C1)
15 EB09-I (3B1)
16 EB10-I (3B1)
17 EB11-I (3A1)
18 EB12-I (4B4)
19 EB13-I (4C4)
20
21
22 GND
23
24 GND
25
26
27 FRYX-I (4B4)
28
29 DRYX-I (4C4)
30 GND
31 SERX-I (4B1)
32 GND
P1
40
41
42
43 SYRT-I (4D4)
44 IUAX-I (4C4)
45
46
47
48 GND
49 TRQX-B (4A1)
50
51
52 BCDX-B (4B1)
53
54 CDCX-B (4A1)
55 GND
56 DCEX-B (4B4)
57 GND
58 TAKX-I (4B4)
59 GND
60 DESX-B (4A4)
61
62
63
64 EB00+ (2D1)
65 EB00- (2D1)
66 EB01+ (4D4)
67 EB01+ (2C1)
68 EB01- (2C1)
69 EB1I+ (4D4)
70 EB02+ (2C1)
71 EB02- (2C1)
P1
72 EB2I+ (4D4)
73
74
75 CRDYI- (5B1)
76
77 ERRORI- (5B1)
78
79 READYI- (5B1)
80
114
115
116
117
118 +5V
119
120
121 +5V
122 GND
J2
1 ROW09- (2D4)
2 GND 6 (2A4)
3 ROW08- (2C4)
4 GND 6 (2A4)
5 ROW07 (2C4)
6 GND 6 (2A4)
7 ROW06- (2B4)
8 GND 6 (2A4)
9 ROW05- (2B4)
10 GND 6 (2A4)
11 ROW04- (2A4)
12 GND 6 (2A4)
J2
13 ROW03- (3D4)
14 GND 7 (3D4)
15 ROW02- (3C4)
16 GND 7 (3C4)
17 ROW01- (3C4)
18 GND 7 (3C4)
19 ROW00- (3B4)
20 GND 7 (3B4)
21 ROW11- (3B4)
22 GND 7 (3B4)
23 ROW12- (3A4)
24 GND 7 3A4
25 CLEARA- (5D1)
26 GND 8 (5D1)
27 PICK-A (5C1)
28 GND 8 (5C1)
29 ITR- (5D4)
30 GND 8 (5D4)
31 IPF- (5D4)
32 GND 8 (5D4)
33 IHE- (5D4)
34 GND 8 (5C4)
35 READY- (5C4)
36 GND 8 (5C4)
37 CI- (5C4)
38 GND 8 (5C4)
39 INDEX- (5B4)
40 GND 8 (5B4)
41
42
43
44
CODE IDENT NO. 21101
SIZE C
DWG NO 91C0455
REV C
SCALE
SHEET 6 OF 8

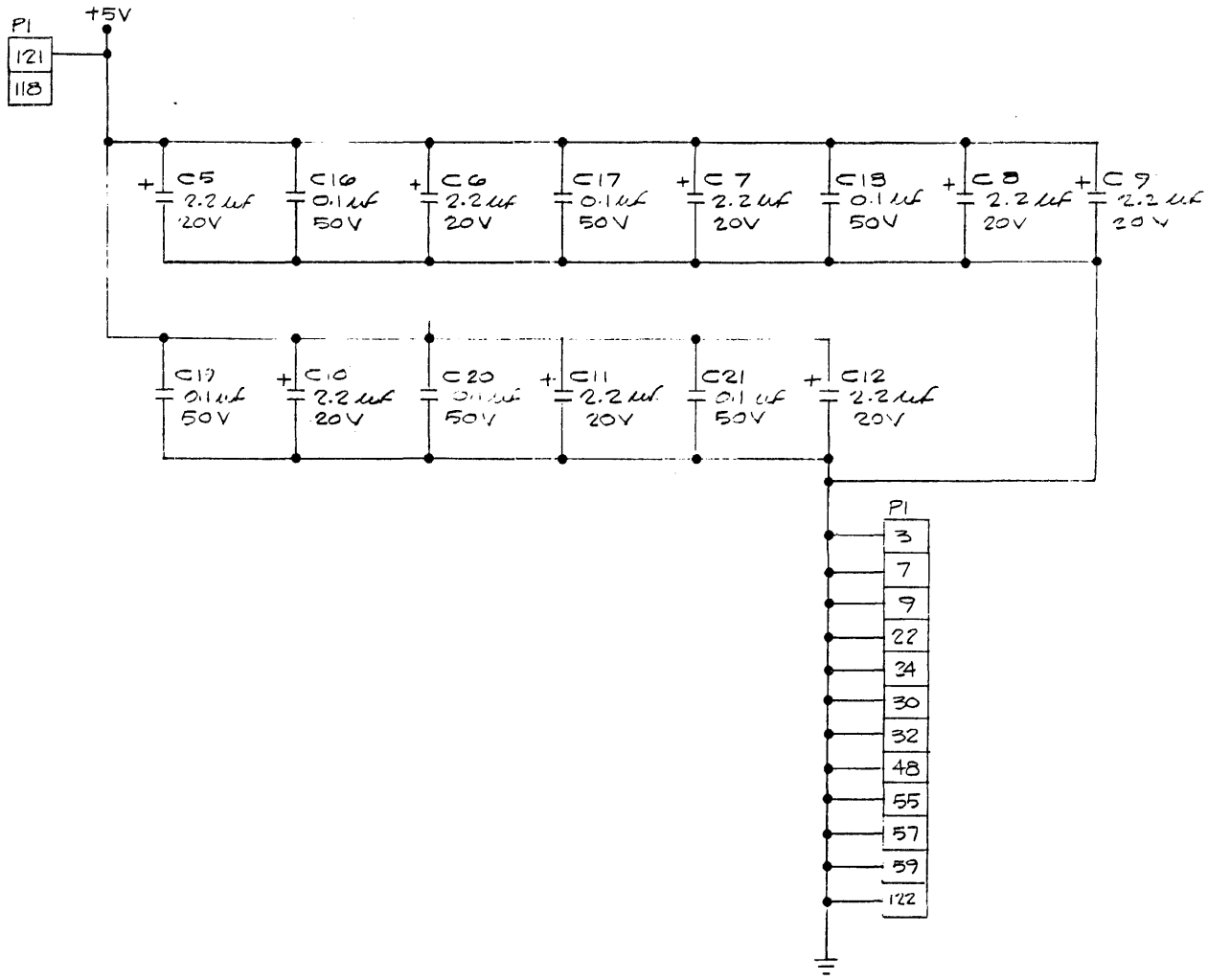
COMPONENT MAP



CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0455	C

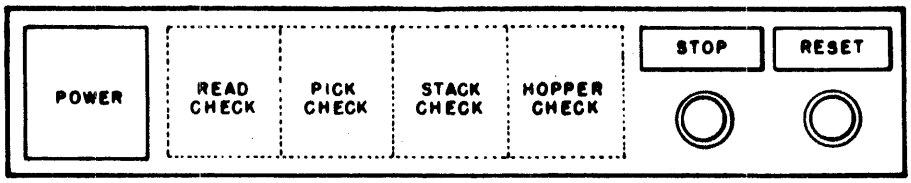
SCALE

SHEET 7 OF

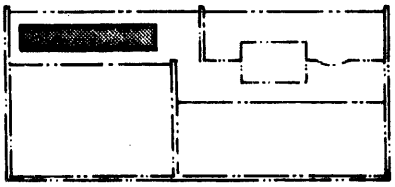


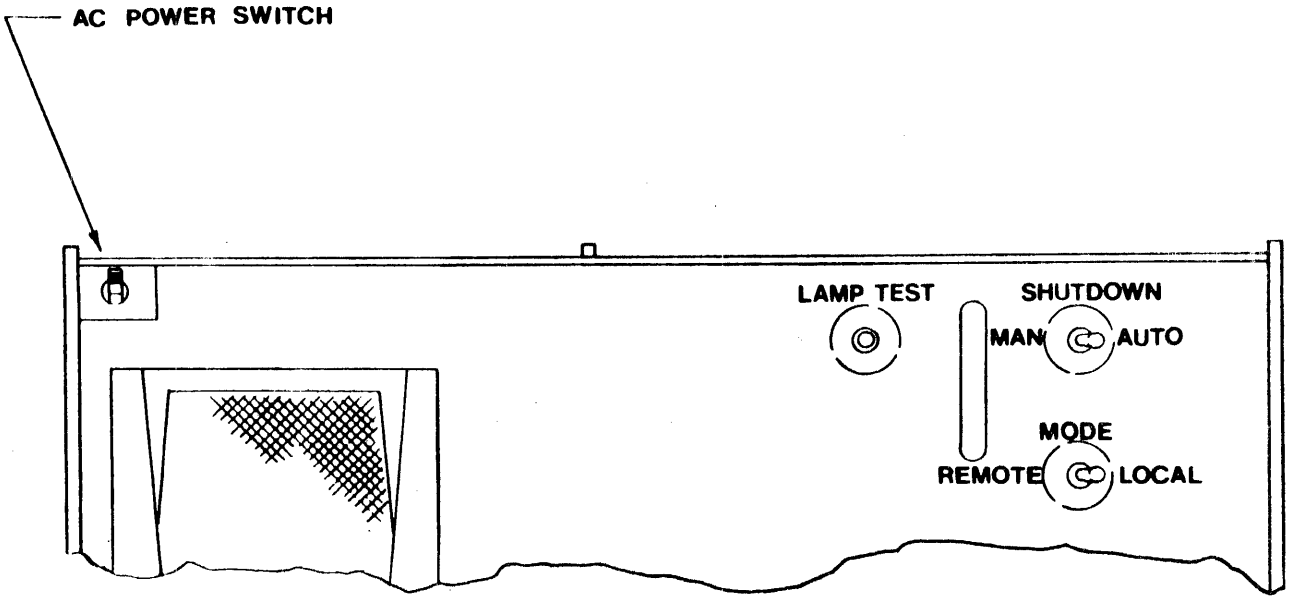
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	7100455	C
SCALE		SHEET 3 OF 3	

6/71 DIETERICH-POST CLEARPRINT 1000H-8



FRONT CONTROL PANEL





REAR PANEL

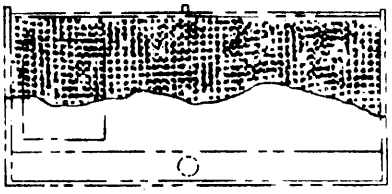


Figure 3. Switch Location

when the input hopper is empty. The motors will automatically restart when cards are placed in the hopper and the RESET switch is depressed. Expect a delay of approximately 3 seconds for the motors to run up.

OPERATIONAL FLOW CHART

Figure 4 shows a flow chart of the sequence of events which may be encountered in operating the reader. If trouble is experienced, refer to this check list before calling for maintenance.

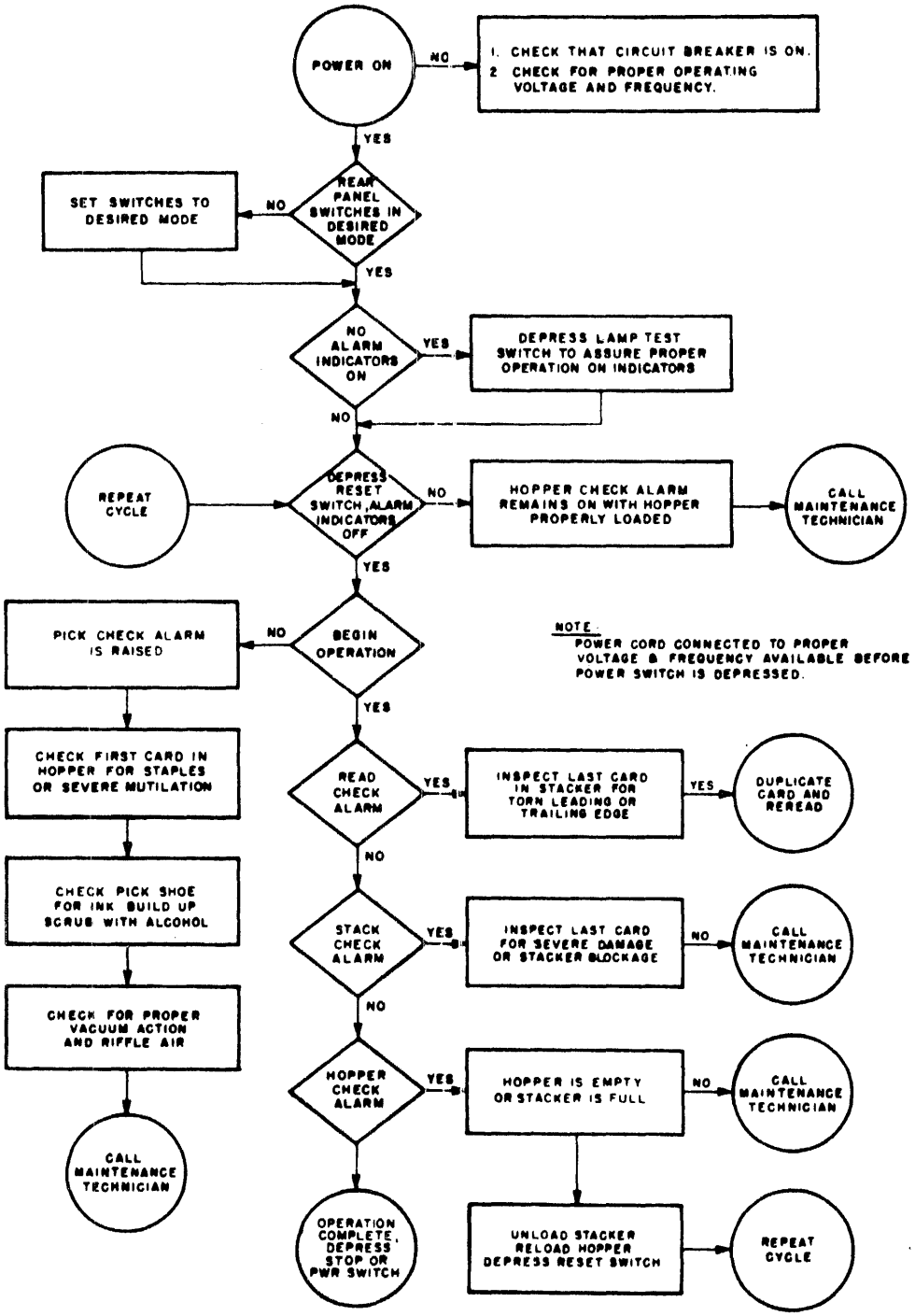


Figure 4. Operational Flow Chart

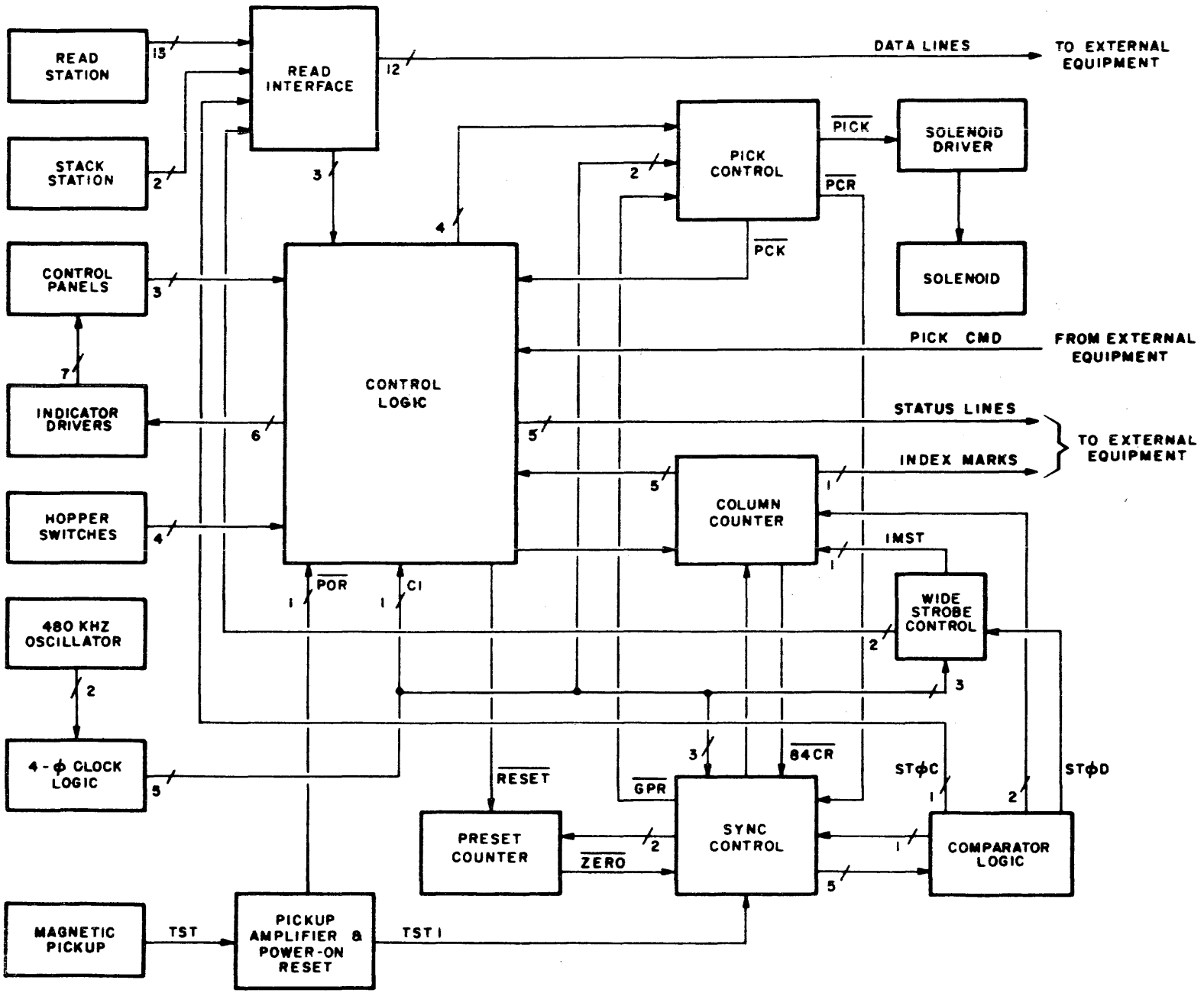


Figure 5. M Series Card Reader Logic Block Diagram

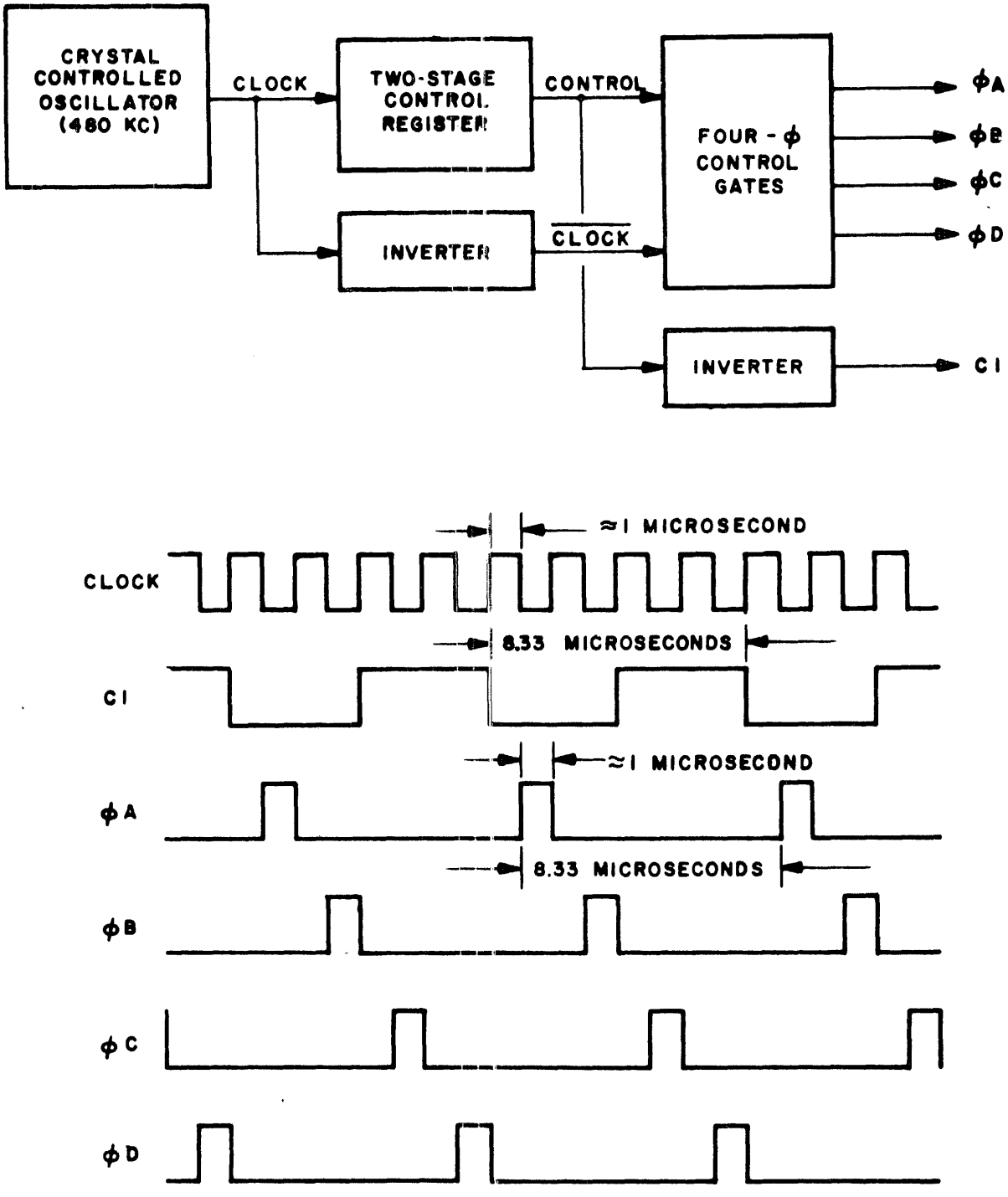
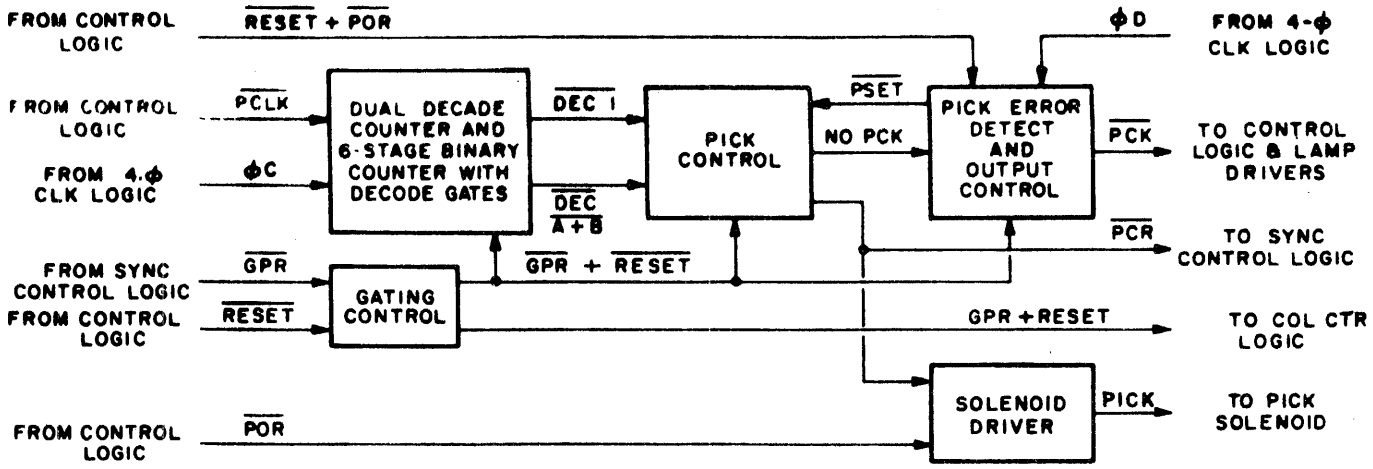
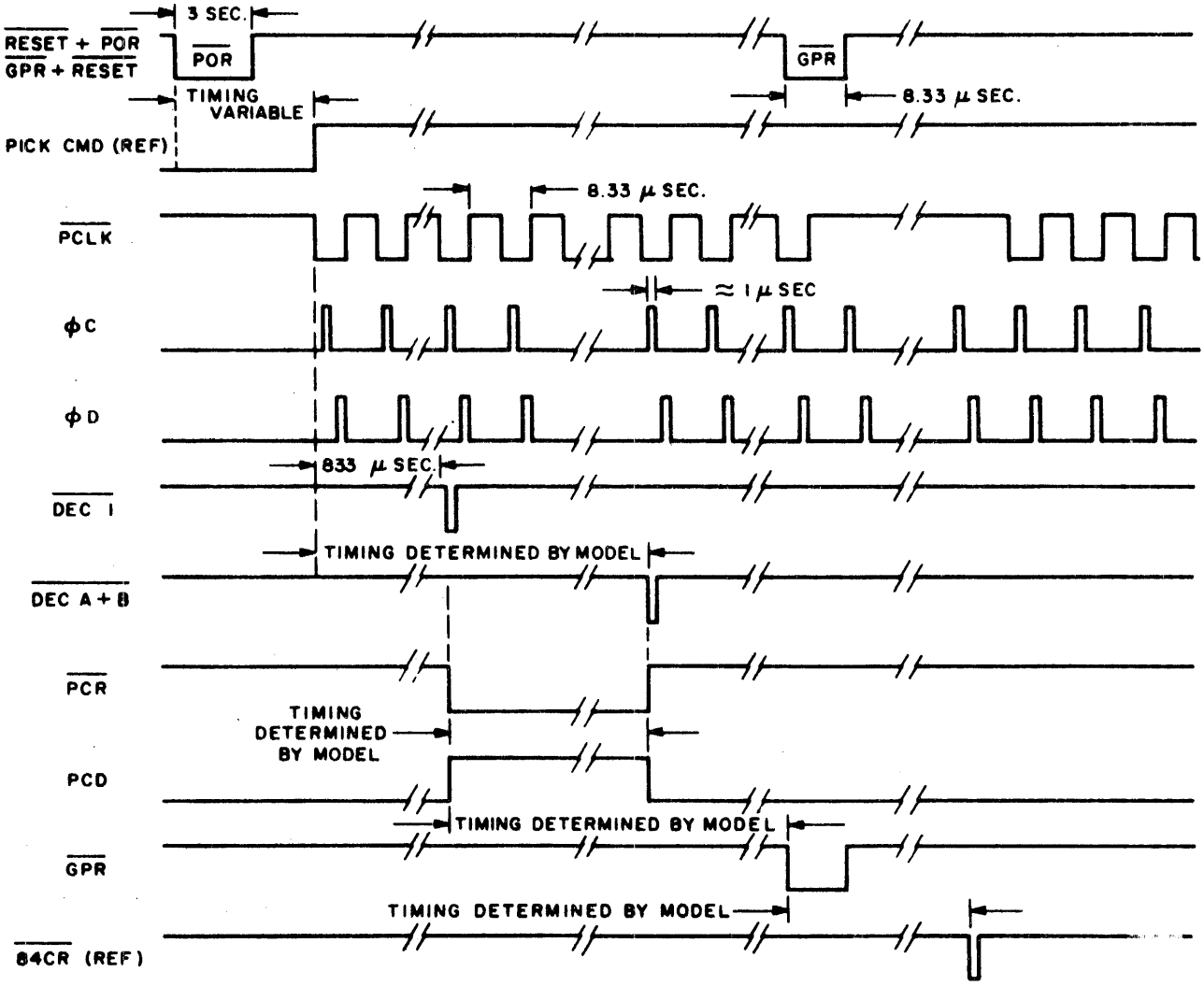


Figure 7. Oscillator/Four-Phase Clock Logic Block Diagram





NOTE: TIMING NOT SHOWN TO SCALE.

Figure 8. Pick Control Logic Block Diagram

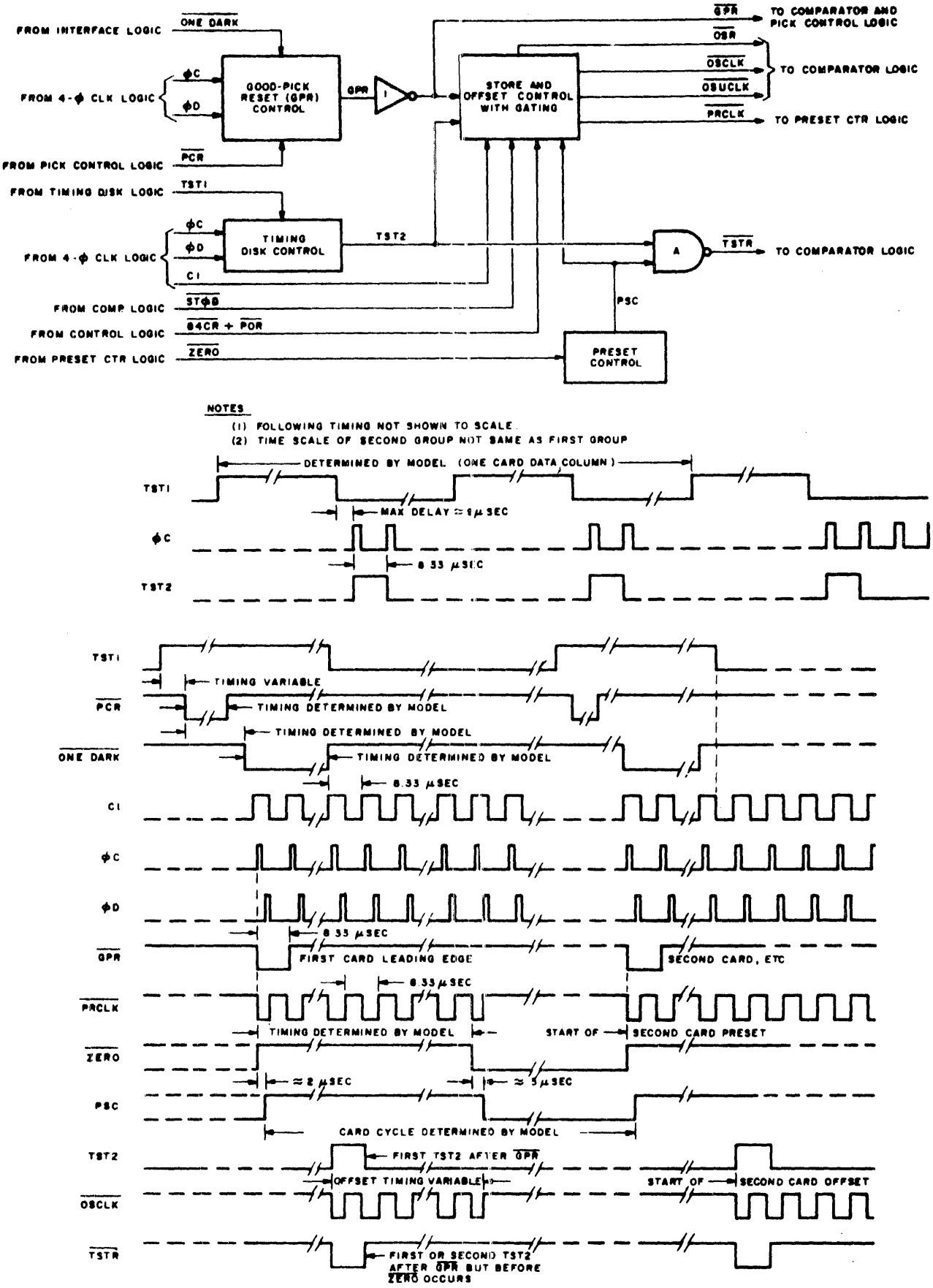


Figure 9. Sync Control Logic Block and Timing Diagram (Sheet 1 of 2).

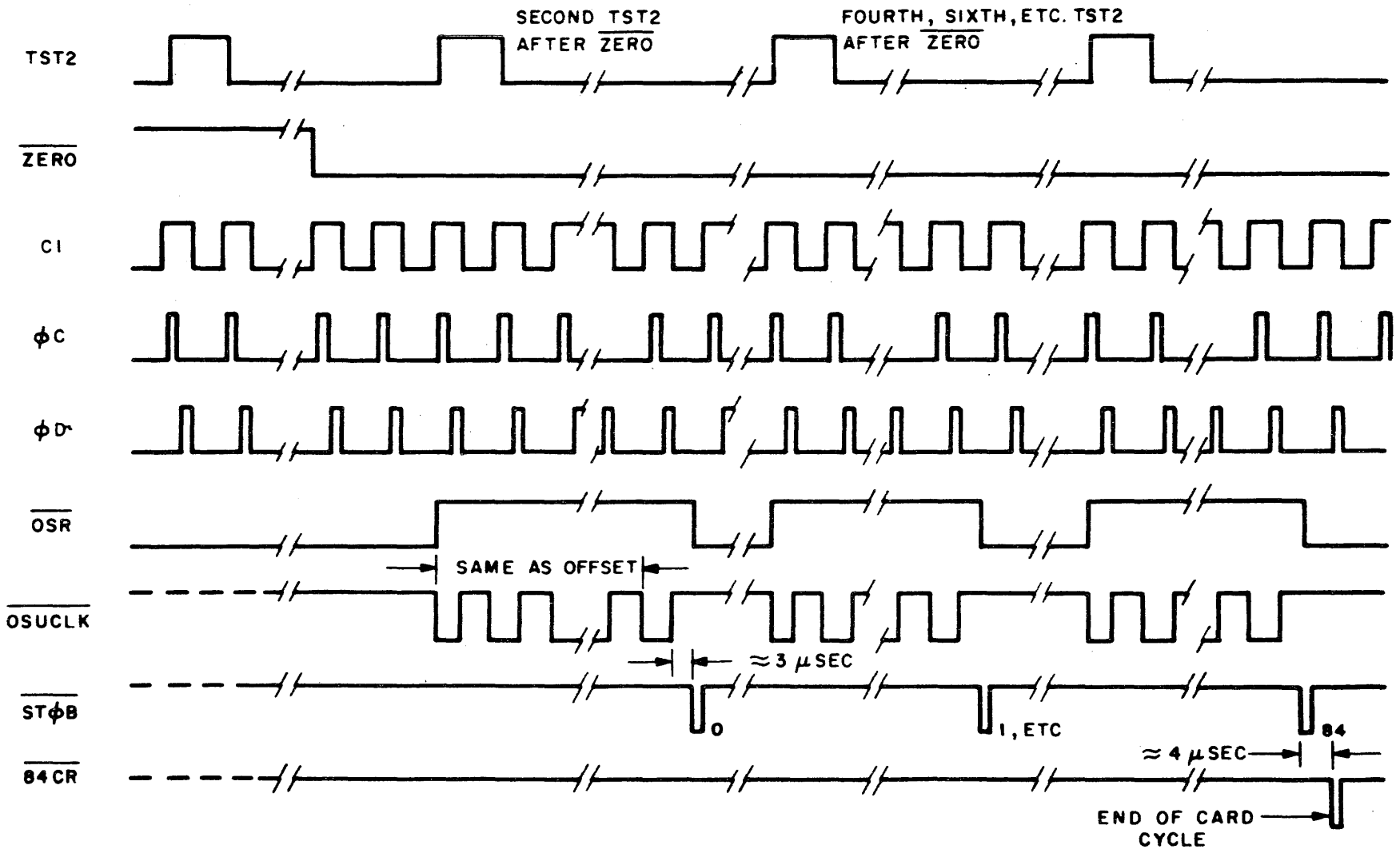


Figure 9. Sync Control Logic Block and Timing Diagram
(Sheet 2 of 2)

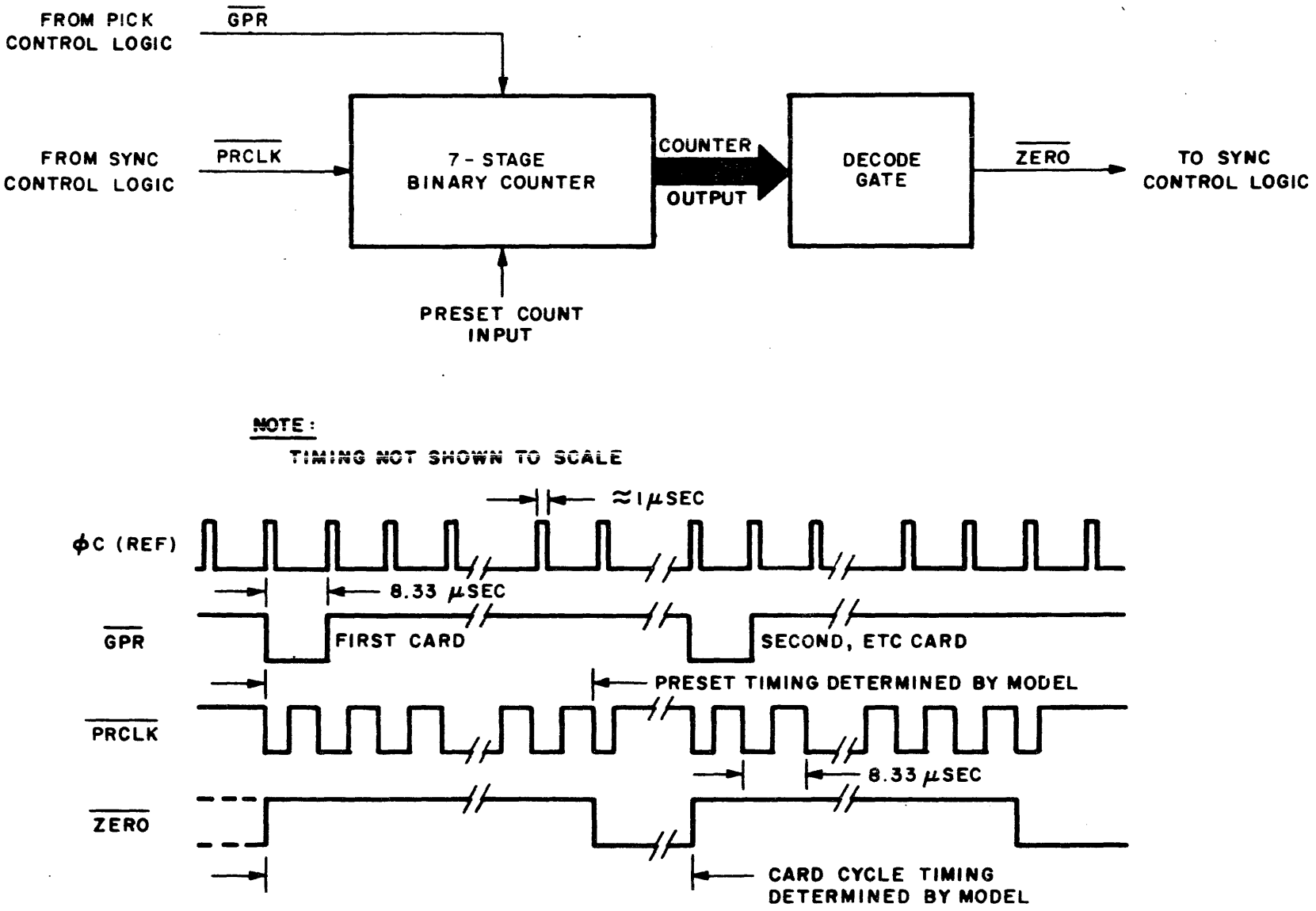


Figure 10. Preset Counter Logic Block Diagram

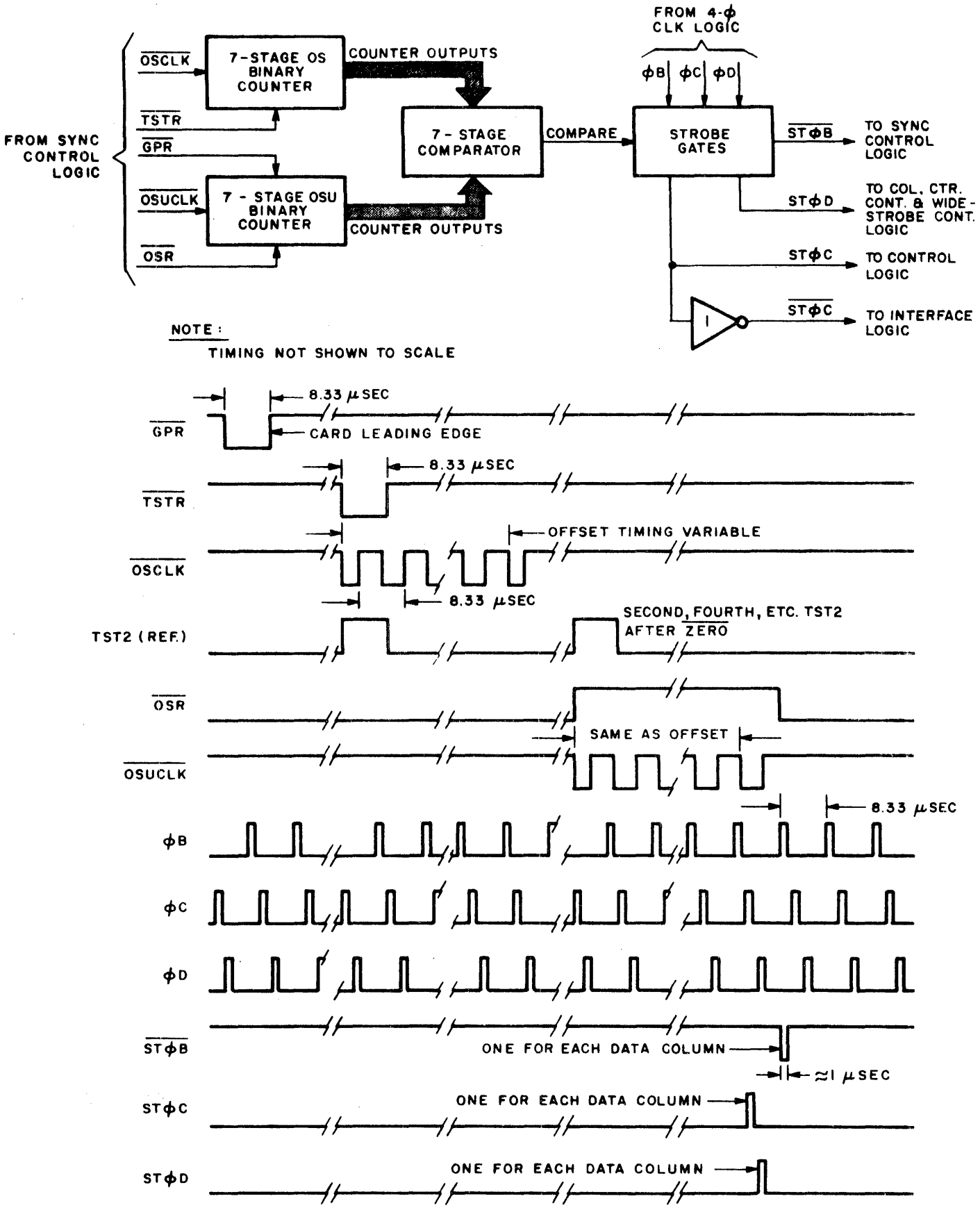
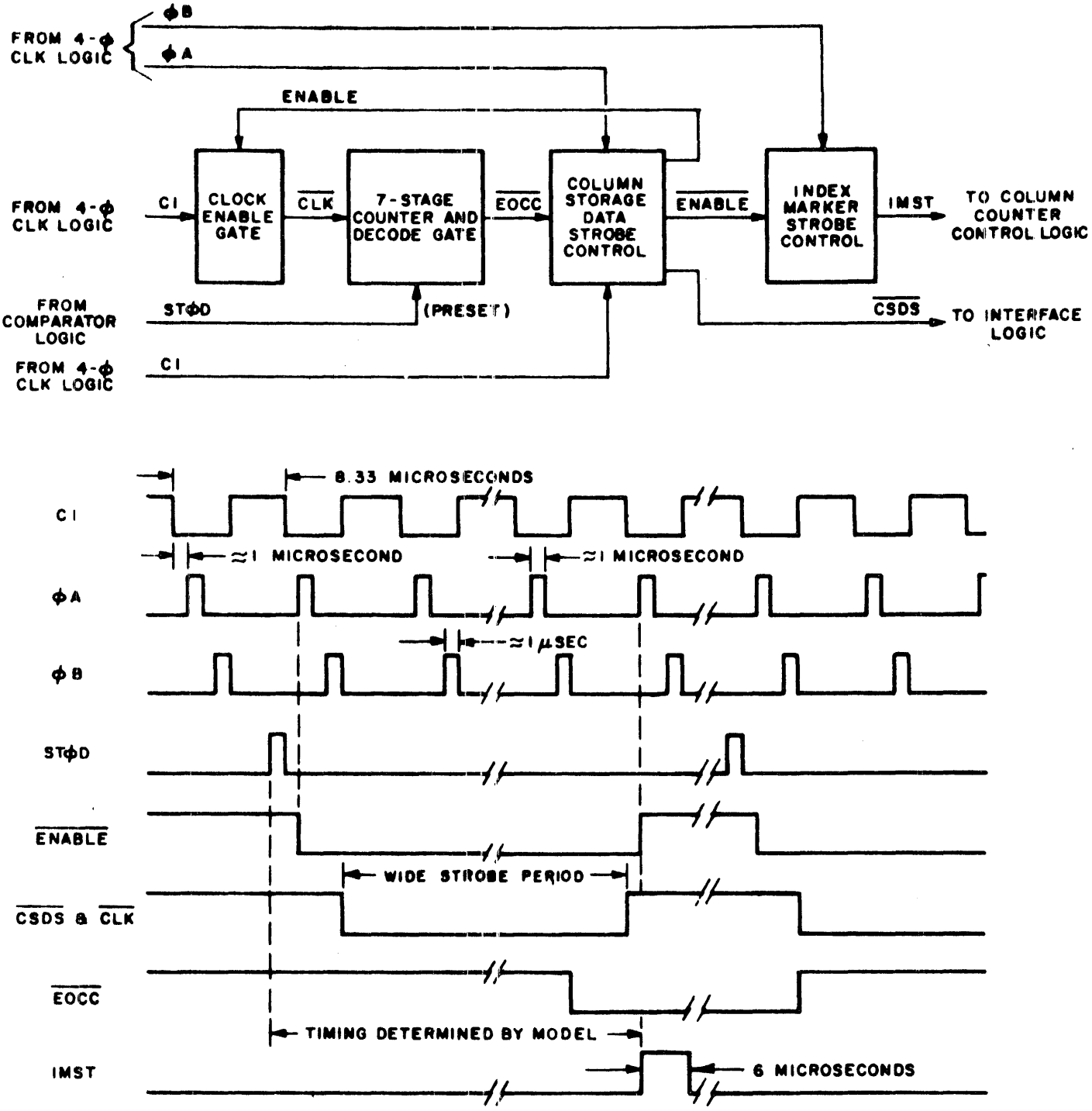


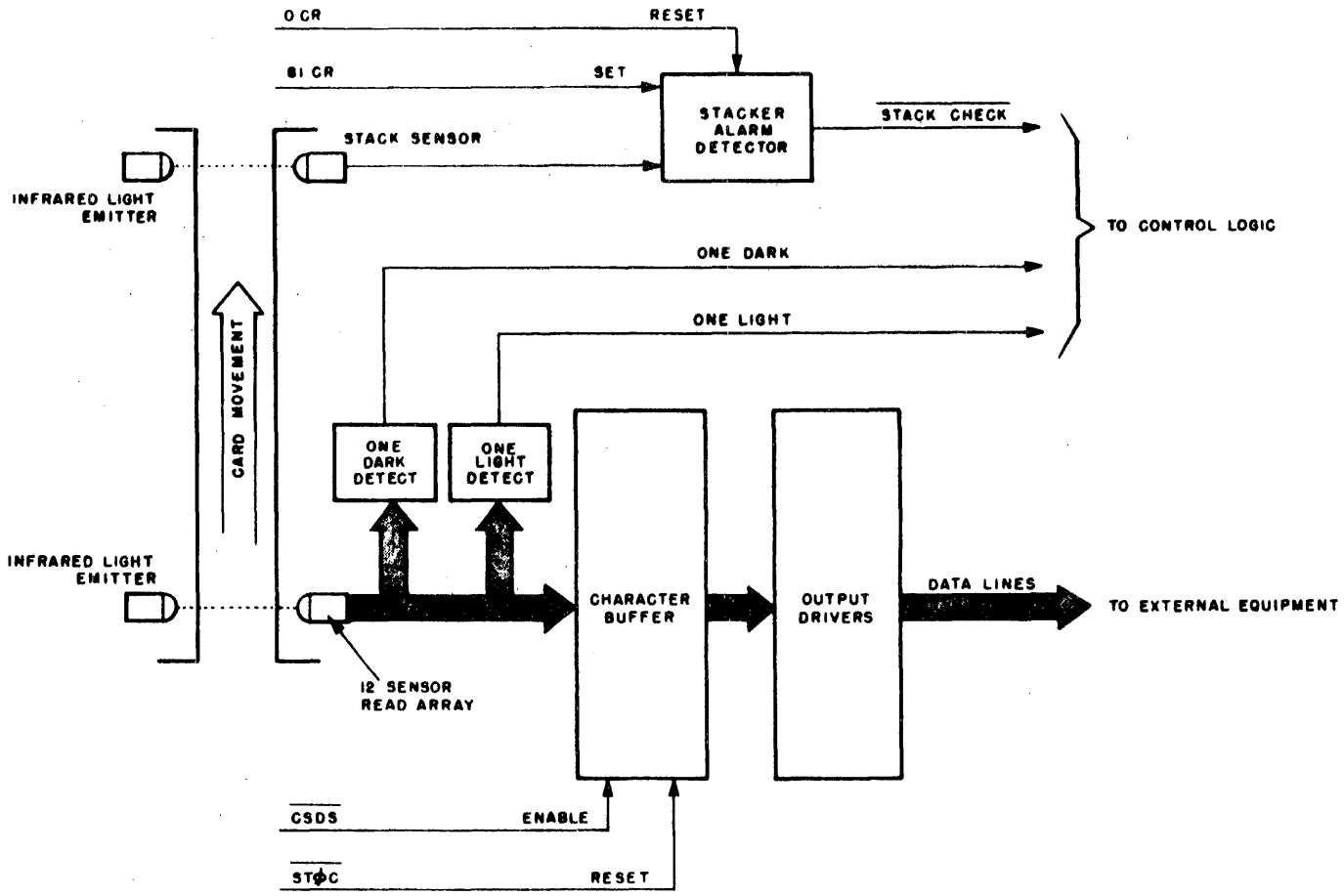
Figure 11. Comparator Logic Block Diagram

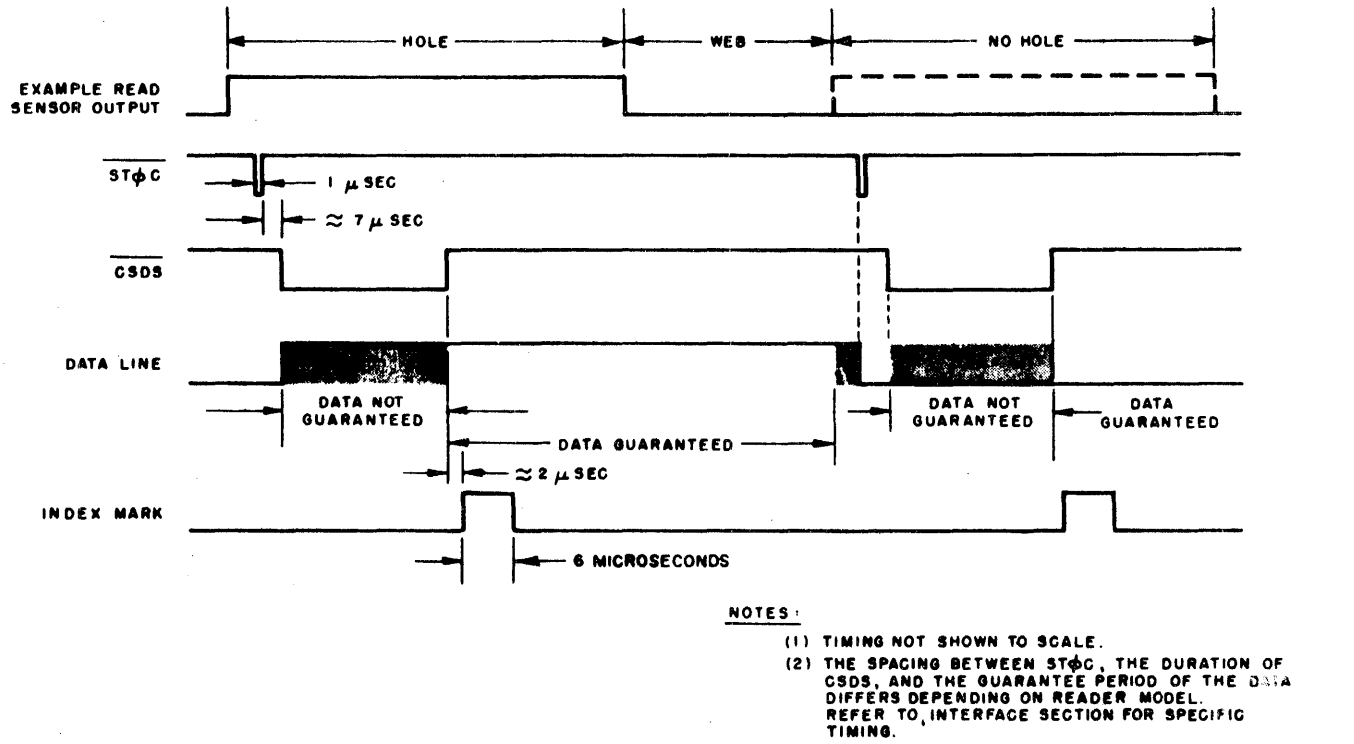


NOTES:

(1) STφD SYNCHRONIZED TO CARD DATA COLUMNS.
(2) TIMING NOT SHOWN TO SCALE.

Figure 12. Wide-Strobe Control Logic Block Diagram



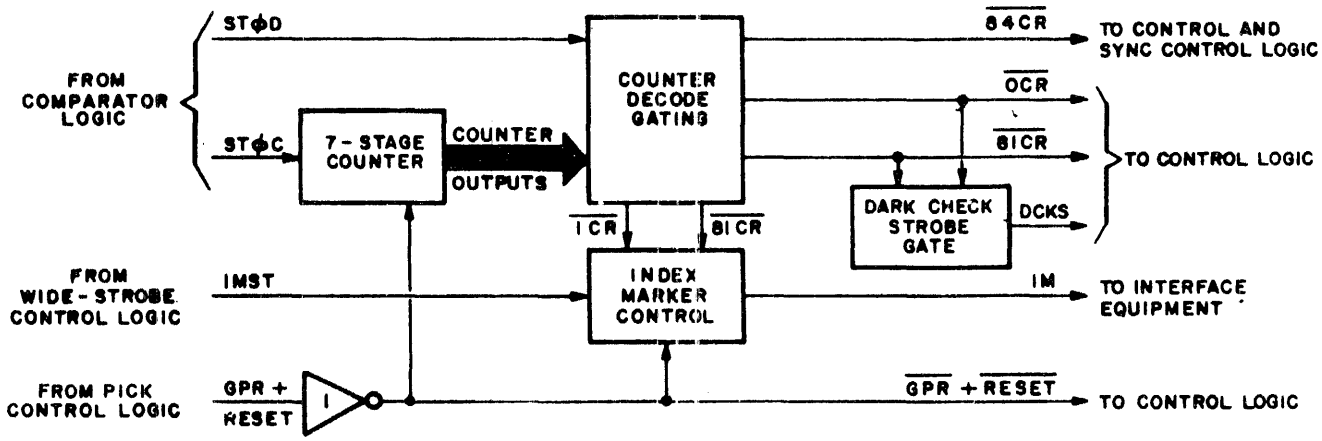


NOTES:

(1) TIMING NOT SHOWN TO SCALE.

(2) THE SPACING BETWEEN STΦC, THE DURATION OF CSDS, AND THE GUARANTEE PERIOD OF THE DATA DIFFERS DEPENDING ON READER MODEL. REFER TO INTERFACE SECTION FOR SPECIFIC TIMING.

Figure 13. Character Buffer Storage Logic Block Diagram



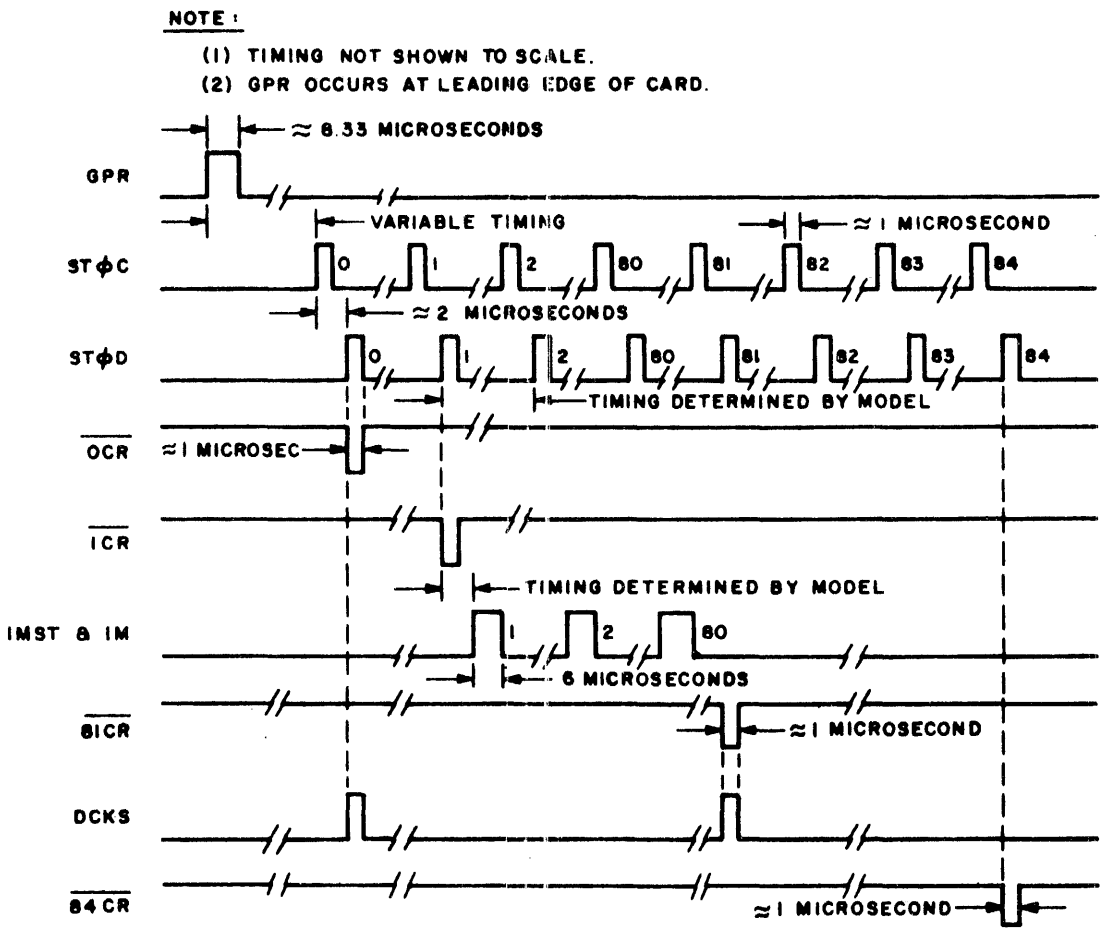


Figure 14. Column Counter Control Logic Block Diagram

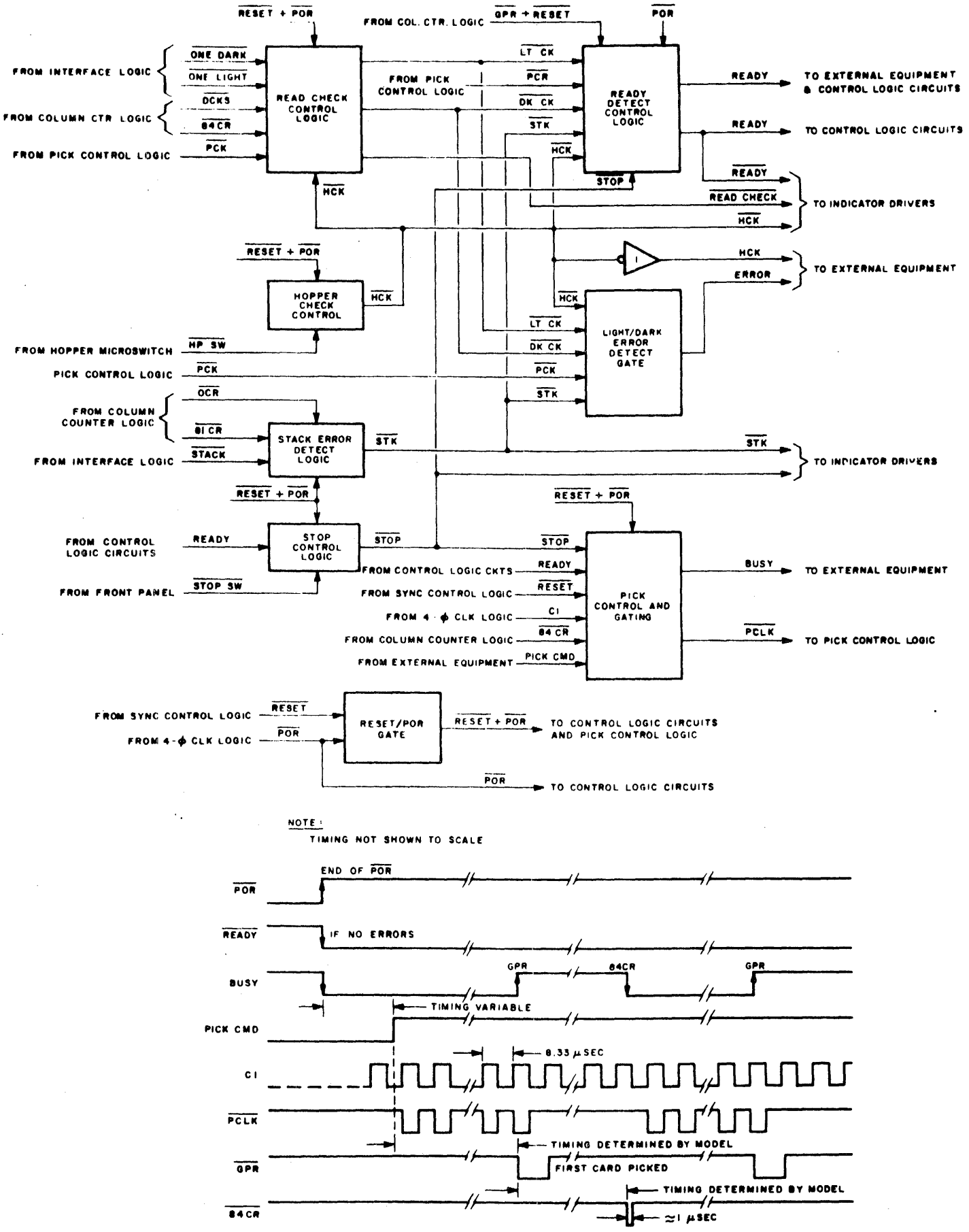
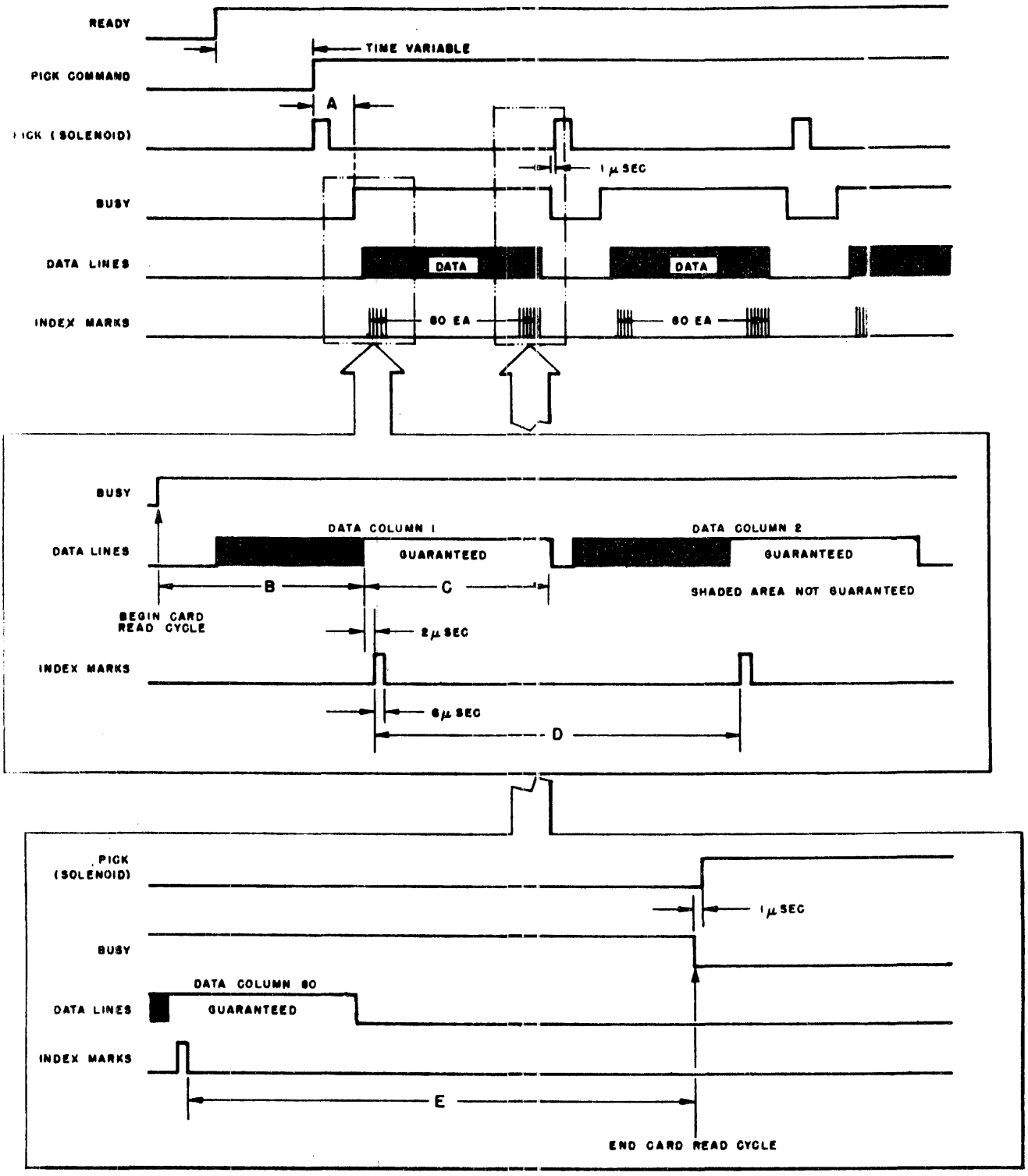


Figure 15. Control Logic Block and Timing Diagram



MODEL	A (MIN)	B	C	D	E	CARD PICK CYCLE
M200	24	6250	1314	2014	8050	200
M300	24	2600	435	870	102,660	200
M600	24	2600	435	870	3480	100
M1000	15	1860	240	478	1910	60
M1200	14	1120	240	406	1529	50
	M SEC	μ SEC	μ SEC	μ SEC	μ SEC	M SEC

NOTE:
WAVEFORMS NOT SHOWN TO SCALE.

Figure 16. Standard Interface Timing for M Series Readers

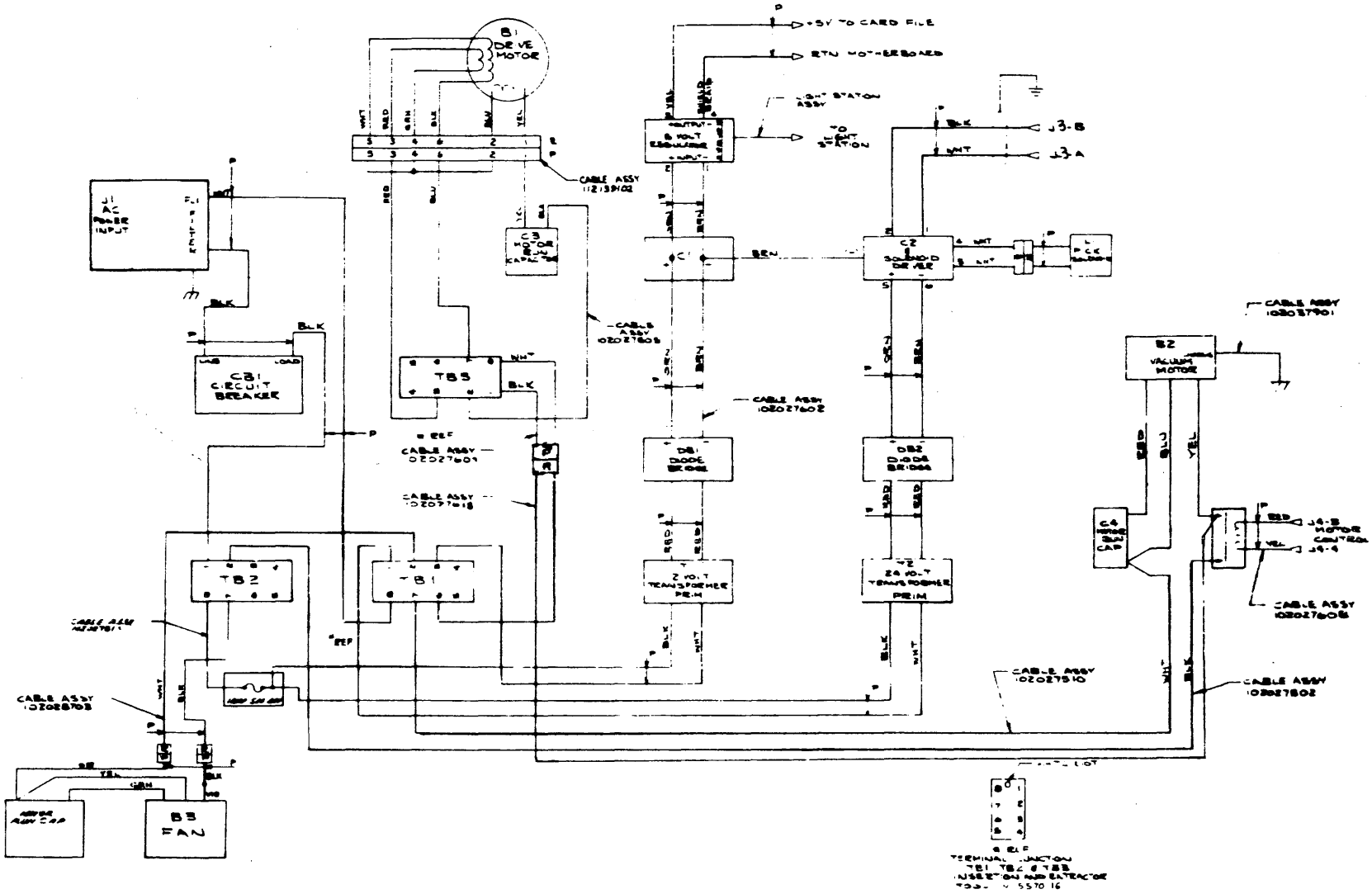


Figure A1A. Wiring Diagram, AC Power Distribution, 230 VAC, 50 Hz
Dwg. No. 1040819

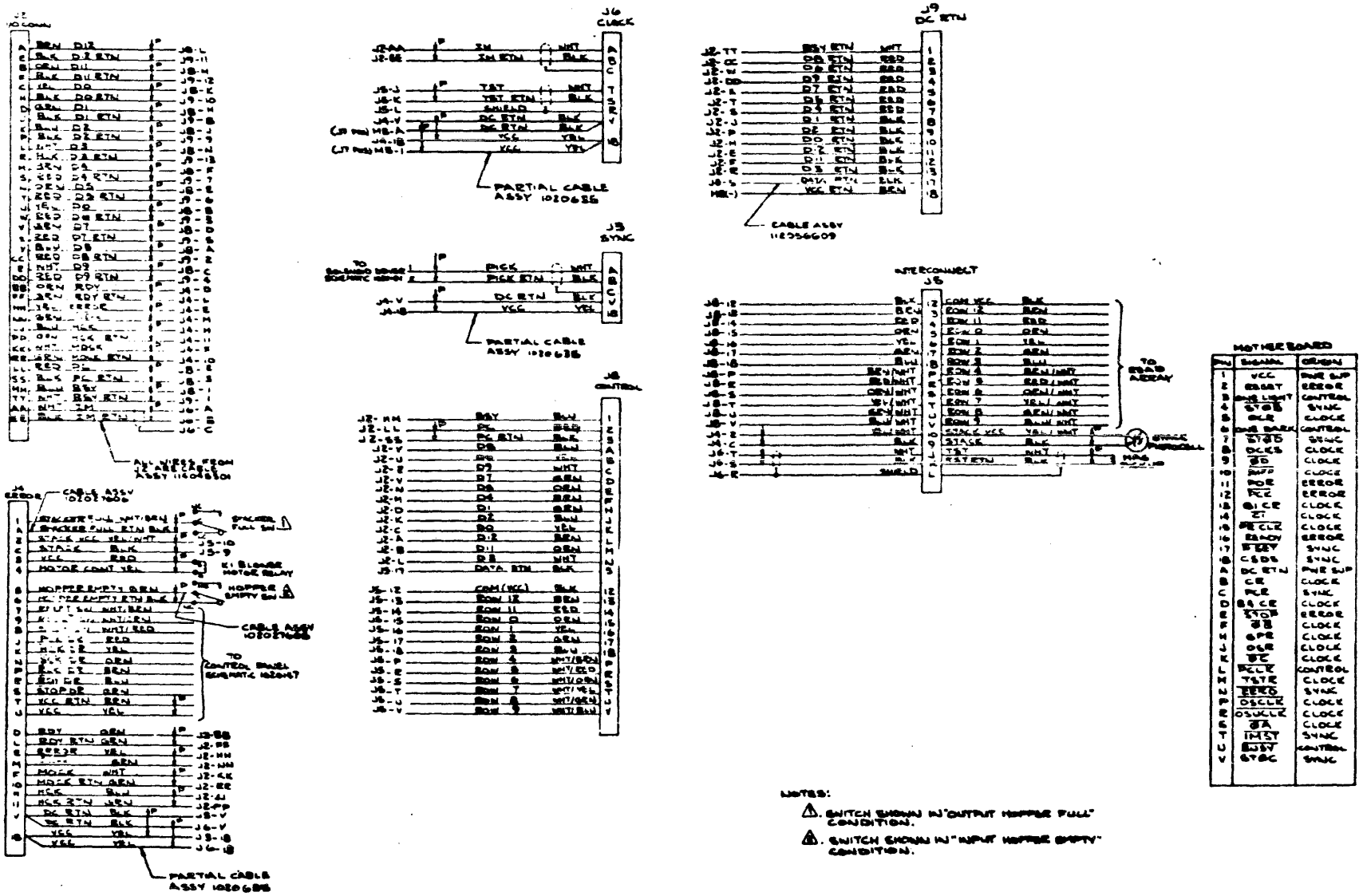


Figure A1. Wiring Diagram, Card Cage
(Dwg. No. 1141934) CS 139A

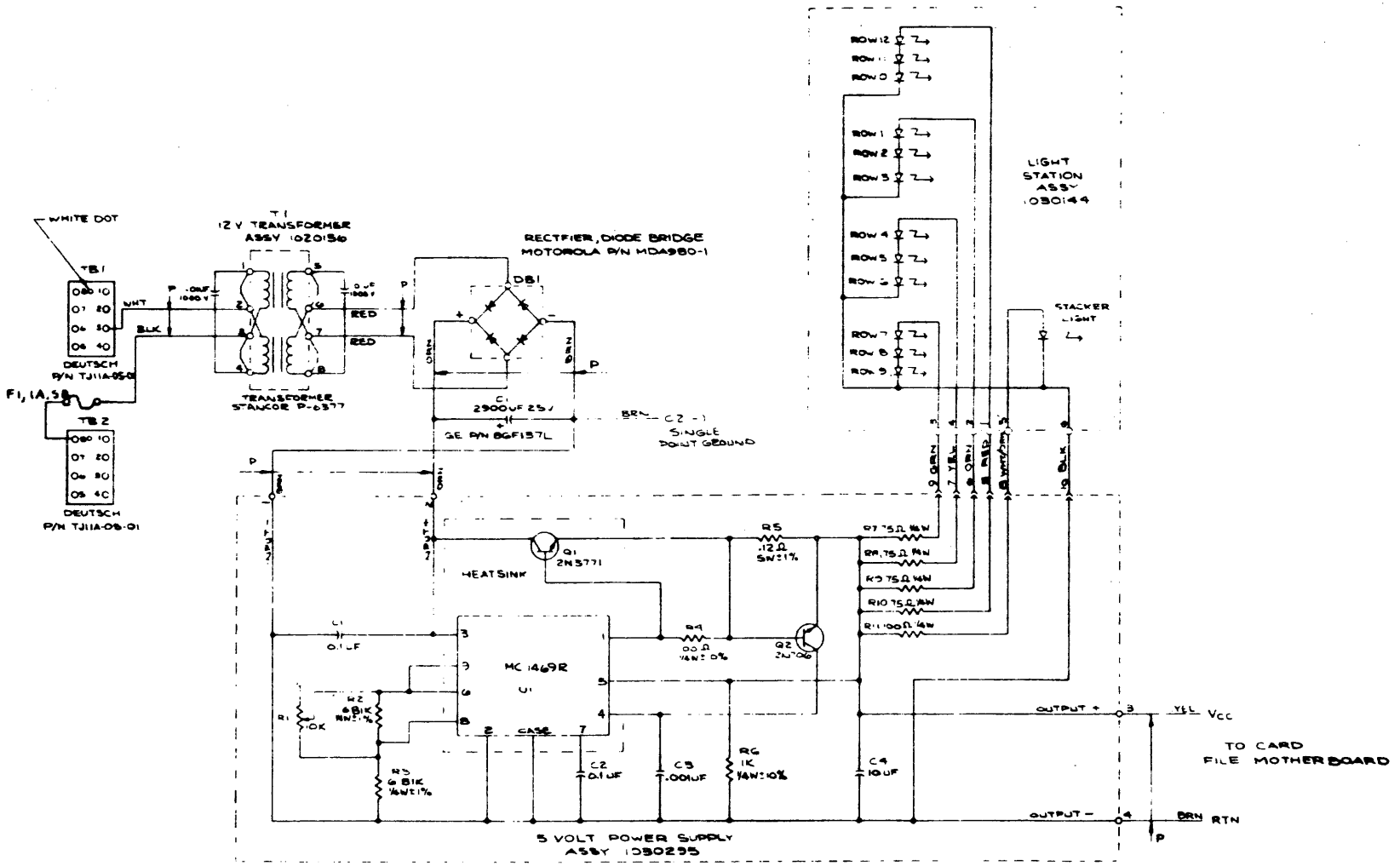


Figure A2. 5 Volt Power Supply
Dwg. No. 1140637

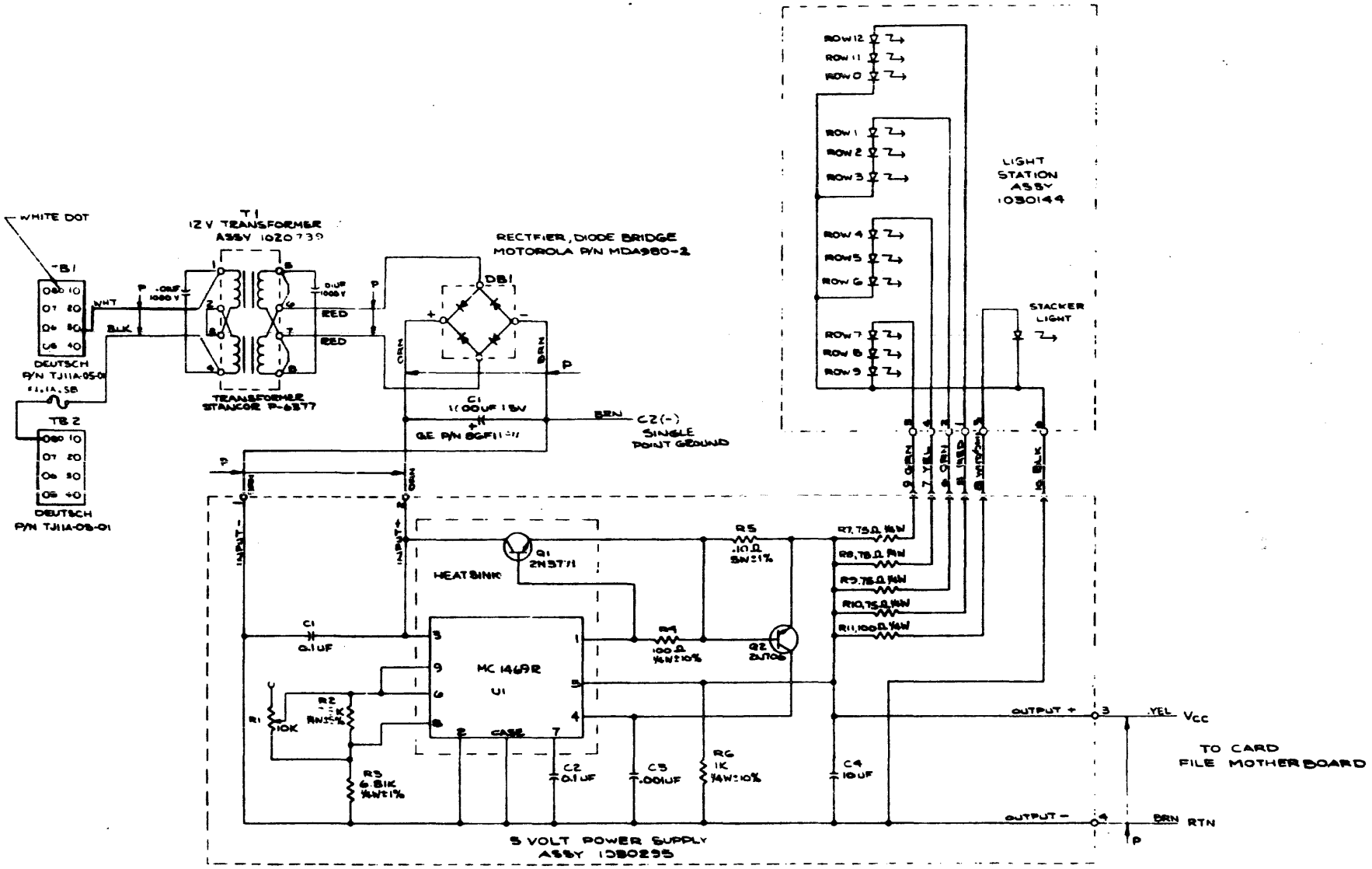


Figure A2A. 5 Volt Power Supply

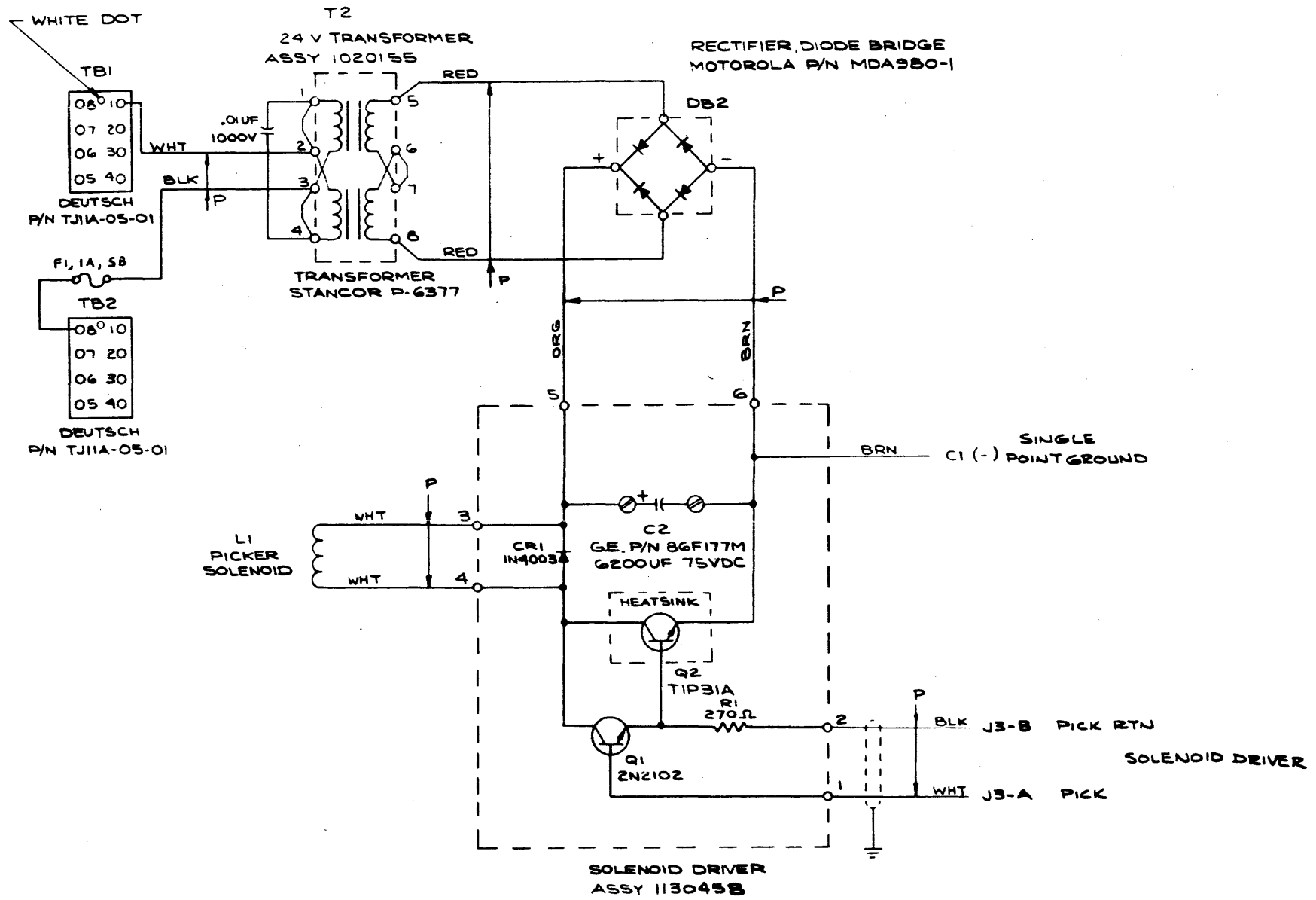


Figure A3. Solenoid Driver
Dwg. No. 1140623

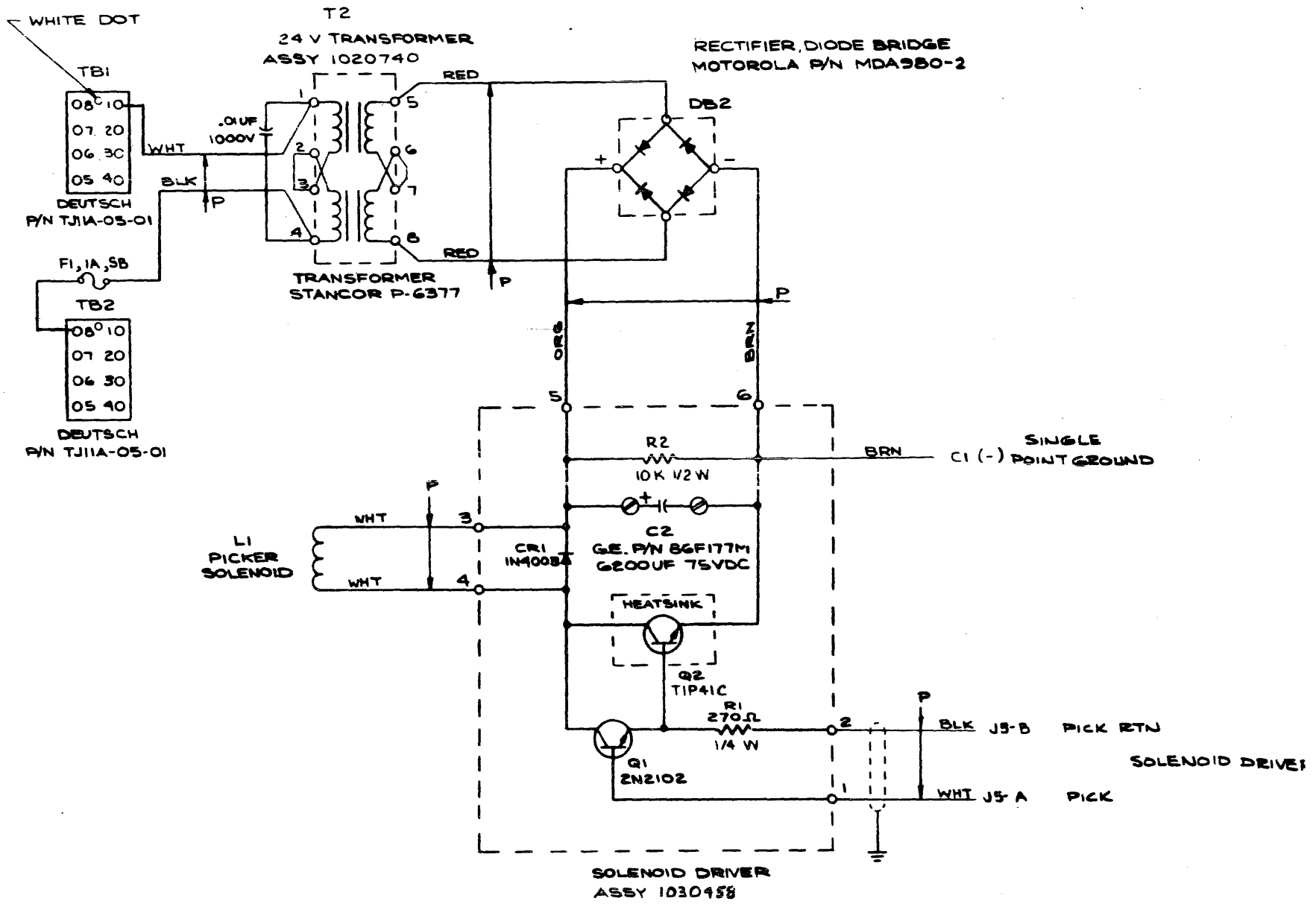
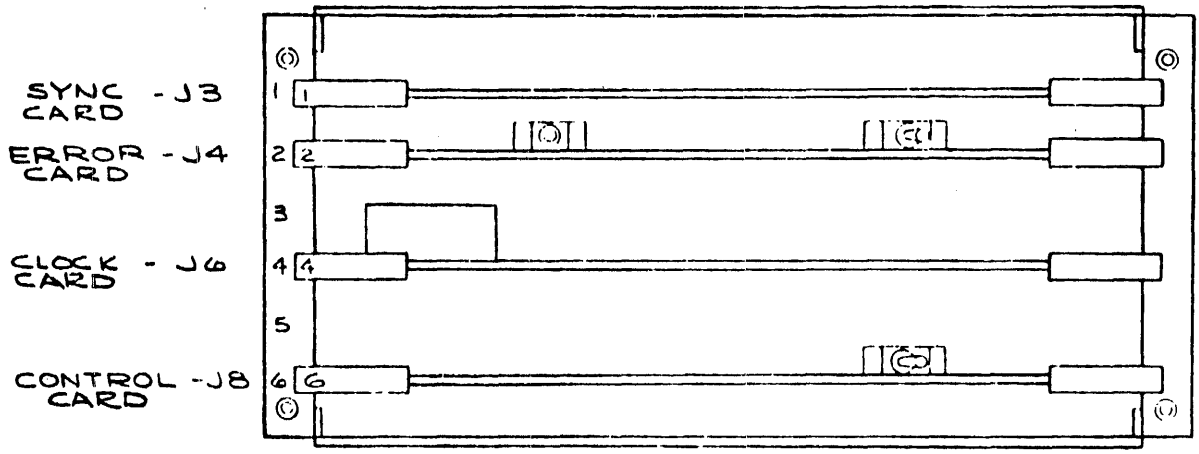
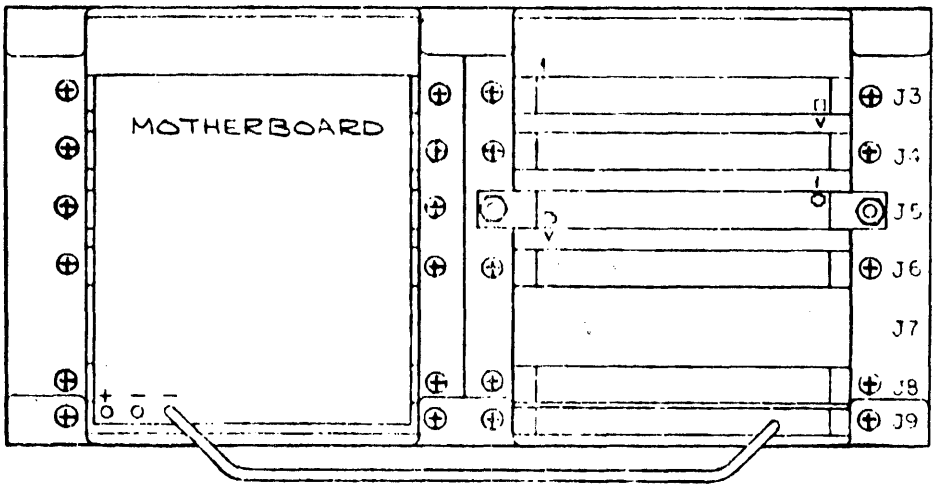


Figure A3A. Solenoid Driver



CARD FILE, REAR VIEW
COVER REMOVED



CONNECTOR VIEW

Figure A4. Card File

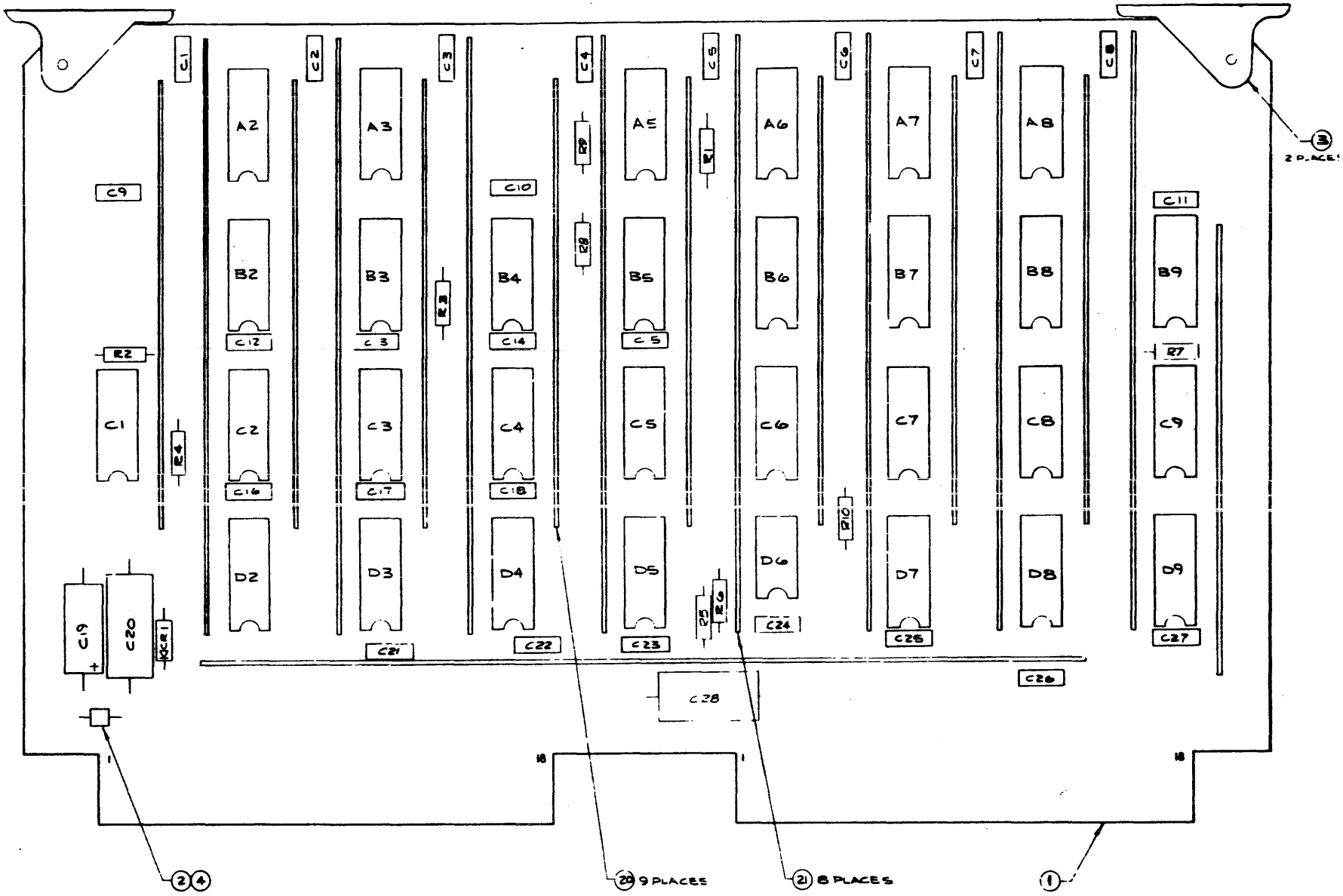


Figure A5. Sync Card Assembly
Dwg. No. 1040353

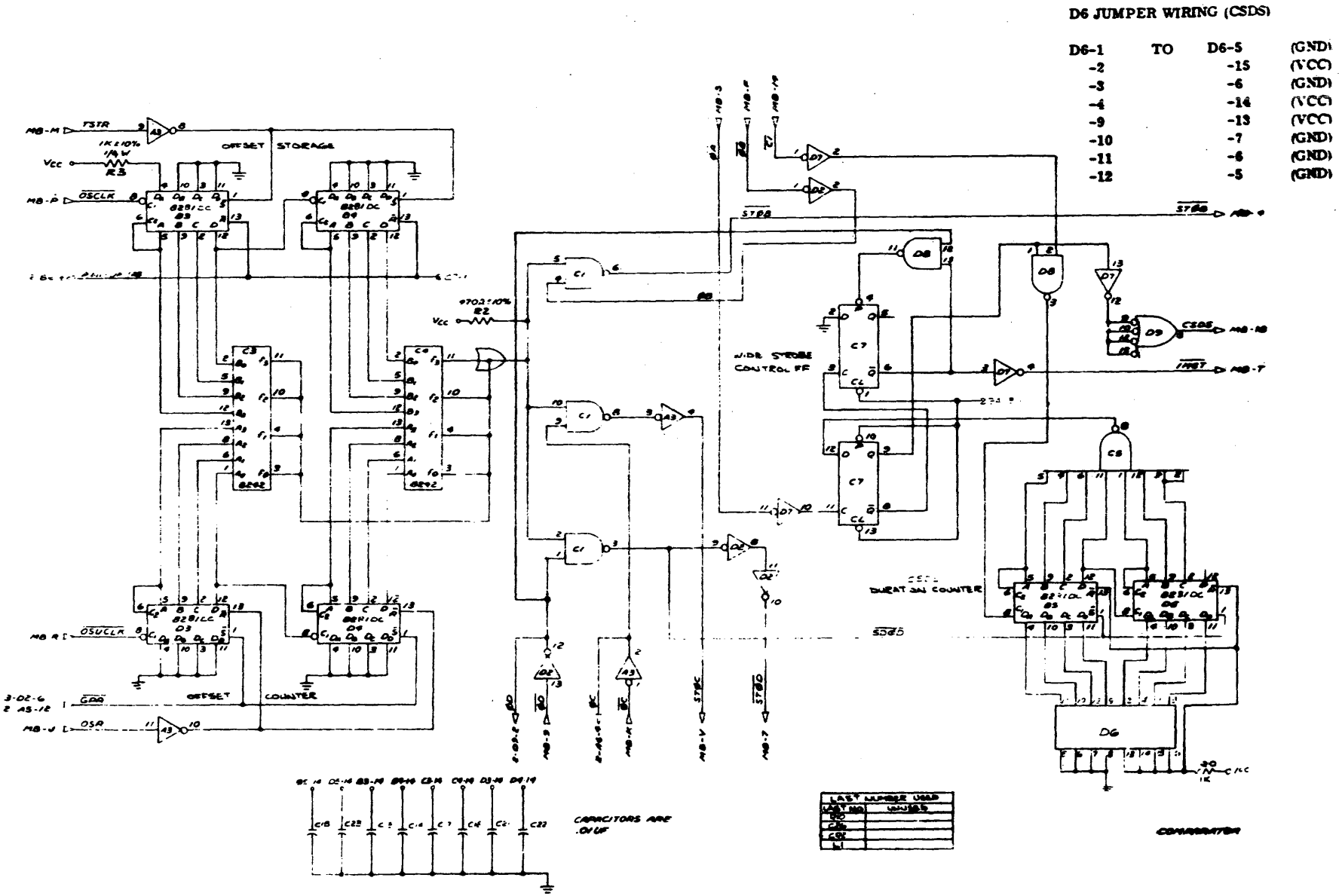


Figure A6. Sync Card Schematic Dwg. No. 1640943 (Sheet 1 of 3) (M-200)

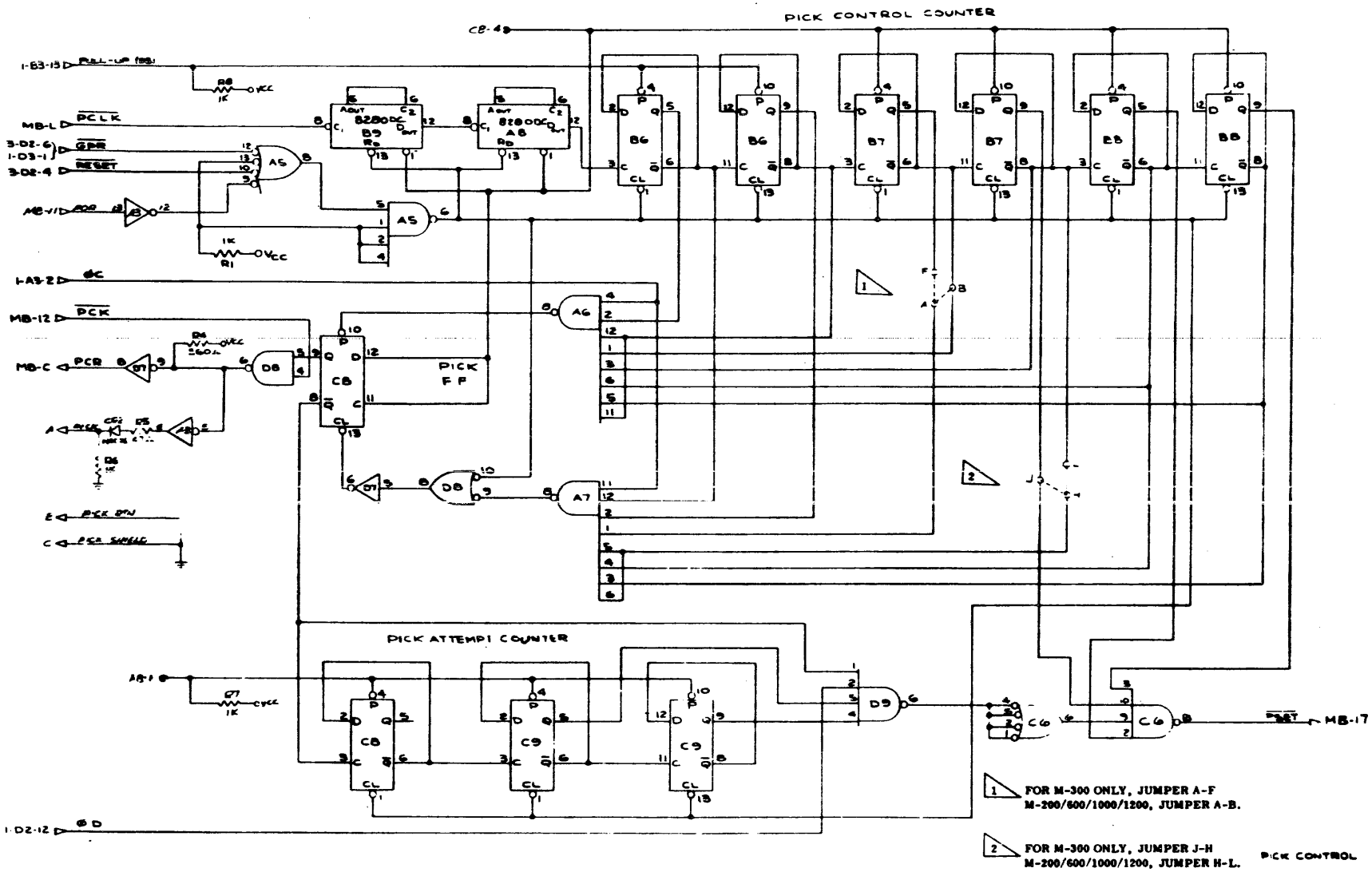
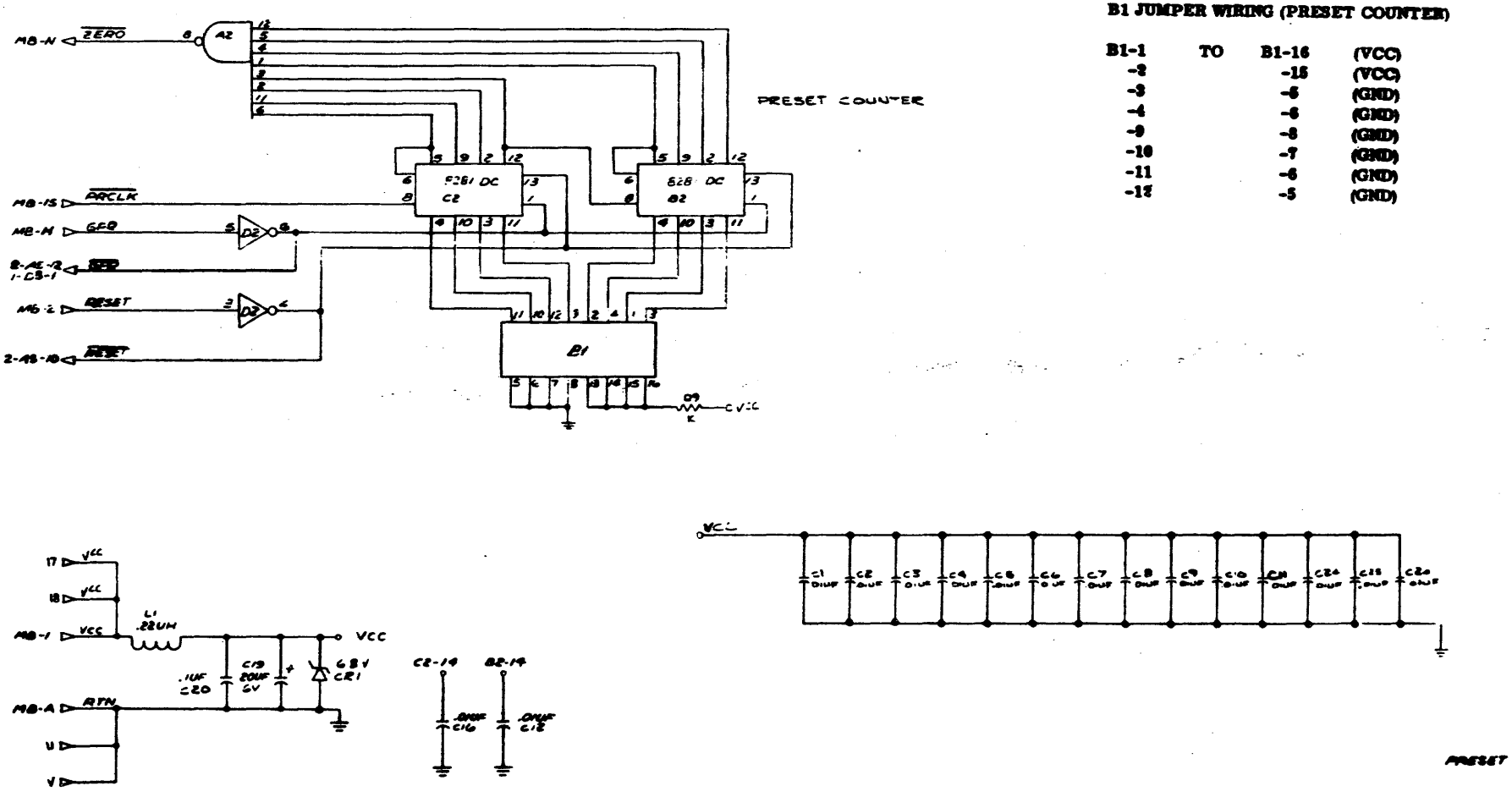


Figure A6. (Sheet 2 of 3)



B1 JUMPER WIRING (PRESET COUNTER)

B1-1	TO	B1-16	(VCC)
-2		-15	(VCC)
-3		-5	(GND)
-4		-6	(GND)
-9		-8	(GND)
-10		-7	(GND)
-11		-6	(GND)
-12		-5	(GND)

A9

Figure A6. Sync Card Schematic Dwg. No. 1640943 (Sheet 3 of 3) (M-200)

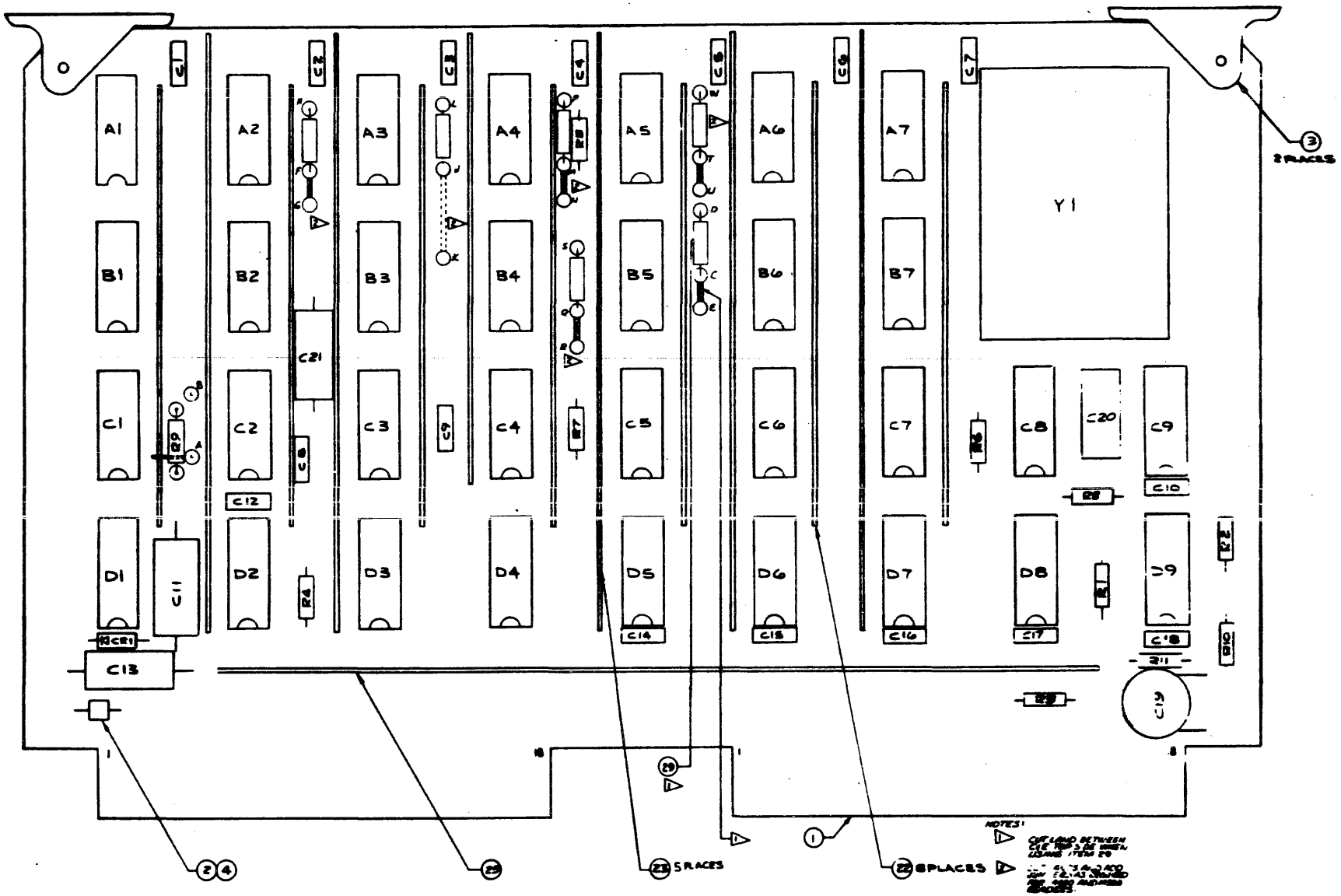


Figure A8. Assembly Diagram, Clock Card
(Dwg. No. 1040765

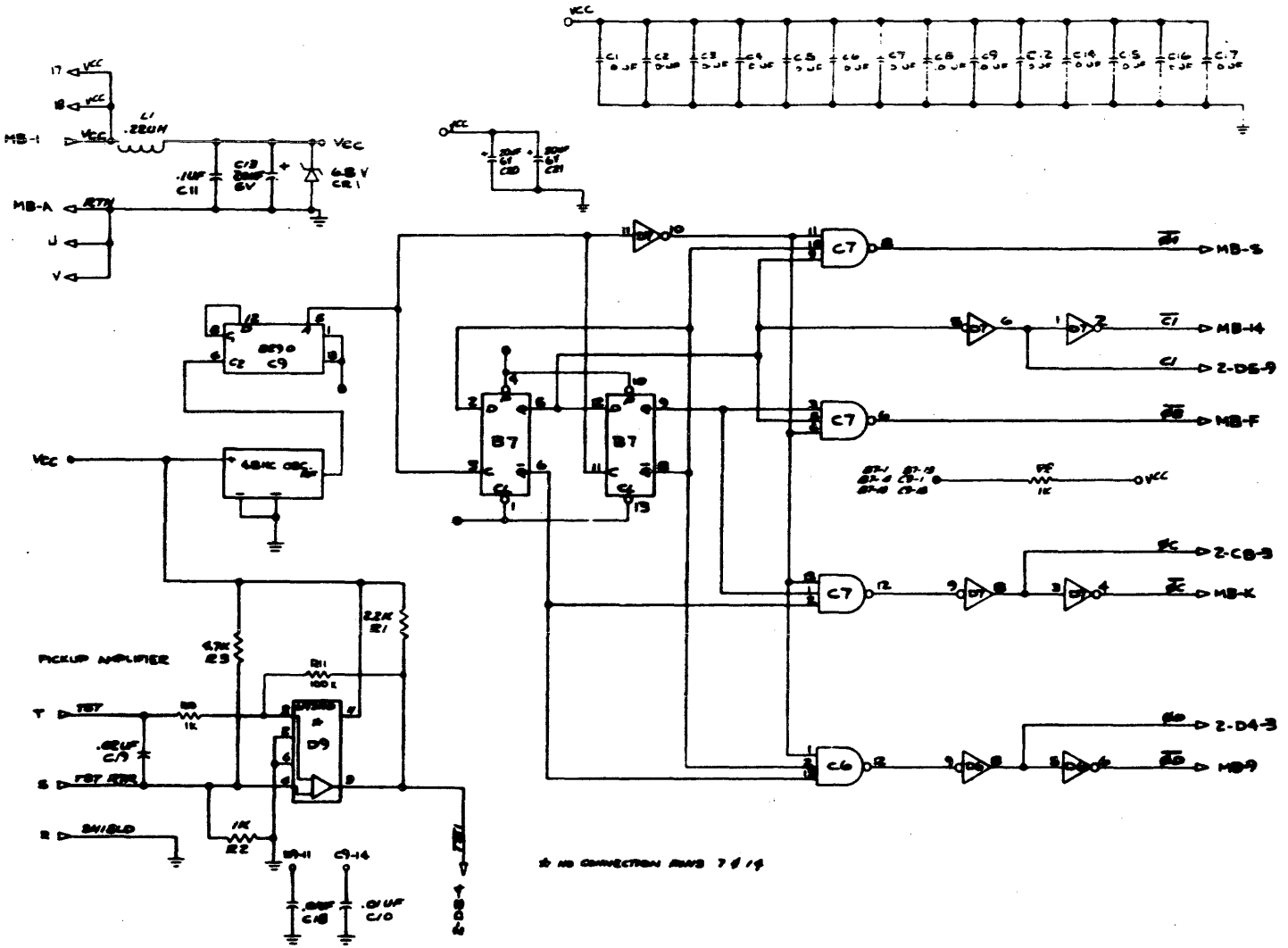


Figure A8. Clock Card Schematic (Sheet 1 of 3)
Dwg. No. 1040800C

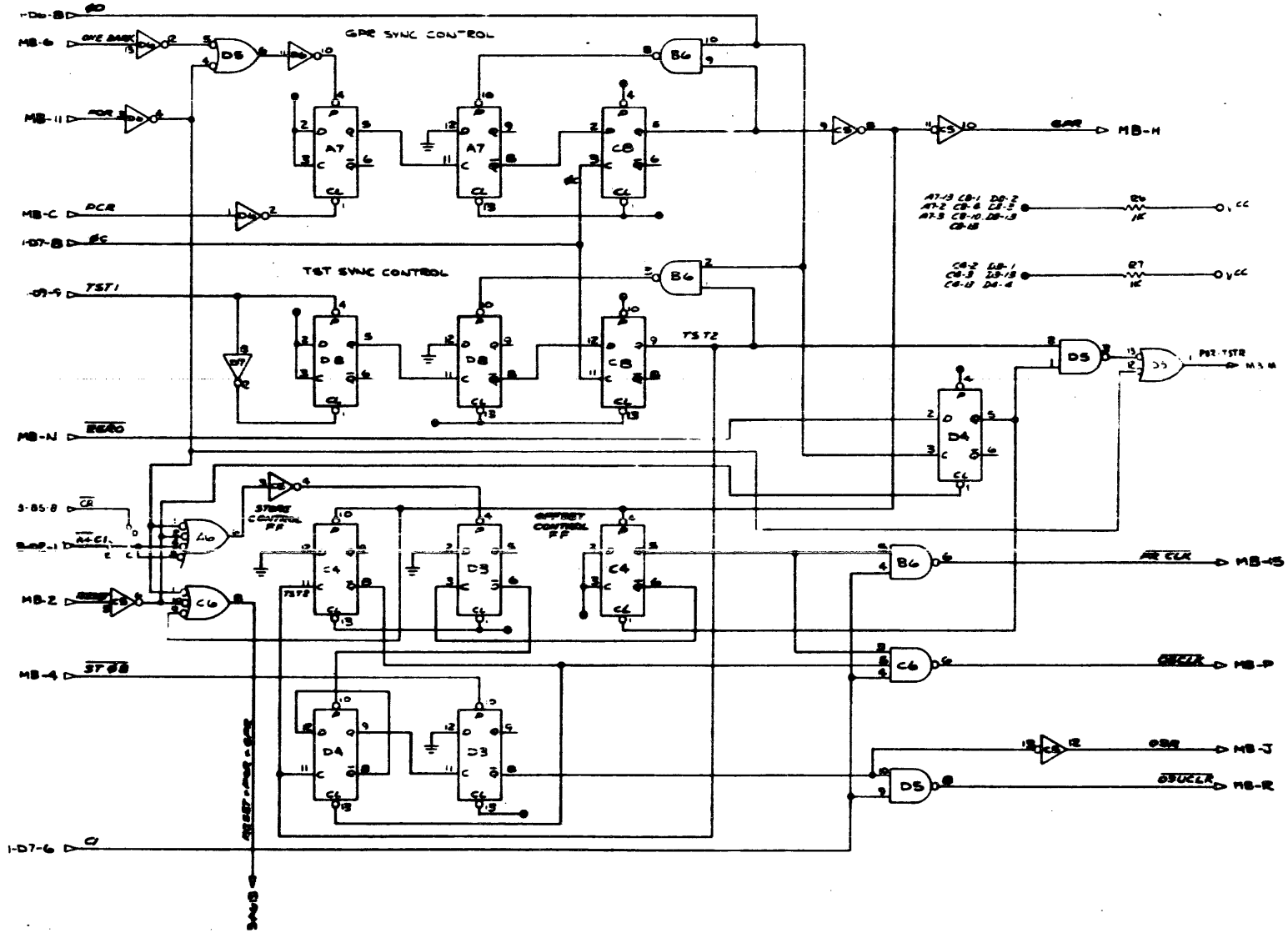


Figure A8. (Sheet 2 of 3)

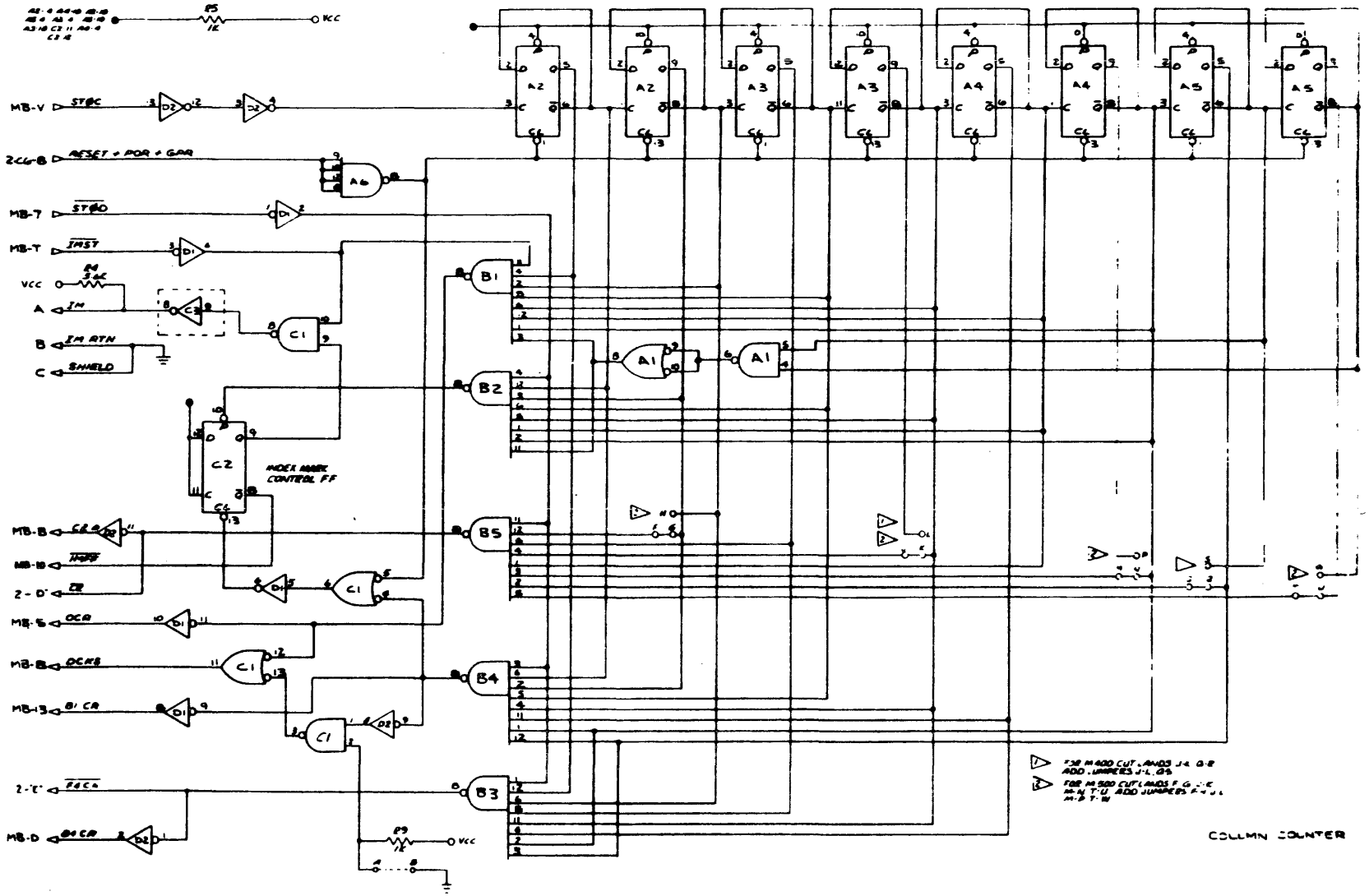


Figure A8. Schematic Diagram, Clock Card, (Sh. 3 of 3)

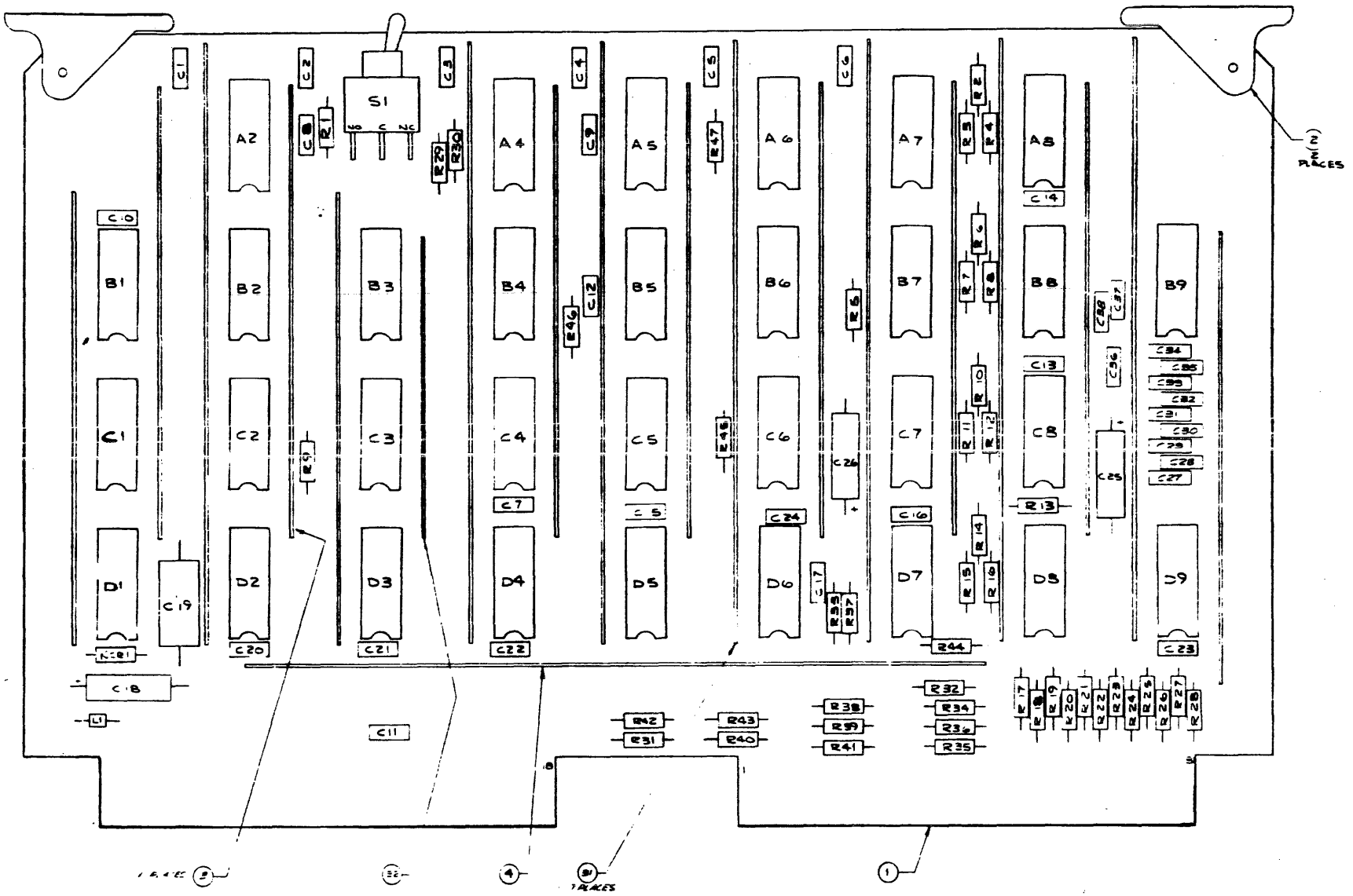


Figure A9. Control Card Assembly
Dwg. No. 1040619

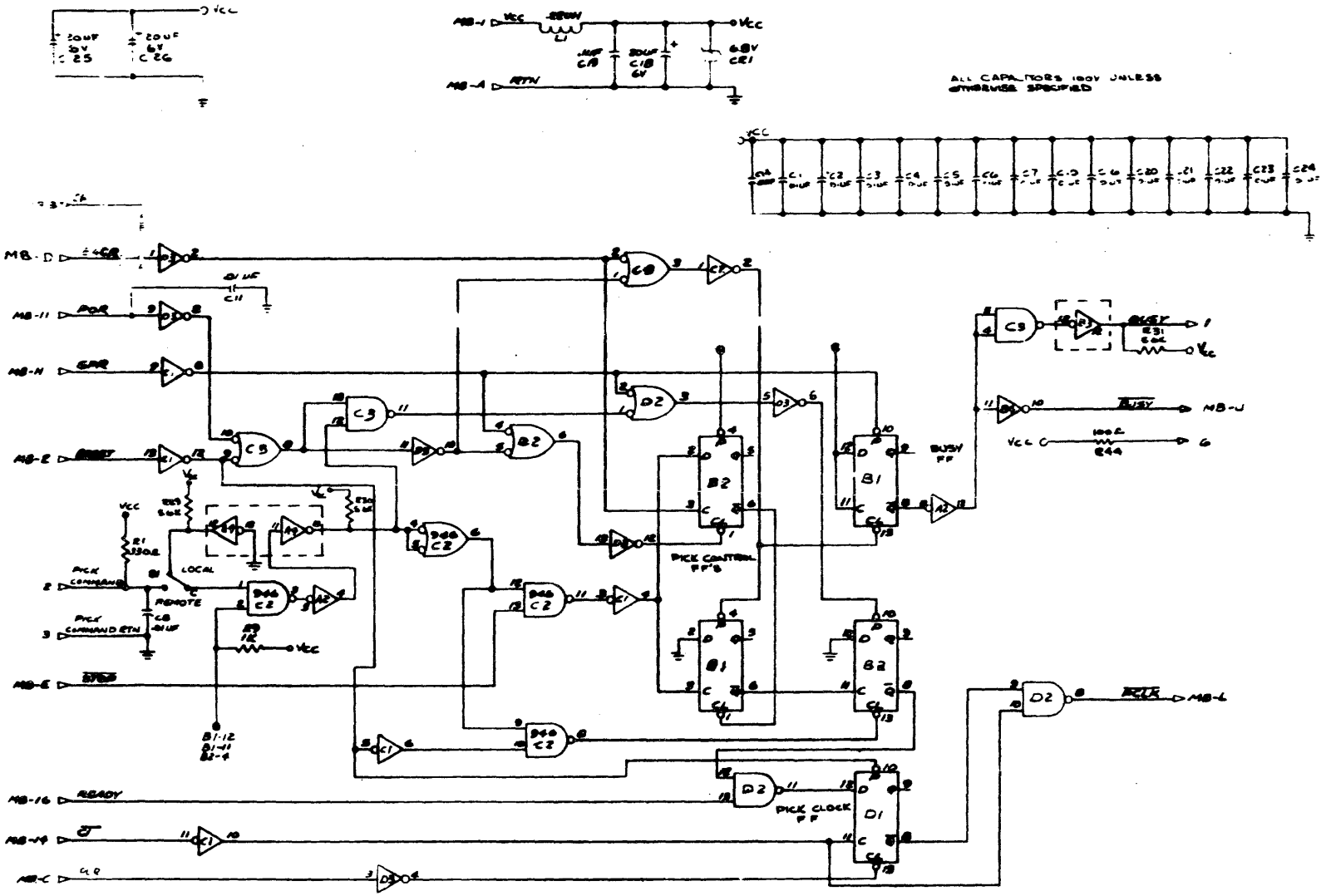


Figure A10. Control Card Schematic (Sheet 1 of 2)
Dwg. No. 1040650D

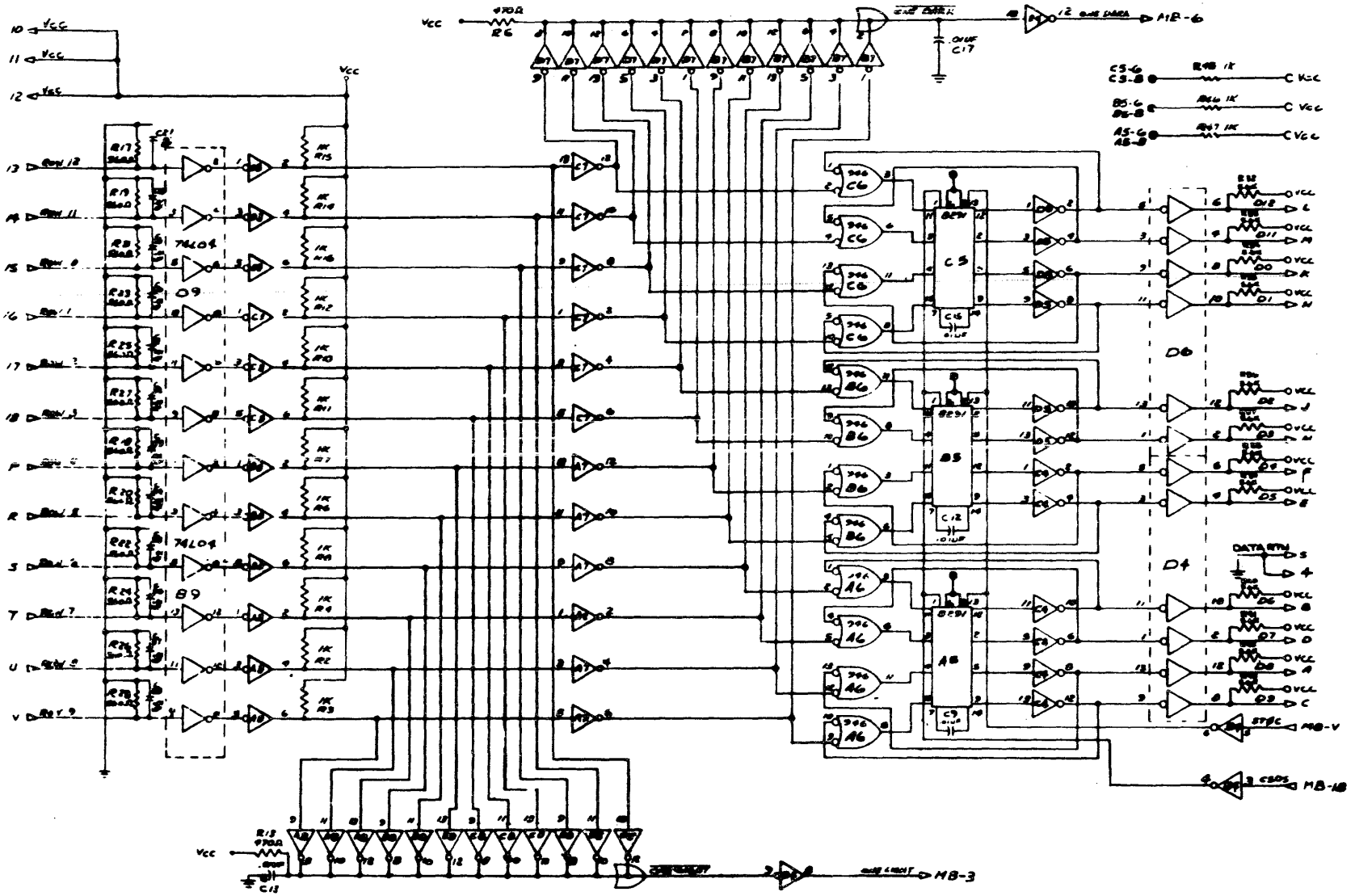


Figure A10. (Sheet 2 of 2)

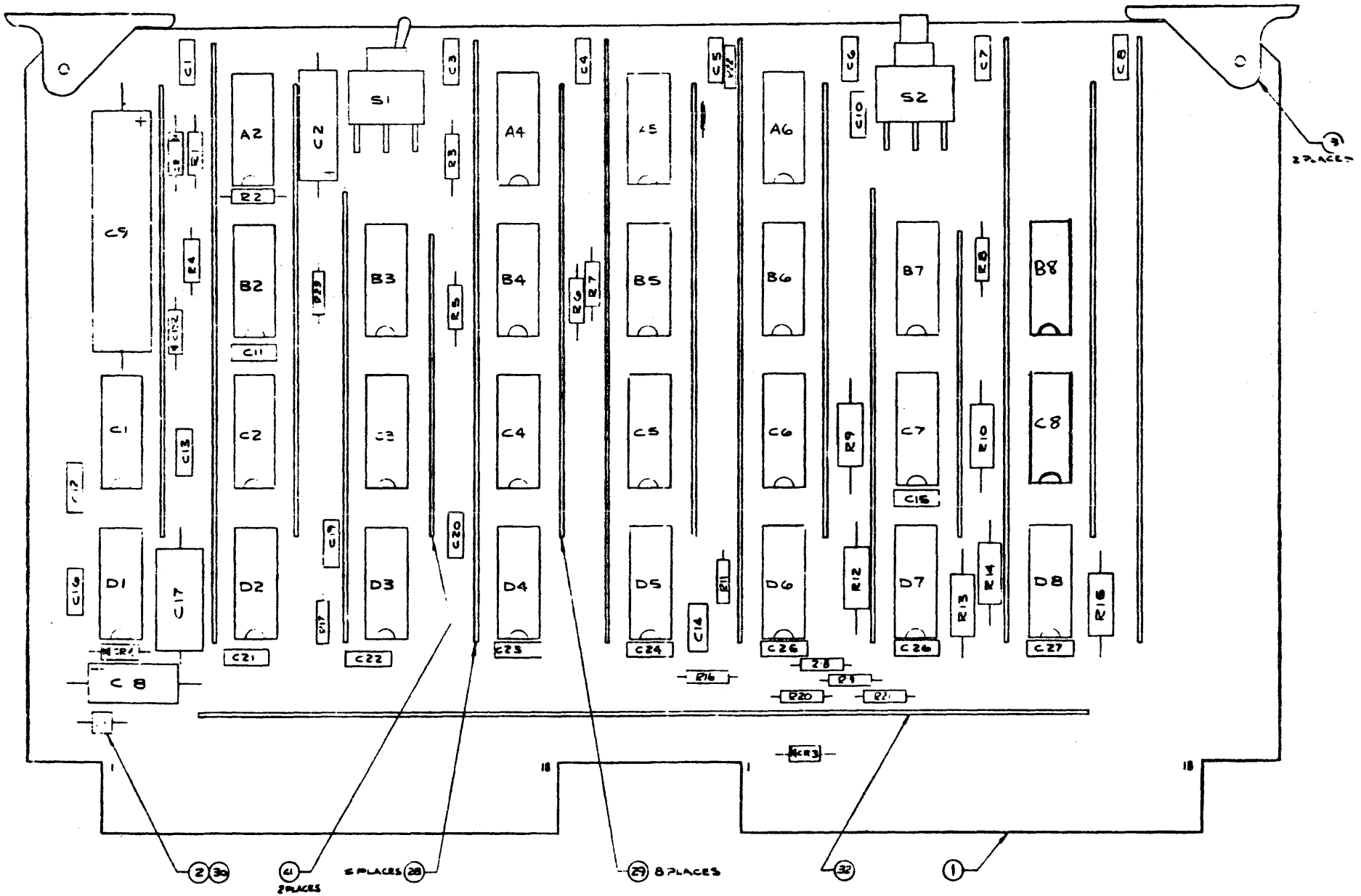


Figure A11. Error Card Assembly
(Dwg. No. 1040610)
<S 139A

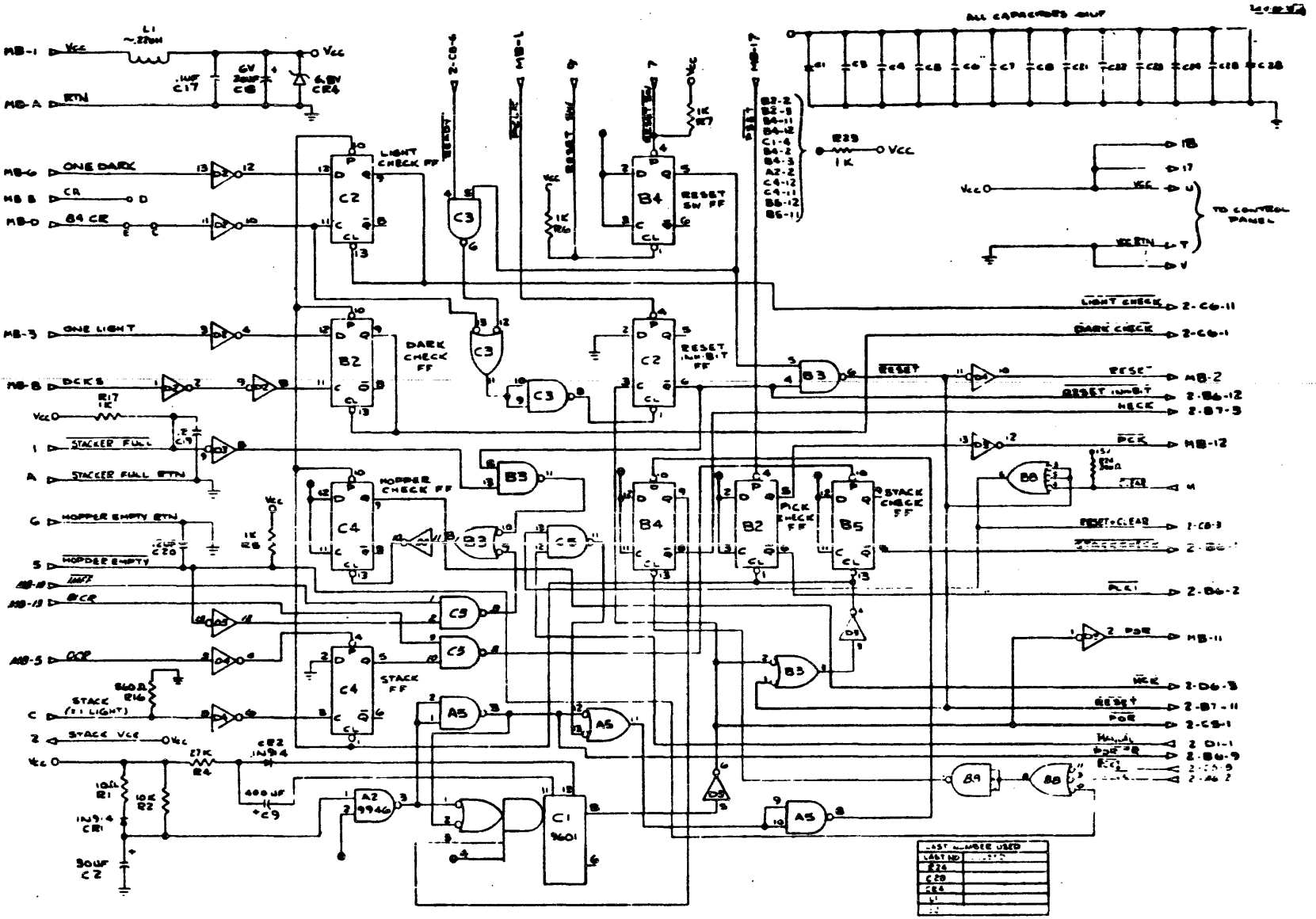


Figure A12. Schematic Diagram, Error Card (sheet 1 of 2)
(Dwg. No. 1041908)

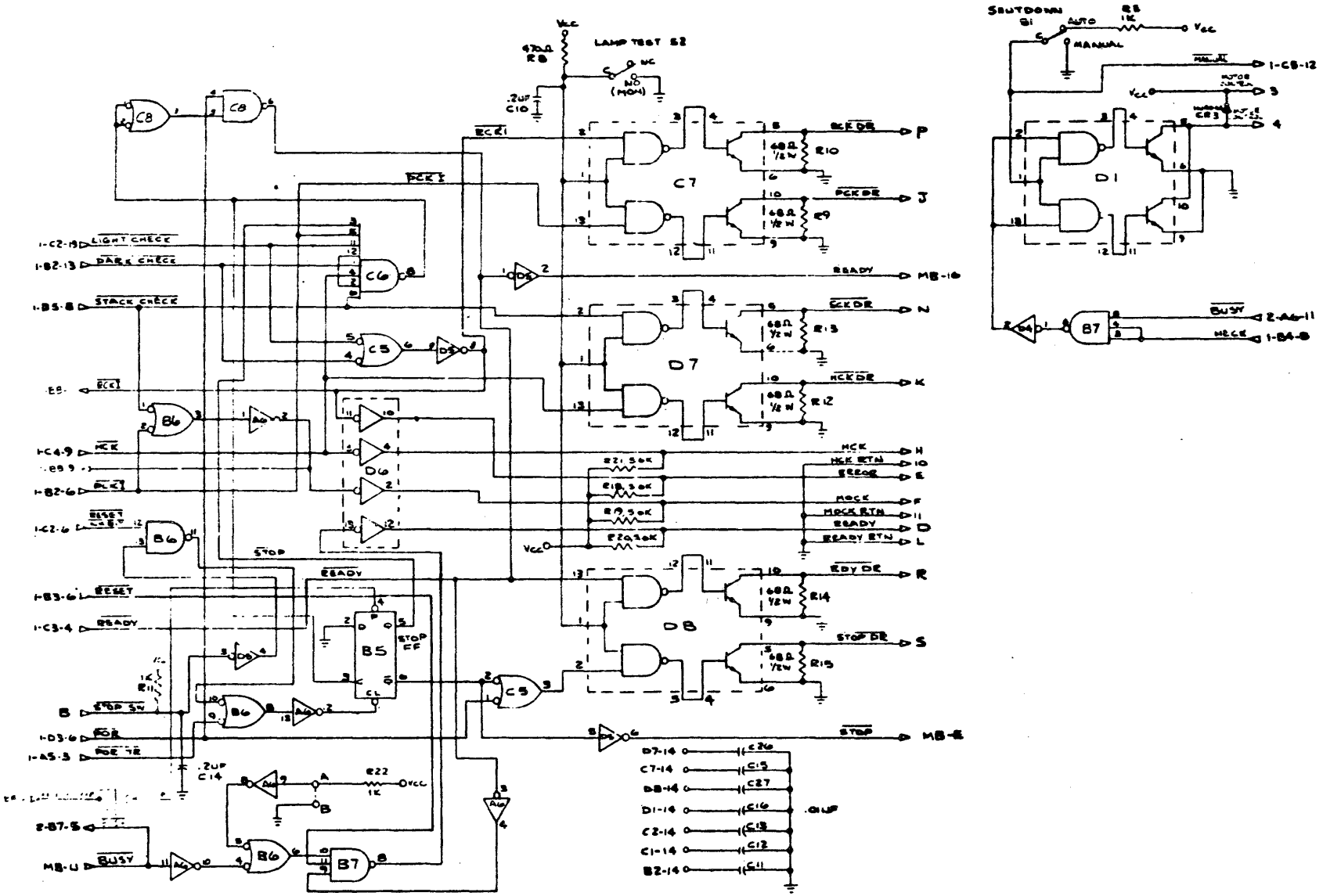


Figure A8. Schematic Diagram, Error Card (sheet 2 of 2)

SIGNAL MNEMONICS AND ABBREVIATIONS

MNEMONIC	DESCRIPTION	LOCATION	ORIGINATING SOURCE
Vcc	+5 volts	MB-1	5 volt power supply (Mother Board)
RTN	+5 volt return	MB-A	5 volt power supply (Mother Board)
TST	Timing Strobe	J3-T	Reluctance Pickup
TST RTN	Timing Strobe Return	J3-S	Reluctance Pickup
SHIELD	Shield for Timing Strobe	J3-R	Reluctance Pickup
TST1	Timing Strobe One	D9-9	Clock Card
ϕA	Clock Phase A	MB-S	Clock Card
C1	Basic Clock	MB-14	Clock Card
ϕB	Clock Phase B	MB-F	Clock Card
ϕC	Clock Phase C	MB-K	Clock Card
ϕD	Clock Phase D	MB-9	Clock Card
ONE DARK	Read Station Any Dark	MB-6	Control Card
POR	Power On Reset	MB-11	Error Card
PCR	Pick Control Reset	MB-C	Sync Card
ZERO	Preset Decode	MB-N	Sync Card
RESET	Gated Reset Switch	MB-2	Sync Card
STϕB	Column Strobe Phase B	MB-4	Sync Card
GPR	Good Pick Reset	MB-H	Clock Card
TST2	Timing Strobe Two	C8-9	Clock Card
TSTR	Timing Strobe Reset	MB-N	Clock Card
PRCLK	Preset Clock	MB-15	Clock Card
OSCLK	Offset Clock	MB-P	Clock Card
OSR	Offset Reset	MB-J	Clock Card
OSUCLK	Offset Up-Clock	MB-R	Clock Card
STϕC	Column Strobe Phase C	MB-V	Sync Card
STϕD	Column Strobe Phase D	MB-7	Sync Card
IMST	Index Mark Strobes	MB-T	Sync Card
IM	Index Marks	J3-A	Clock Card
IM RTN	Return for Index Marks	J3-B	Clock Card
SHIELD	Shield for Index Marks	J3-C	Clock Card
CR	Column Reset	MB-B	Clock Card
OCR	Zero Column Reset	MB-5	Clock Card

SIGNAL MNEMONICS AND ABBREVIATIONS
(Continued)

MNEMONIC	DESCRIPTION	LOCATION	ORIGINATING SOURCE
DCKS	Dark Check Strobes	MB-8	Clock Card
81CR	81st Column Reset	MB-13	Clock Card
84CR	84th Column Reset	MB-D	Clock Card
PICK COMMAND	Pick Command Input	J8-2	Control Card
PICK COMMAND RTN	Pick Command Input Return	J8-3	Control Card
STOP	Stop	MB-E	Error Card
READY	Ready	MB-16	Error Card
BUSY	Busy Output	J8-1	Control Card
PCLK	Pick Clock	MB-L	Control Card
Vcc	+5V to Read Sensor Array	J8-12	Control Card
Row 12	Read Sensor Input Row 12	J8-13	Control Card
Row 11	Read Sensor Input Row 11	J8-14	Control Card
Row 0	Read Sensor Input Row 0	J8-15	Control Card
Row 1	Read Sensor Input Row 1	J8-16	Control Card
Row 2	Read Sensor Input Row 2	J8-17	Control Card
Row 3	Read Sensor Input Row 3	J8-18	Control Card
Row 4	Read Sensor Input Row 4	J8-P	Control Card
Row 5	Read Sensor Input Row 5	J8-R	Control Card
Row 6	Read Sensor Input Row 6	J8-S	Control Card
Row 7	Read Sensor Input Row 7	J8-T	Control Card
Row 8	Read Sensor Input Row 8	J8-U	Control Card
Row 9	Read Sensor Input Row 9	J8-V	Control Card
ONE LIGHT	Read Station Any Light	MB-3	Control Card
D12	Data Row 12 Output	J8-L	Control Card
D11	Data Row 11 Output	J8-M	Control Card
D0	Data Row 0 Output	J8-K	Control Card
D1	Data Row 1 Output	J8-H	Control Card
D2	Data Row 2 Output	J8-J	Control Card
D3	Data Row 3 Output	J8-N	Control Card
D4	Data Row 4 Output	J8-F	Control Card
D5	Data Row 5 Output	J8-E	Control Card
RTN	Data Drivers Return	J8-5	Control Card
D6	Data Row 6 Output	J8-B	Control Card

SIGNAL MNEMONICS AND ABBREVIATIONS
(Continued)

MNEMONIC	DESCRIPTION	LOCATION	ORIGINATING SOURCE
D7	Data Row 7 Output	J8-D	Control Card
D8	Data Row 8 Output	J8-A	Control Card
D9	Data Row 9 Output	J8-C	Control Card
CSDS	Column Storage Data Strobe	MB-18	Sync Card
HOPPER FULL	Hopper Full Switch	J4-1	Error Card
HOPPER FULL RTN	Hopper Full Switch Return	J4-A	Error Card
HOPPER EMPTY RTN	Hopper Empty Switch Return	J4-6	Error Card
HOPPER EMPTY	Hopper Empty Switch	J4-5	Error Card
STACK	Stack Sensor Input	J4-C	Error Card
STACK Vcc	Stack Sensor +5 volts	J4-2	Error Card
RESET SW	Reset Switch Normally Open	J4-9	Error Card
$\overline{\text{RESET SW}}$	Reset Switch Normally Closed	J4-7	Error Card
PSET	Pick Check Set	MB-17	Sync Card
LIGHT CHECK	Light Check	C2-9	Error Card
DARK CHECK	Dark Check	B2-9	Error Card
HECK	Hopper Empty Check	B4-8	Error Card
PCK	Pick Check	B2-5	Error Card
STACK CHECK	Output Stacker Check	B5-8	Error Card
PCKI	Pick Check Indicator	B2-2	Error Card
HCK	Input or Output Hopper Check	C4-9	Error Card
SHUTDOWN STATUS	Mode Switch Input	S1-C	Error Card
POR TR	Power on Reset Trigger	A5-12	Error Card
STOP SW	Stop Switch Input	J4-B	Error Card
RCK DR	Read Check Lamp Driver	J4-P	Error Card
PCK DR	Pick Check Lamp Driver	J4-P	Error Card
SCK DR	Stack Check Lamp Driver	J4-N	Error Card
HCK DR	Hopper Check Lamp Driver	J4-K	Error Card
HCK	Hopper Check Output	J4-H	Error Card
HCK RTN	Hopper Check Output Return	J4-10	Error Card
ERROR	Error Output	J4-E	Error Card
ERROR RTN	Error Output Return	J4-M	Error Card
MOCK	Motion Check Output	J4-F	Error Card

SIGNAL MNEMONICS AND ABBREVIATIONS
(Continued)

MNEMONIC	DESCRIPTION	LOCATION	ORIGINATING SOURCE
MOCK RTN	Motion Check Output Return	J4-11	Error Card
READY	Ready Output	J4-D	Error Card
READY RTN	Ready Output Return	J4-L	Error Card
RDY DR	Ready Lamp Driver	J4-R	Error Card
STOP DR	Stop Lamp Driver	J4-S	Error Card
PICK	Pick Driver Output	J5-A	Sync Card
PICK RTN	Pick Driver Output Return	J5-B	Sync Card
SHIELD	Shield for PICK	J5-C	Sync Card
BUSY	Busy Signal	MB-U	Control Card

DWG NO

REVISIONS

SYM	DESCRIPTION	APPROVED	DATE
X	PRE PRODUCTION RELEASE		
A	PRODUCTION RELEASE PER EN 5586.		5/25/71
B	REVISED PER EN # 80281		
C	REVISED PER EN # 80792		
D	REVISED PER EN # 82394		

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Development

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CHK	
DSGN	2/2/71
ENGR	2/22/71
APPD	2/21/71
APPD	4/23/71

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TITLE

SOFTWARE PERFORMANCE SPECIFICATION
620 CARD READER TEST

CODE IDENT NO.	SIZE	DWG NO.	REV
21101	A	89A0180	D

SCALE

SHEET 1 OF 51

TABLE OF CONTENTS

SECTION 1: TEST PROGRAM OVERVIEW

1.1 INTRODUCTION

The 620 Card Reader Test determines whether or not the card reader is functioning correctly in conjunction with the 620 computer. Card reader models 620-22, 620-25 and 620-28 can be thus tested.

The 620 Card Reader Test operates with the 620 Test Executive and thus uses standard teletype I/O routines and is equipped with both a Console Mode and a Teletype Mode (see Document 98A99520[illegible]).

1.2 PROGRAM DESIGN OVERVIEW

1.2.1

An optional initialization check is provided to test the initialization command (EXC 030 for card reader device address 030). This command is currently implemented only on the models 620-25 and 620-28.

The program will attempt to read one card using the user indicated I/O mode; if reader ready comes on and no error is detected, each of the 80 characters will be stored in memory. If reader ready does not come on or a mechanical error is sensed or recognized by a time-out, the program will report it to the user and halt.

1.2.2

Each commumn is tested for preset bit configuration and if the data is correct, the next card is read. If the data is incorrect, the error count is incremented and if SS2 is set, the program will halt with the error information in the registers. If SS2 is not set, the next column will be tested.

1.2.3

Each column of each card is thus tested. If SS3 is set at any time or if the hopper becomes empty, the total data error count will be provided to the user and a halt will be executed. Otherwise the program will continue to run

until a reader ready condition does not come on and/or an error condition is sensed.

1.2.4

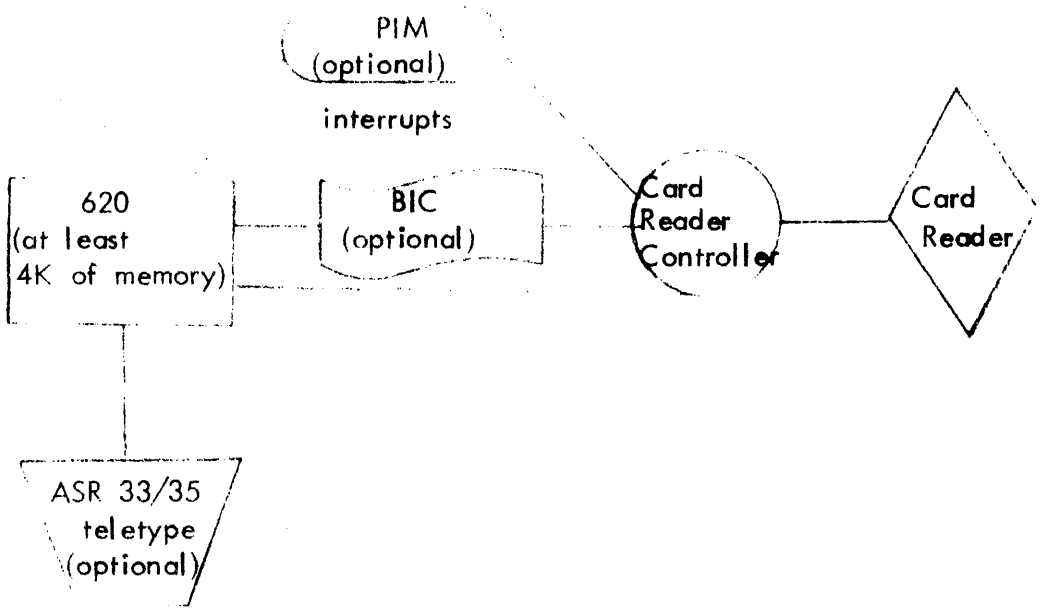
The user may determine whether I/O is to be performed under sense, PIM, or BIC control by providing the appropriate parameter.

1.3 HARDWARE SUMMARY

The following hardware items are required or are optional to use this program:

1. A 620 series computer with at least 4K of memory.
2. A Model 620-22, 620-25, or 620-28 Card Reader.
3. (Optional) A model ASR33 or ASR35 teletype.
4. (Optional) BIC.
5. (Optional) PIM.

A hardware diagram is given below:



2.1 GENERAL

The external specification provides all the operating procedures and information pertinent to user interface.

2.2 LOADING PROCEDURE

The 620 Card Reader Test is available as an object tape or as an object card deck.

2.2.1

If the object tape is used, the user must secure a copy of the 620 Test Executive object tape (part number 92U0107-001, SPS 89A0122). The device used to load the tapes can be the ASR33 or ASR35 teletype paper tape reader or the high speed paper tape reader. The 620 Test Executive is loaded first and executed to set the Console/ Teletype Mode flag (see 2.3) according to the user's entry point. The 620 Card Reader Test object tape is then loaded, either by executing an 'L .' from the 620 Test Executive (if a teletype is being used), or by loading it from the console.

2.2.2

If the object card deck is used, the user must enter the card reader bootstrap given below. The card deck provided (part number 92J0101060A) contains the card binary loader, 620 Card Reader Test, and 620 Test Executive in that order. This deck is placed in the read hopper of the card reader and the card reader readied. The A, B, X and Instruction registers are then cleared; the P register set to 0131; and 'SYSTEM RESET' then hit 'RUN' on the 620 console. When the 'READY' light comes on, on the card reader, the cards will begin to load (there may be some warm-up time before 'READY' comes on).

A successful load is designated by a halt at 06177 in the 620 Test Executive. From there the user picks the entry point to the 620 Test Executive (SPS 89A0122) to set the Console/Teletype Mode flag and hits 'RUN'. The actual 620 Card Reader Test is started at 0500, after the Console/Teletype Mode flag has been set.

2.2.3 CARD OBJECT BOOTSTRAP LOADER*

Location	Coding	Symbolic Program		
000114	102530	BOOR	CIA	030
000115	004250		LRLA	8
000116	101130		SEN	0130, BOOS
000117	000122			
000120	001000		JMP	*-2
000121	000116			
000122	102130	BOOS	INA	030
000123	055000		STA	0,1
000124	005144		IXR	
000125	001000		JMP	BOOU
000126	000131			
000127	000000	BOOT	DATA	PLD
000130	100230		EXC	0230
000131	101130	BOOU	SEN	0130, BOOR
000132	000114			
000133	101630		SEN*	0630, BOOT
000134	100127			
000135	001000		JMP	*-4
000136	000131			

* The assumed device address is 030. To change for a different device address, change the last two octal digits of each I/O command to the desired device address.

2.3 OPERATING PROCEDURE

After loading the 620 Test Executive, and the 620 Card Reader Test, and setting the Console/Teletype Mode flag by entry point to the 620 Test Executive (SPS 89A0122), the user sets the program counter to 0500 and resets SS3. The two procedures for Console and for Teletype Mode are given next.

2.3.1 SENSE SWITCH SETTINGS

Switch	'Set'	'Reset'
1	Not used	
2	Halt on data error	On data error, count it and continue
3	Wind-up test and prepare for a new one	Continue with test

2.3.2 TELETYPE MODE

After starting the program at 0500 the teletype prints:

620 CARD READER TEST
OPTIONS?

The user responds with a 'Y' or an 'N' for 'yes' or 'no', respectively (no period or comma is input). If no options are requested, the parameters remain unchanged and the initialization test is performed (see below). If options are requested the following message is output:

CARD READER DA=

The user then responds with the octal device address of the card reader and a period or comma.

INITIALIZATION TEST PERFORMED?

The user responds with a 'Y' or an''N' for 'yes' or 'no', respectively (no period or comma is input). If 'Y' is input the following is typed:
EMPTY HOPPER OF CARD READER AND THEN RESTORE CARDS
The program then halts at IR=1* to allow the user to comply with this request. The user then hits 'RUN'.

The program then senses for a reader ready condition. If the reader is ready when sensed, indicating a malfunction of the reader ready sense line, the following is printed:

READER READY SENSED

* IR is the Instruction Register

The rest of the parameters are then input (or if no options were specified, the test trys to read a card).

If 'READER READY' is not sensed the program executes a card reader initialize command (currently implemented only on the model 620-25 and 620-28 card reader). A wait occurs to allow the reader to be mechanically initialized by this command. The reader ready sense is then executed again. If the reader is not ready, the following message is printed and a halt occurs at IR = 2.

INITIALIZATION ERROR

Hit 'SYSTEM RESET' and 'RUN' to continue with the test. If the reader is ready, the initialization was satisfactorily performed. In either case, if options were not specified, the program attempts to read a card using the sense mode, if options were specified, the program prints:

I/O MODE=

The user then types BIC, SEN, or PIM* (no period or comma is input). If he types neither, the program types 'INVALID' and again waits for BIC, SEN, or PIM.

If he types SEN or PIM, the following message is skipped; otherwise the teletype types:

BIC DA=

The user must then type the octal device address of the BIC followed by a period or comma.

If he types BIC or SEN the following messages are skipped; otherwise the teletype types:

PIM DA=
TRAP LOCATION=
INTERRUPT MASK=

The user must type the corresponding octal values followed by a period or a comma after each '=' (reference following table for interrupt mask).

Interrupt Line	Most Common Trap Location	Interrupt Mask
0	0100	0376
1	0102	0375
2	0104	0373

* While inputting BIC, SEN, or PIM, the user may delete the previous character input with a ' ←— '.

Interrupt Line	Most Common Trap Location	Interrupt Mask
3	0106	0367
4	0110	0357
5	0112	0337
6	0114	0277
7	0116	0177

If the 'READY' condition does not come true on the card reader, the program will type 'READER NOT READY' and subsequently halt at IR = 3 unless SS3 is set, in which case the summary message will be typed. If no reader error is detected, each of the 80 characters will be stored in memory. If a card reader error is sensed and the hopper is not empty, the program will type the following:

CARD READER ERROR

This will be followed by a halt at IR = 4.

If a card reader error is sensed and the hopper is empty, the following message will be typed followed by the summary message.

HOPPER EMPTY

Other abnormal conditions which would prevent the reading of a card are also typed when appropriate. The messages are generally self explanatory and are given below together with the subsequent halt location:

Message	Halt
CHARACTER READY TIME-OUT	IR = 5
BIC BUSY (prior to initialization of BIC)	IR = 6
BIC ABNORMAL STOR	IR = 7
INTERRUPT TIME-OUT	IR = 010
BIC BUSY TIME OUT (after initialization of BIC)	IR = 011

After any such error, it is only necessary to hit 'SYSTEM RESET' and then 'RUN' to resume the attempt to read a card.

Each column is tested for a preset bit configuration, and if the data is correct, the next card is read. If any data is incorrect, the error count is incremented and if SS2 is set, the program will halt at IR = 0100, with the X, B, and A - registers containing the

column, the expected value, and the actual value, respectively. Hit 'RUN' to continue.

Each column of each card is thus tested. If SS3 is set at any time during the read operation or if a 'hopper empty' is sensed, the program types the following:

END OF TEST, NUMBER OF CARDS READ IS XXXXXX

TOTAL NUMBER OF ERRORS IS YYYYYY

where XXXXXX and YYYYYY are 6-digit octal numbers.

The test then prints 'OPTIONS?' to restart the given sequence. The following messages may be printed as detected:

CARD IN READ STATION STATUS	IR = 012
PREMATURE END OF CARD STATUS	IR = 013

2.3.3 CONSOLE MODE

After starting the program at 0500, the program halts at IR0201.

The user then enters a '1' in the A-register and hits 'RUN' if he wishes to input parameter options. Otherwise he just hits "RUN". If no options are to be input, the parameters remain unchanged, sense mode will be used, and the initialization test is begun (see below).

If options are to be input, the test halts at IR=0202. The default values here are 030 for the card reader device address and a '1' to indicate that the initialization test is to be performed. If the user is not satisfied with these values, he must key-in the card reader device address in the A-register and/or a '0' in the B-register to indicate that the initialization test is not to be performed. If no initialization is to be performed, the initialization section is skipped.

If initialization is to be performed, the test halts at IR=0203. The user then empties the card reader hopper and subsequently restores the cards to the card reader hopper to induce a hopper empty and a reader not ready condition. The user then hits 'RUN'. The sense reader ready is then executed, and if it is true an error halt occurs at IR=0204. The user may then hit 'RUN' to continue after the initialization section of the test.

If the reader is not sensed as ready, an initialization command is executed and a wait executed in order to allow the initialization command to be mechanically effected. A sense reader ready is then executed. This time if the result is 'TRUE' no message is printed, and the test proceeds.

If the result of this sense reader ready is 'FALSE', an error halt occurs at IR = 0205. The user may continue with the test by hitting 'SYSTEM RESET' followed by 'RUN'.

If the 'options' alternative was not specified, the test trys to read a card using the sense mode. If the 'options' alternative was specified, the test halts at IR = 0206.

The user then enters the I/O mode in the A-register ('0' for sense, '1' for BIC, and '-1' for PIM); and, if appropriate, the BIC device address in the B-register. The default values are A-register = 0, B-register = 020. 'RUN' is then hit.

If the PIM is specified, the program halts at IR=0207 and the user must enter the PIM device address in the A-register, the trap location in the B-register, and the interrupt mask in the X-register. The default values are A = 040, B = 0100, X = 0376; see the following table to obtain the interrupt mask:

Interrupt Line	Most Common Trap Location	Interrupt Mask
0	0100	0376
1	0102	0375
2	0104	0373
3	0106	0367
4	0110	0357
5	0112	0337
6	0114	0277
7	0116	0177

If the 'READY' condition comes on, on the card reader, the program will read one card; otherwise, the program will halt at IR = 3. If no error is detected, each of the 80 characters will be stored in memory. If a card reader error is sensed and the hopper is not empty, the program will halt at IR = 4.

If a card reader error is sensed and the hopper is empty, the test will halt at the IR=0210 summary location (see below). Other abnormal conditions which would prevent the reading of a card also produce halts when appropriate. They are:

Halt	Explanation
IR = 5	No character ready after sufficient interval
IR = 6	BIC busy prior to BIC initialization
IR = 7	BIC abnormal stop

Halt	Explanation
IR = 010	No character ready interrupt after sufficient interval
IR = 011	BIC busy time-out after initialization of BIC

After any such error, it is only necessary to hit 'SYSTEM RESET' and then 'RUN' to resume the attempt to read a card.

Each column is tested for a preset bit configuration and if the data is correct, the next card is read. If the data is incorrect, the error count is incremented and if SS2 is set, the program will halt at IR = 0100 with the X, B, and A-registers containing the column, the expected value, and the actual value, respectively. Hit 'RUN' to continue.

Each column of each card is thus tested. If SS3 is set at any time during the read operation of if a 'hopper empty' is sensed, the program will halt at IR = 0210 with the following information in the registers:

A register = data error count
B register = number of cards read

The following halts may be executed as detected:

IR = 012	Card in read station status
IR = 013	Premature end of card status
IR = 014	Reader ready while reading

2.4 OUTPUT STATEMENTS

620 CARD READER TEST
CARD READER DA =
I/O MODE
BIC DA =
PIM DA =
TRAP LOCATION =
INTERRUPT MASK =
INVALID
CHARACTER READY TIME-OUT
CARD READER ERROR
END OF TEST, NUMBER OF CARDS READ IS XXXXXX,*
TOTAL NUMBER OF ERRORS IS XXXXXX,*
BIC ABNORMAL STOP
READER NOT READY
BIC BUSY
PERFORM INITIALIZATION TEST?
EMPTY HOPPER OF CARD READER AND THEN RESTORE CARDS
DO NOT MAKE READER READY
HOPPER EMPTY
READER READY SENSED
IT SHOULD NOT HAVE BEEN

* Octal numbers

INITIALIZATION ERROR
OPTIONS ?
INTERRUPT TIME-OUT
BIC BUSY TIME-OUT
CARD IN READ STATION STATUS
PREMATURE END OF CARD STATUS
READER READY WHILE READING

2.5 INPUT STATEMENTS

The following output statements require that the user input octal numbers followed by a period or comma:

CARD READER DA =
PIM DA =
BIC DA =
TRAP LOCATION =
INTERRUPT MASK =

The following output statements require that the user input 'Y' for 'yes' or 'N' for 'no'.

OPTIONS ?
PERFORM INITIALIZATION TEST?

The following output statement requires that the user input 'BIC', 'SEN', or 'PIM'.

I/O MODE =

2.6 HALT TABLE

Instruction Register	Significance
1	User removes cards from reader and then replaces them (initialization test-Teletype mode). Hit 'RUN' to continue.
2	Initialization error (Teletype Mode). Hit 'SYSTEM RESET' and 'RUN' to continue.
0201	Set: A = 1 to input options. If no options wanted, leave A = 0. (Console Mode). Hit 'RUN' to continue.
0202	Set: A = card reader device address, B = '0' for no initialization test, and '1' for initialization test;

Instruction Register	Significance
	or leave defaults A = 030, B = 1 (Console Mode). Hit 'RUN' to continue.
0203	User removes cards from reader and then replaces them (initialization test-Console Mode). Hit 'RUN' to continue.
0204	Reader ready sensed before initialization error (Console Mode). Hit 'RUN' to continue.
0205	Initialization error (Console Mode). Hit 'SYSTEM RESET' and 'RUN' to continue.
0206	Set: A = '0' for sense mode, '1' for BIC mode, '-1' for PIM mode; and B = BIC device address, if appropriate. Default values are A =0, B=020 (Console Mode). Hit 'RUN' to continue.
0207	Set: A = PIM device address, B = trap location, X = interrupt mask. Default values are A = 040, B = 0100, X = 0376 (Console Mode). Hit 'RUN' to continue.
0100	Data error (SS2 set). X = column B = expected data A = actual data Hit 'RUN' to continue.
7	BIC abnormal stop. Hit 'SYSTEM RESET' and 'RUN' to continue.
5	Character ready time-out. Hit 'SYSTEM RESET' and 'RUN' to continue.
010	Interrupt time-out (PIM mode). Hit 'SYSTEM RESET' and 'RUN' to continue.
011	BIC busy time-out after initialization of BIC (BIC Mode). Hit 'SYSTEM RESET' and 'RUN' to continue.
3	Reader not ready. Hit 'SYSTEM RESET' and 'RUN' to continue.

Instruction Register	Significance
6	BIC busy prior to initialization. Hit 'SYSTEM RESET' and 'RUN' to continue.
4	Card reader error. Hit 'SYSTEM RESET' and 'RUN' to continue.
0210	Test summary (Console Mode). A = number of data errors B = number of cards read

3.1 COMPONENT SPECIFICATIONS

The mainline section of coding performs all the functions of the 620 Card Reader Test except inputting a card. The actual teletype communication subroutines referenced in the mainline section, however, are actually in the 620 Test Executive. These subroutines are OUTD, OUTG, INPD, INPE, and INPG.

There are three card reader I/O routines - one which utilizes sense control only, one which utilizes the BIC, and one which utilizes the PIM. The routine utilized is determined by the user.

3.2 MEMORY MAP

Location	Contents
500-2070	Mainline section
2071-2266	Card Reader Driver (Sense Control)
2267-2433	Card Reader Driver (PIM Control)
2424-2571	Card Reader Driver (BIC control)
2572-2620	Device Address Setter
2620-3341	Teletype Messages
0-01 040-043 0400-0477 05100-07777	620 Maintain II Test Executive and Loaders

3.3 I/O COMMANDS TESTED

3.3.1 Card Reader (assumed device address = 030)

Command	Meaning
SEN 0630	Reader ready?
SEN 0330	Hopper empty?
SEN 0230	Reader error?
SEN 0130	Character ready?
EXC 030	Initialize Card Reader (implemented only on 620-25 and 620-28)
EXC 0230	Feed a card
CIA 030	Input Character Buffer
SEN 030	Card in Read Station

3.3.2 PIM (assumed device address = 040)

Command	Meaning
EXC 0540	Clear and disable PIM
EXC 0240	Enable PIM
OAR 040	Output PIM interrupt mask

3.3.3 BIC (assumed device addresses = 020 and 021)

Command	Meaning
EXC 020	Activate BIC
EXC 021	Initialize BIC
SEN 020	BIC busy?
SEN 021	BIC abnormal stop?
OAR 020	Output to BIC initial address register
OAR 021	Output to BIC final address register

3.4 COMPONENT DESCRIPTIONS AND FLOWCHARTS

Title: Mainline Program (not a closed subroutine)

Symbolic Name: START

Purpose: To input user parameters; optionally, perform initialization test; check card input data; and communicate error conditions.

Description: There are two modes: Teletype and Console. In Teletype mode, the Options parameter, Initialization Test parameter, card reader device address, I/O mode, BIC device address (if appropriate) and PIM device address, trap location, and interrupt mask (if appropriate) are input from the teletype. The cards are then input and checked until a data error occurs (with SS2 set), or a card reader problem occurs, or the user sets SS3. All messages, except data error, are output to the teletype. The Console mode is the same but register entry and display are used instead of the teletype.

Entry Points: START

Calling Sequence: N.A.

Entrance Parameters: N.A.

Exit Point: The program is a continous loop. Any halt followed by a 'RUN' on the 620 console will restart or continue it.

Exit Parameters: N.A.

Tables or Files Modified or Read: N.A.

Tables or Files Created: The card data input buffer, IBUF, is used for data input.

Called by: N.A.

Called from: CDRD, PMRD, and BCRD - the Card Reader Drivers; DVAD - the Device Address Setter; and 620 Executive I/O routines.

Exception Conditions: See 2.3.2 and 2.3.3.

Timing: 900 cards per minute for 620-22, and 300 cards per minute for 620-25, 620-28.

Size: 01371 words, including data blocks.

Comments: This program is designed to be run in conjunction with the 620 Test Executive and uses flags and I/O routines residing in that program. Console mode is set by starting the 620 Test Executive at 06152; Teletype mode is set by starting it at 07000.

Special Notation: N.A.

Hardware Details: A Model 620-22, 620-25, or 620-28 card reader is required. Also: SEN 0630 and, optionally, EXC 030*.

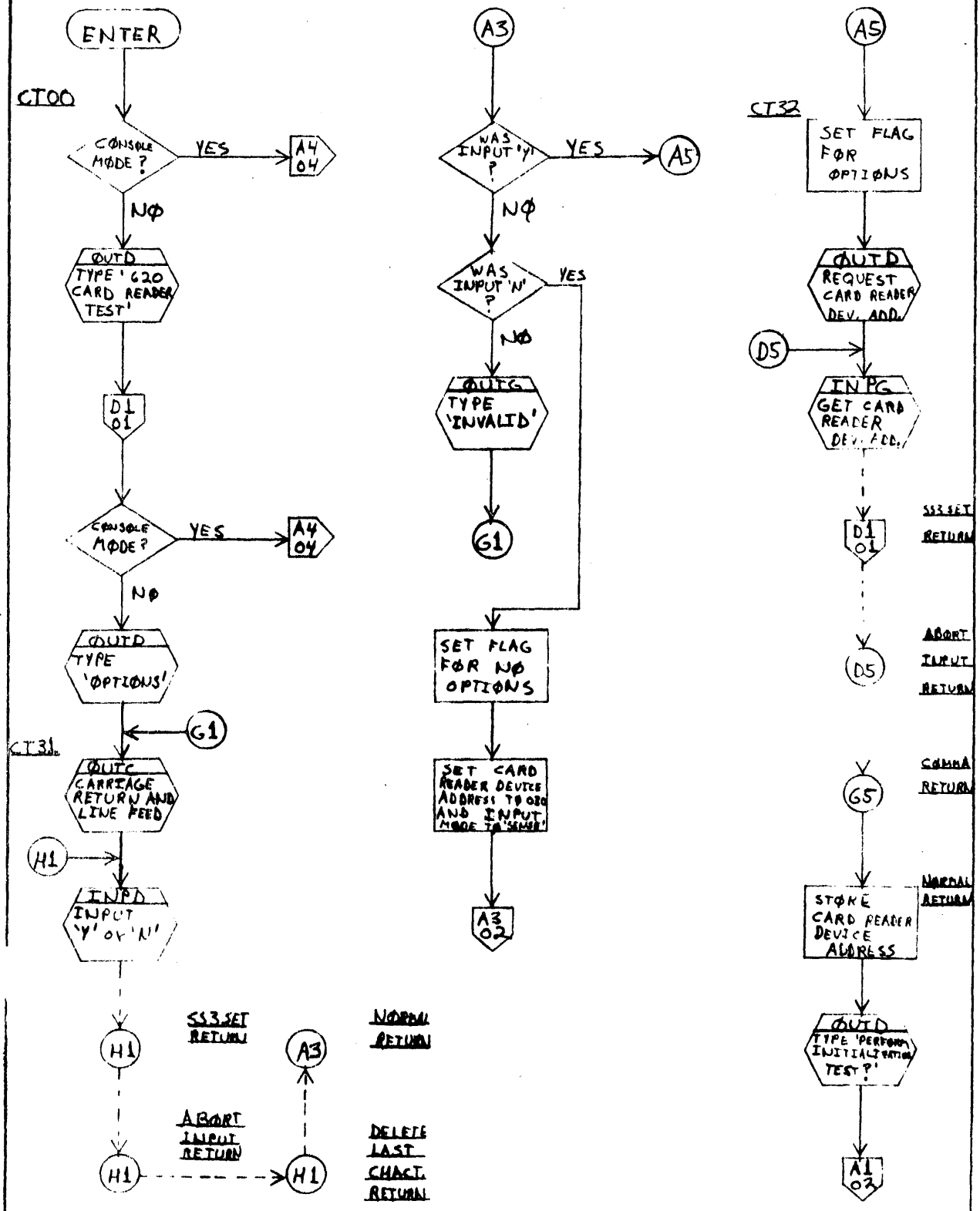
Flowcharts: See following sheets.

* A device address of 030 is assumed for the card reader.

Flowchart Worksheet

PROGRAMMER: Purcell	PROGRAM NO.:	DATE	PAGE 1
CHART I.D.	CHART NAME	PROGRAM NAME	

START



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varian data machines, a varian subsidiary	CODE IDENT. NO.	89A0180	REV D
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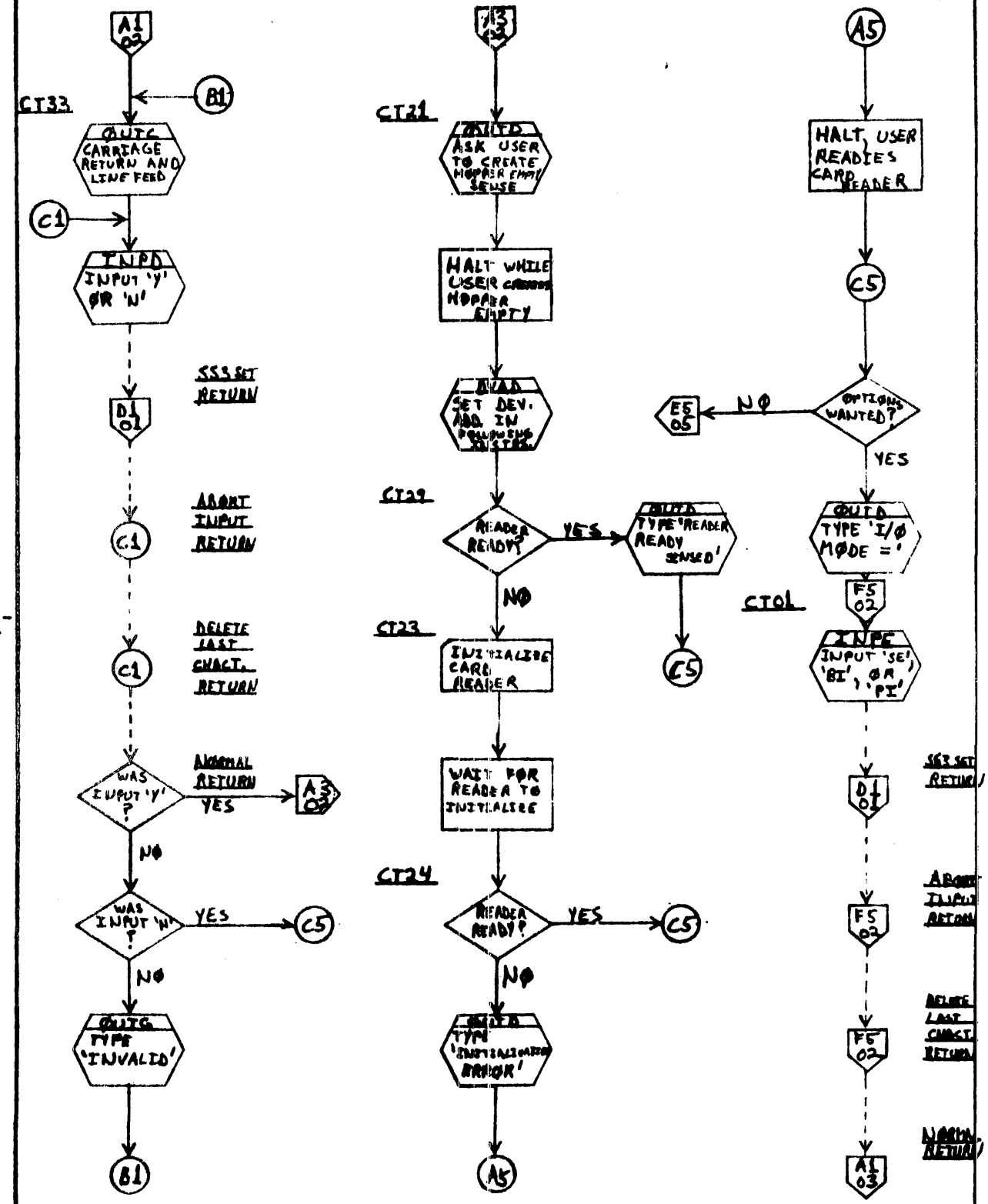
Flowchart Worksheet

PROGRAMMER:	PROGRAM NO.:	DATE	PAGE 2
CHART I.D.	CHART NAME	PROGRAM NAME	



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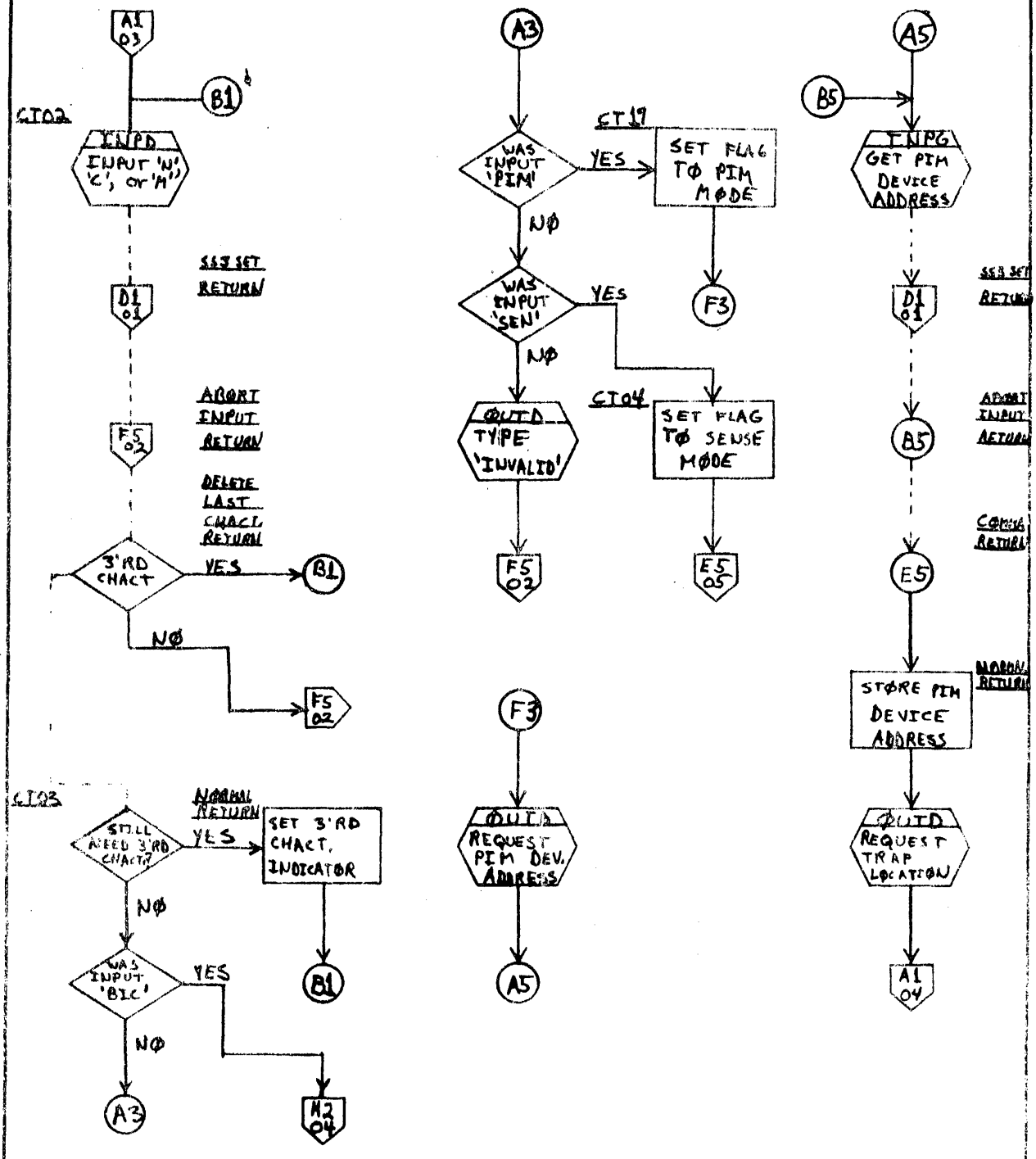
	PREPARED BY	APPROVED BY	SHEET 22 OF 51	

Flowchart Worksheet

PROGRAMMER:	PROGRAM NO.:	DATE	PAGE 3
CHART I. D.	CHART NAME	PROGRAM NAME	



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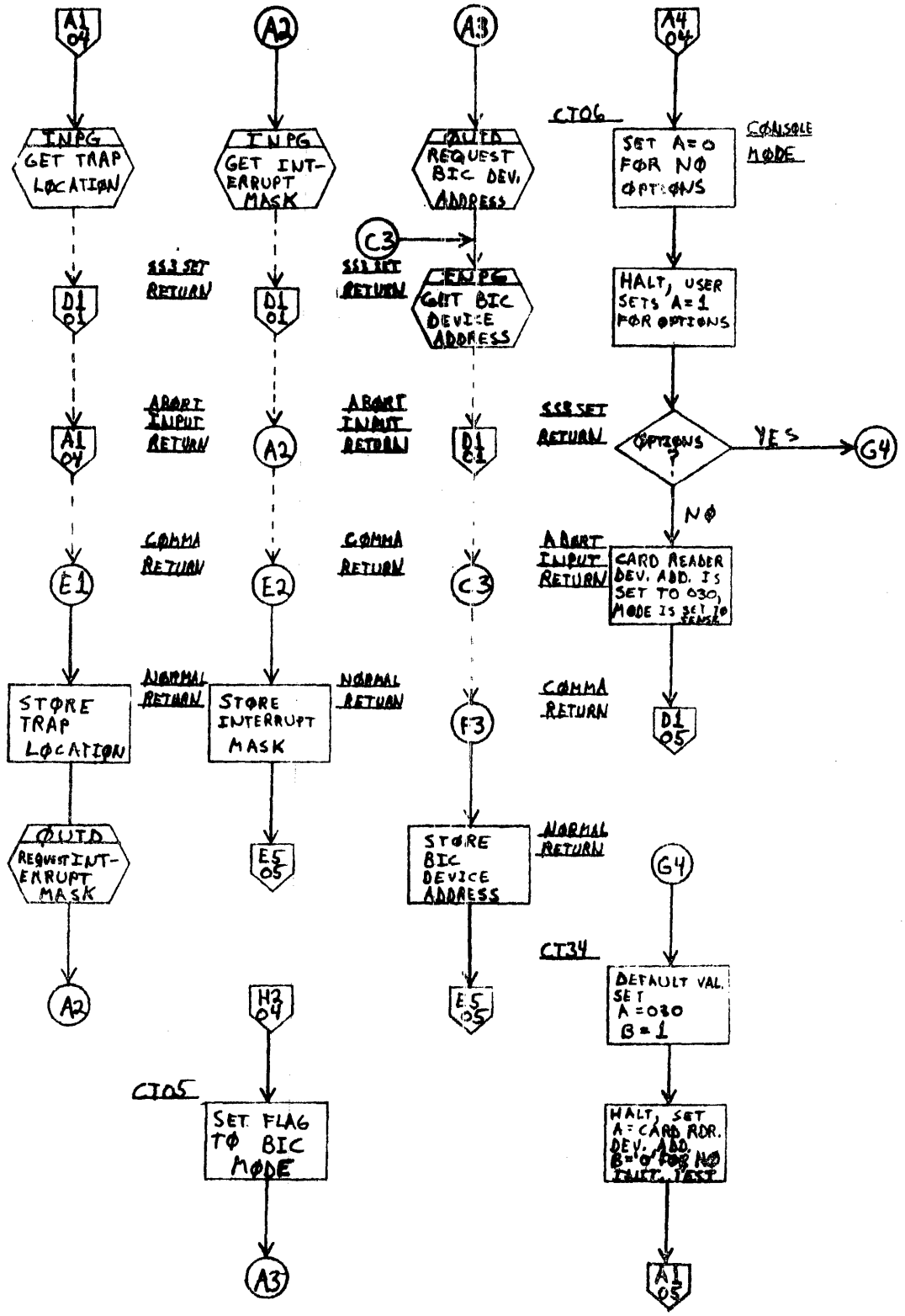
Flowchart Worksheet

PROGRAMMER:	PROGRAM NO.:	DATE	PAGE 4
CHART I.D.	CHART NAME	PROGRAM NAME	



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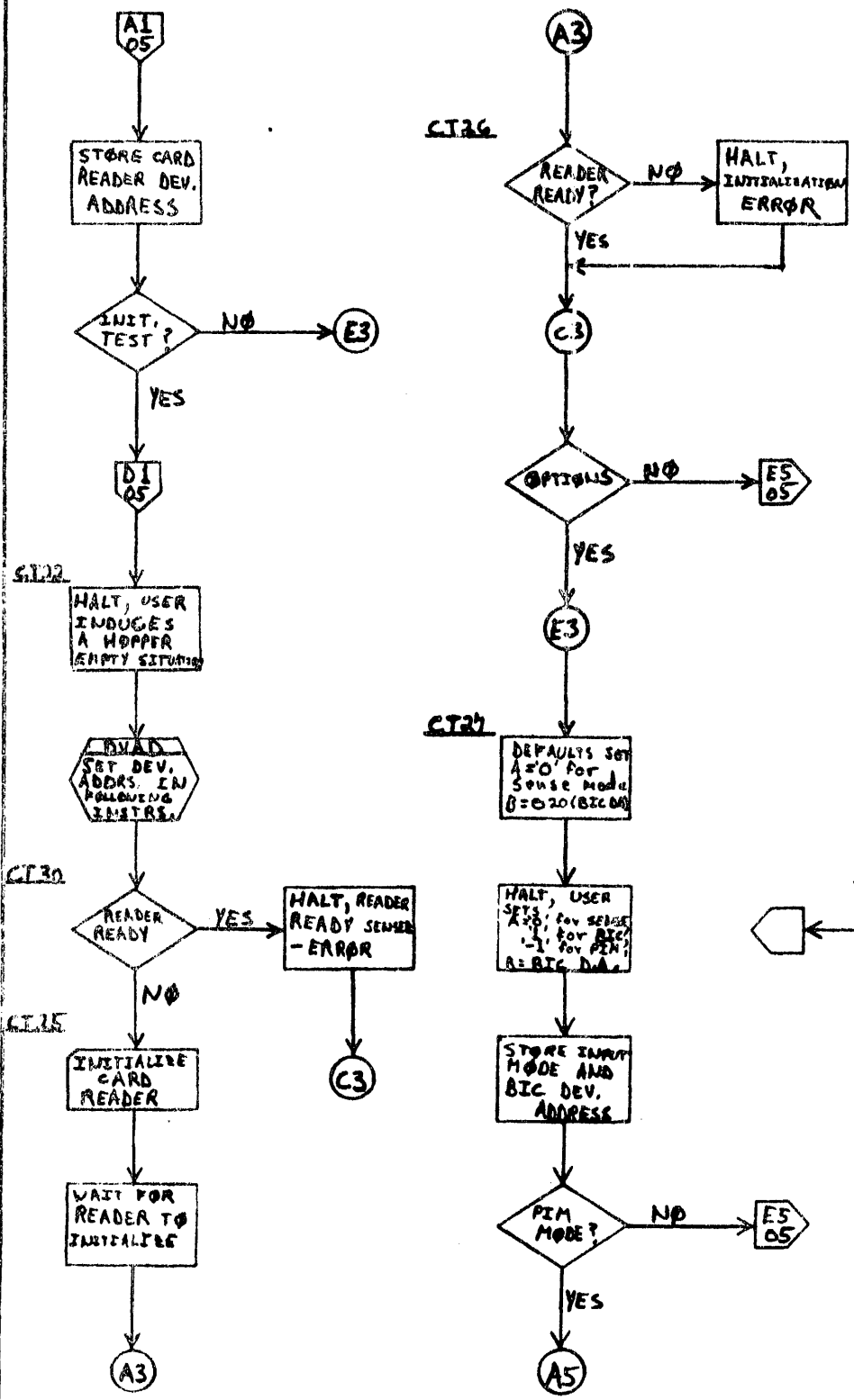
00A9240-000A

Flowchart Worksheet

PROGRAMMER:	PROGRAM NO.:	DATE	PAGE 5
CHART I.D.	CHART NAME	PROGRAM NAME	



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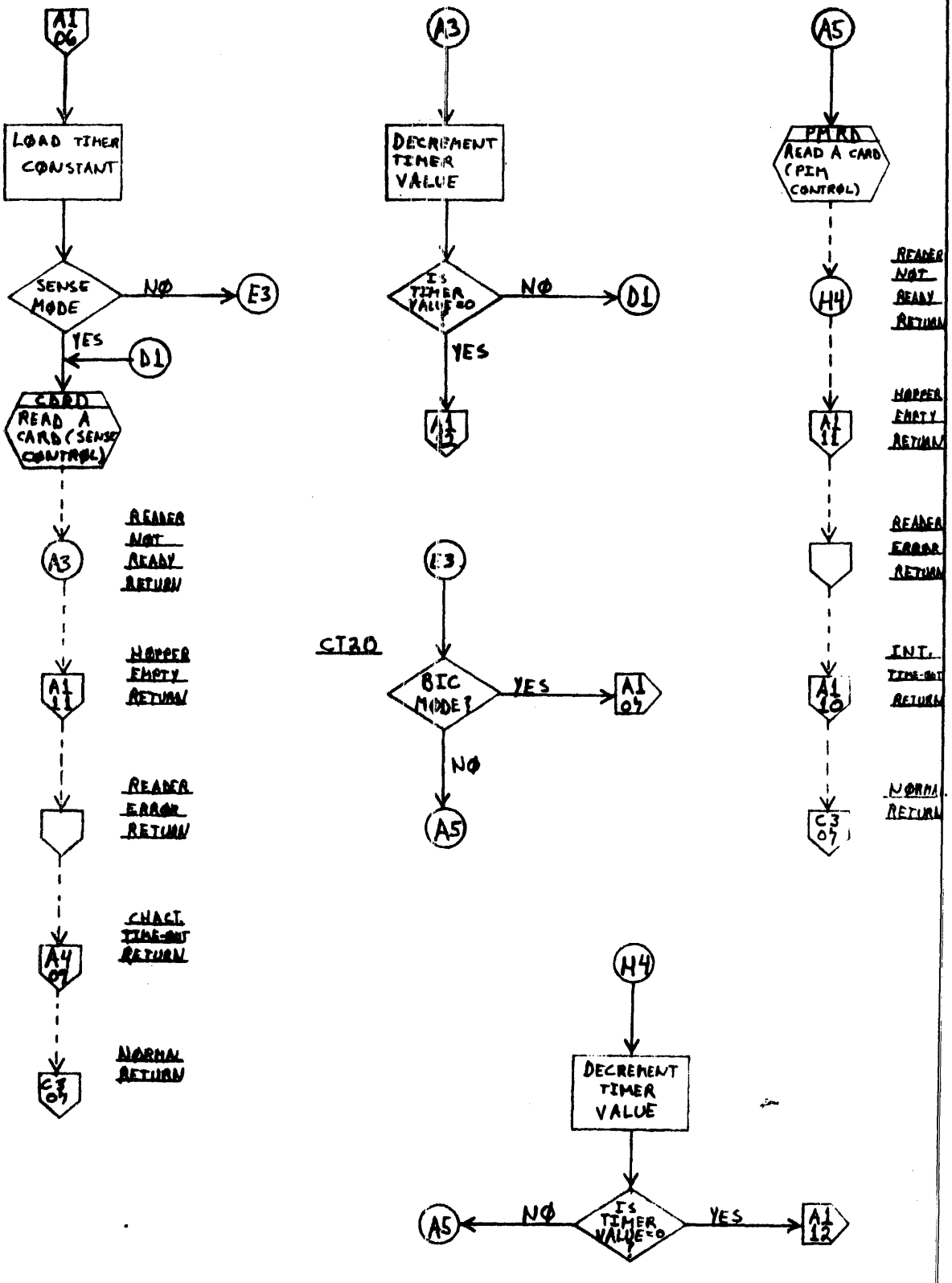
Flowchart Worksheet

PROGRAMMER:	PROGRAM NO.:	DATE	PAGE 6
CHART I.D.	CHART NAME	PROGRAM NAME	



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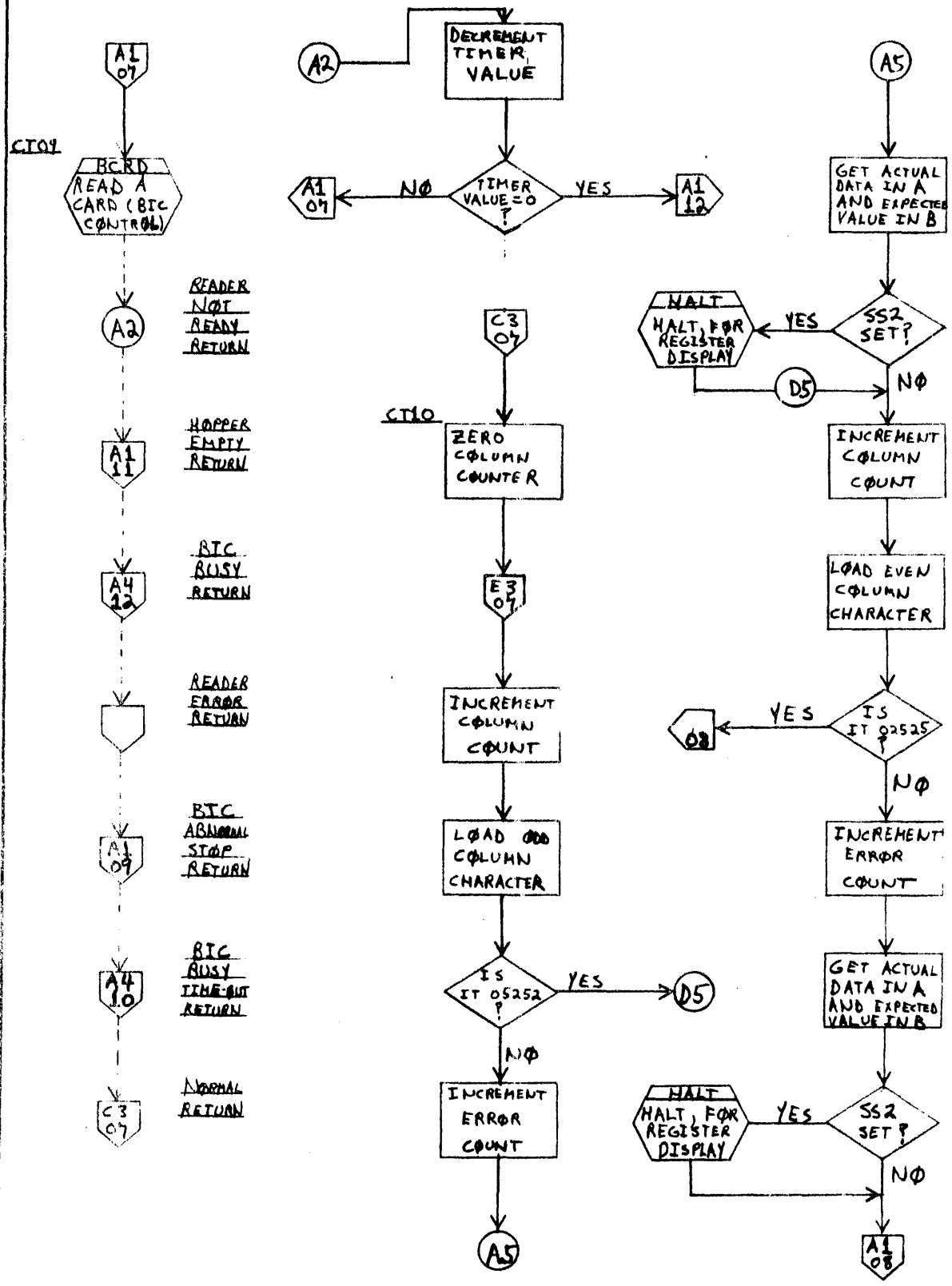
Flowchart Worksheet

PROGRAMMER:	PROGRAM NO.:	DATE	PAGE 7
CHART I.D.	CHART NAME	PROGRAM NAME	



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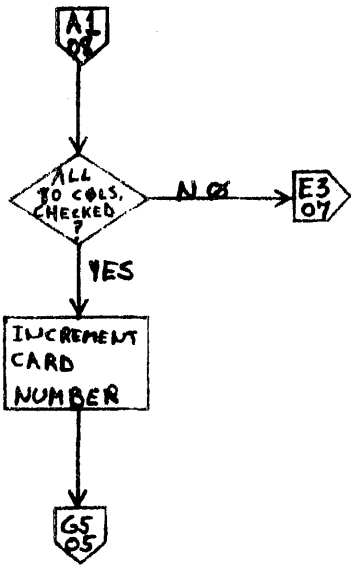
Flowchart Worksheet

PROGRAMMER:	PROGRAM NO.:	DATE	PAGE 8
CHART I.D.	CHART NAME	PROGRAM NAME	



HALT

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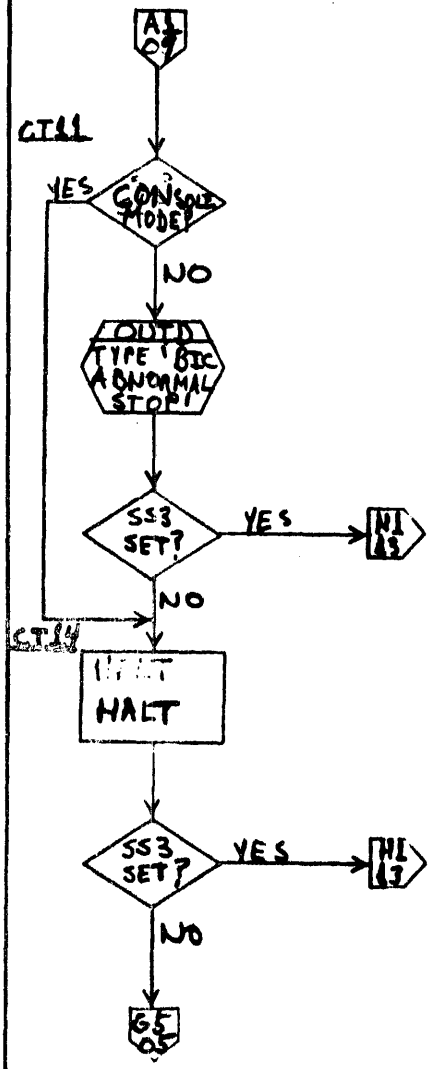

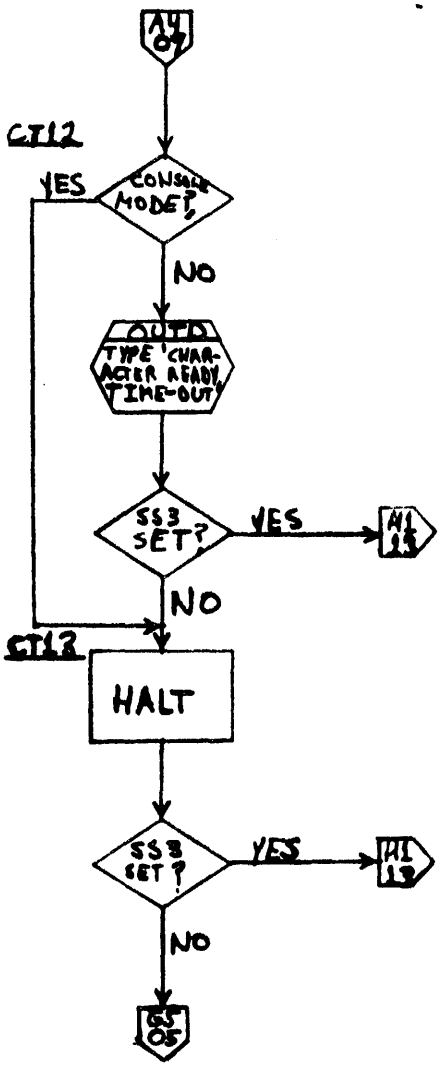

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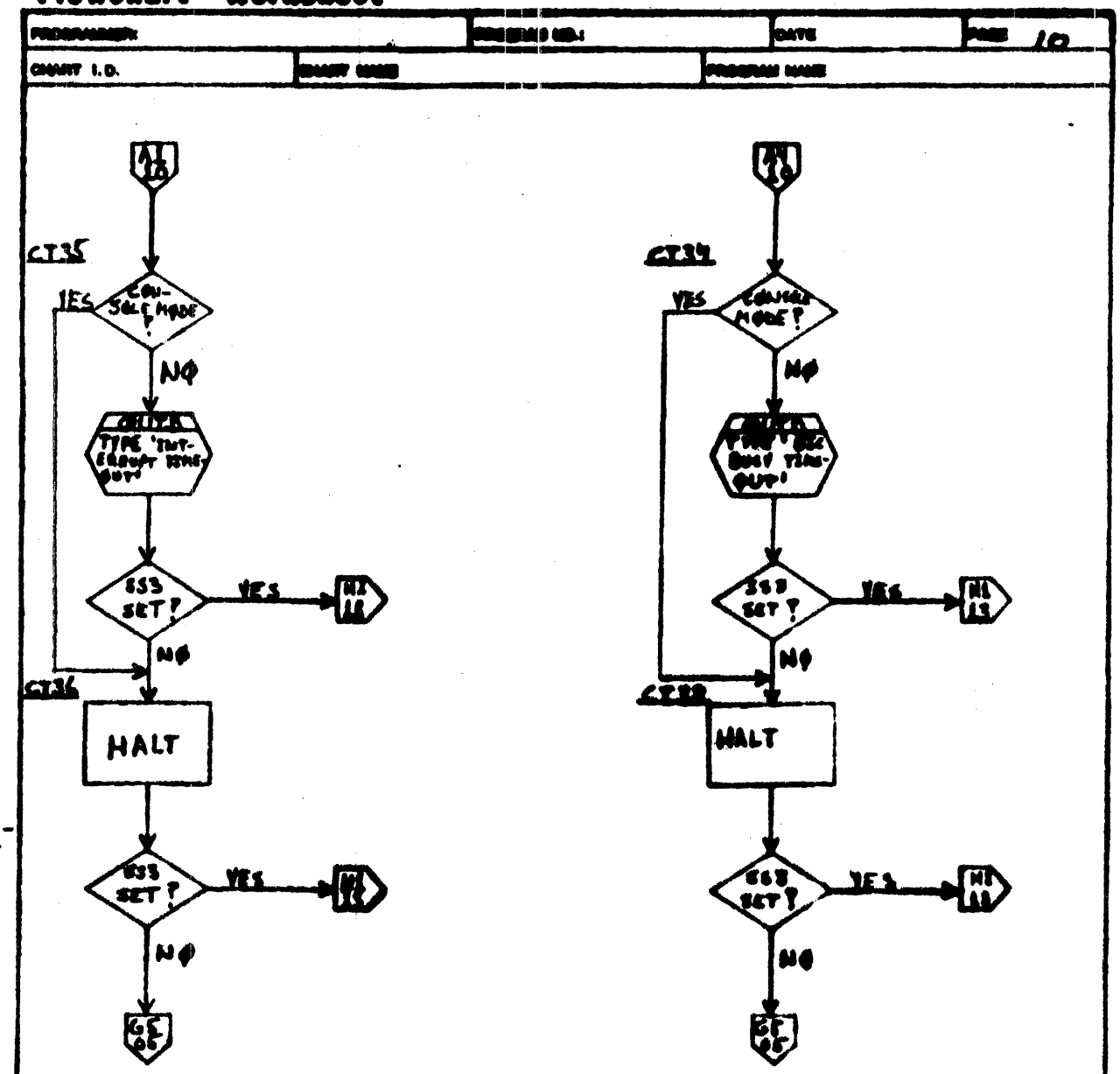
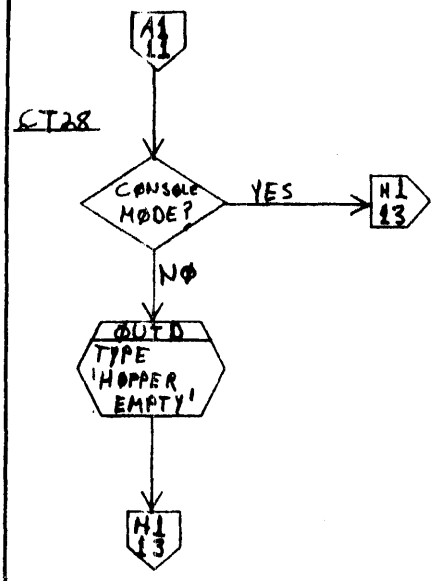
Flowchart Worksheet





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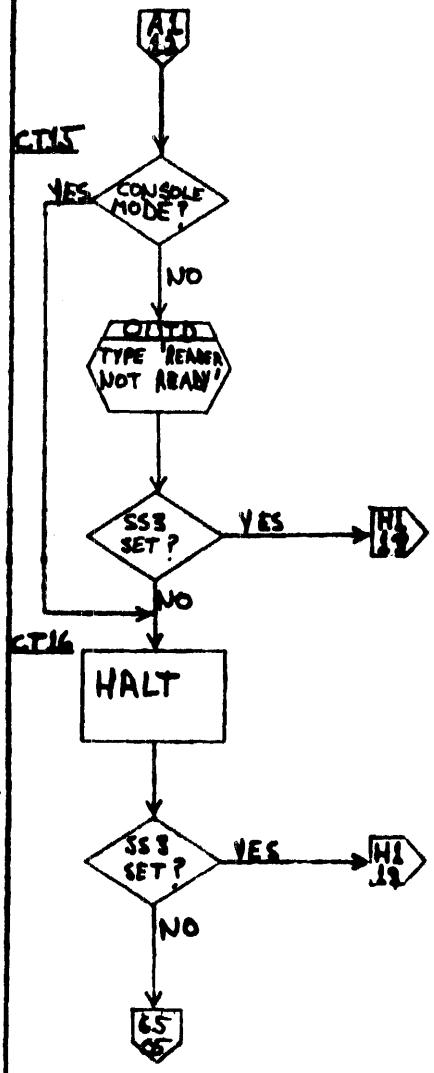

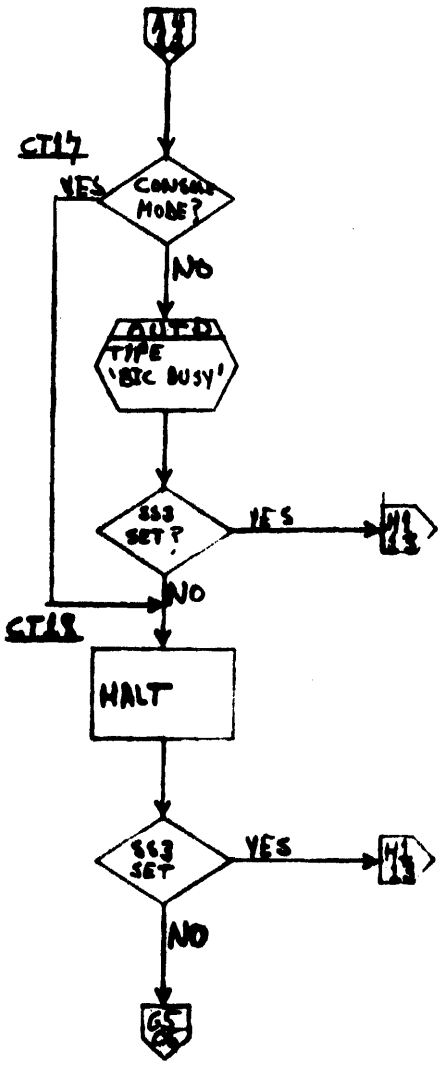

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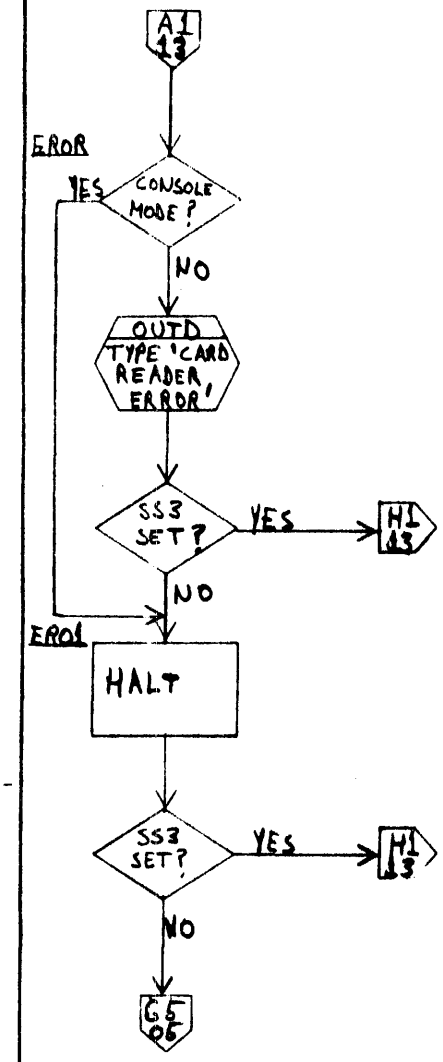
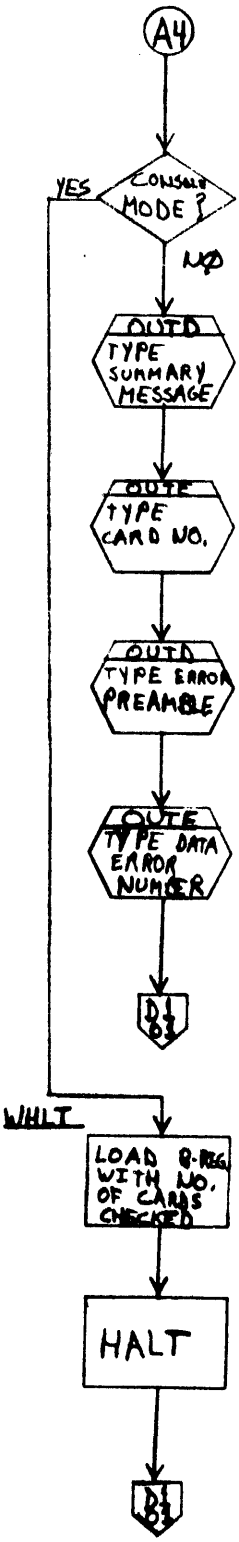
PROGRAMMER	PROGRAM NO.	DATE	PAGE 13
CHART I. D.	CHART NAME	PROGRAM NAME	





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Title: DEVICE ADDRESS SETTER

Symbolic Name: DVAD

Purpose: To set the device addresses of I/O instructions referred to in the calling sequence, according to the parameter specified in the calling sequence.

Description: The device address to be used is gotten from the calling sequence. Each instruction is fetched from the calling sequence pointers, altered, and stored back. When all the specified addresses are altered, the program returns.

Entry Points: The only entry point is DVAD.

Calling Sequence: CALL DVAD, (Device address); ---a sequence of addresses of instructions to be altered---; (a zero); return location.

Entrance Parameters: The device address is specified in the first data word after the call to DVAD. The subsequent data words are all addresses of instructions to be altered. The final data word is a zero.

Exit Point: The subroutine will exit right after the zero following the instruction address-list explained in Entrance Parameters.

Exit Parameters: N.A.

Table of Files Modified or Read: Each specified instruction has its last 6 bits set to the given device address.

Table or Files Created: N.A.

Called By: START - Mainline section; and CDRD, PMRD, and BCRD - the Card Reader Drivers.

Called From: N.A.

Exception Conditions: N.A.

Timing: About 22 cycles per instruction altered + 13 cycles.

Size: 027 words.

Comments: N.A.

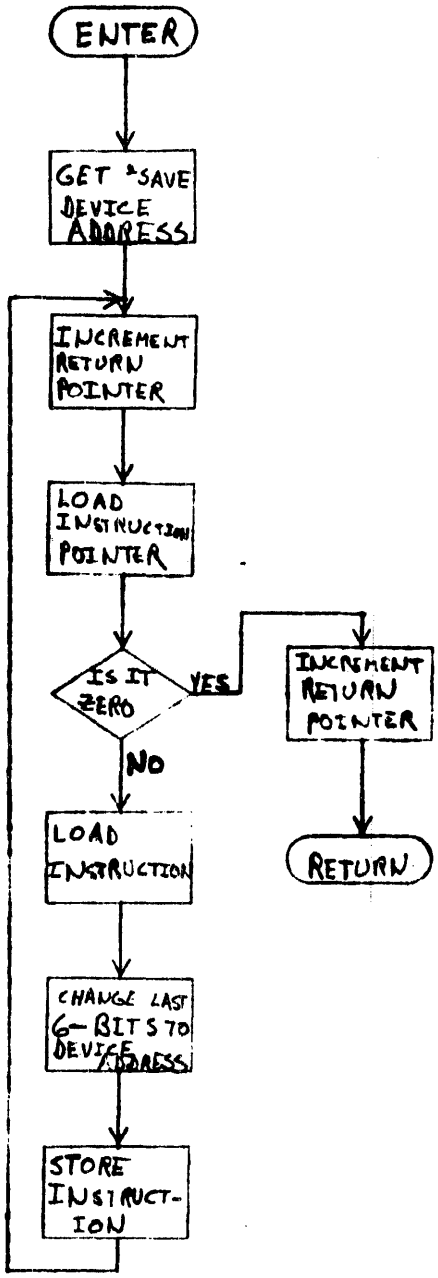
Special Notation: N.A.

Hardware Details: N.A.

Flowcharts: See following sheet.

PROGRAMMER	PROGRAM NO.	DATE	PAGE 1
CHART I.D.	CHART NAME	PROGRAM NAME	

DVAD



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84A0810-000A

Title: CARD READER DRIVER (SENSE CONTROL)

Symbolic Name: CDRD

Purpose: To input and store 80 columns of data from 1 card using sense control.

Description: The B and X registers are preserved, and the card reader device address is set in all I/O instructions by calling DVAD. A reader ready sense is performed, and if the sense response is true, a card is fed, and each character is input and stored in the buffer given in the calling sequence when sense character ready comes true. If the reader is not ready originally, if there is a reader error sensed during character input wait, or if character ready is not sensed true, and or hopper empty is sensed, an appropriate exit is taken. Otherwise, the normal exit is taken.

Entry Points: The only entry point is at CDRD.

Calling Sequence: CALL CDRD; (Buffer Address)[1 word]; (Reader Not Ready Return)[2 words]; (Hopper Empty Return)[2 words]; (Reader Error Return)[2 words]; (Character Ready Time-out Return)[2 words]; (Normal Return).

Entrance Parameters: The buffer address is specified in the first data word after the call to CDRD. No registers need be set for entry.

Exit Point: The exit points are given in the calling sequence and, with the exception of the normal return, must contain JMP instructions to the appropriate processing area.

Exit Parameters: The B and X registers are restored at exit time.

Table or Files Modified or Read: 80 characters are stored in the given buffer, IBUF, starting from the buffer beginning.

Tables or Files Created: N.A.

Called By: Mainline program (START)

Called From: Device Address Setter (DVAD)

Exception Conditions: **The device address of the card reader must be stored in $CRD before entry.**

Timing: **900 cards per minute for 620-22, and 300 cards per minute for** 620-25, 620-28

Size: 0176

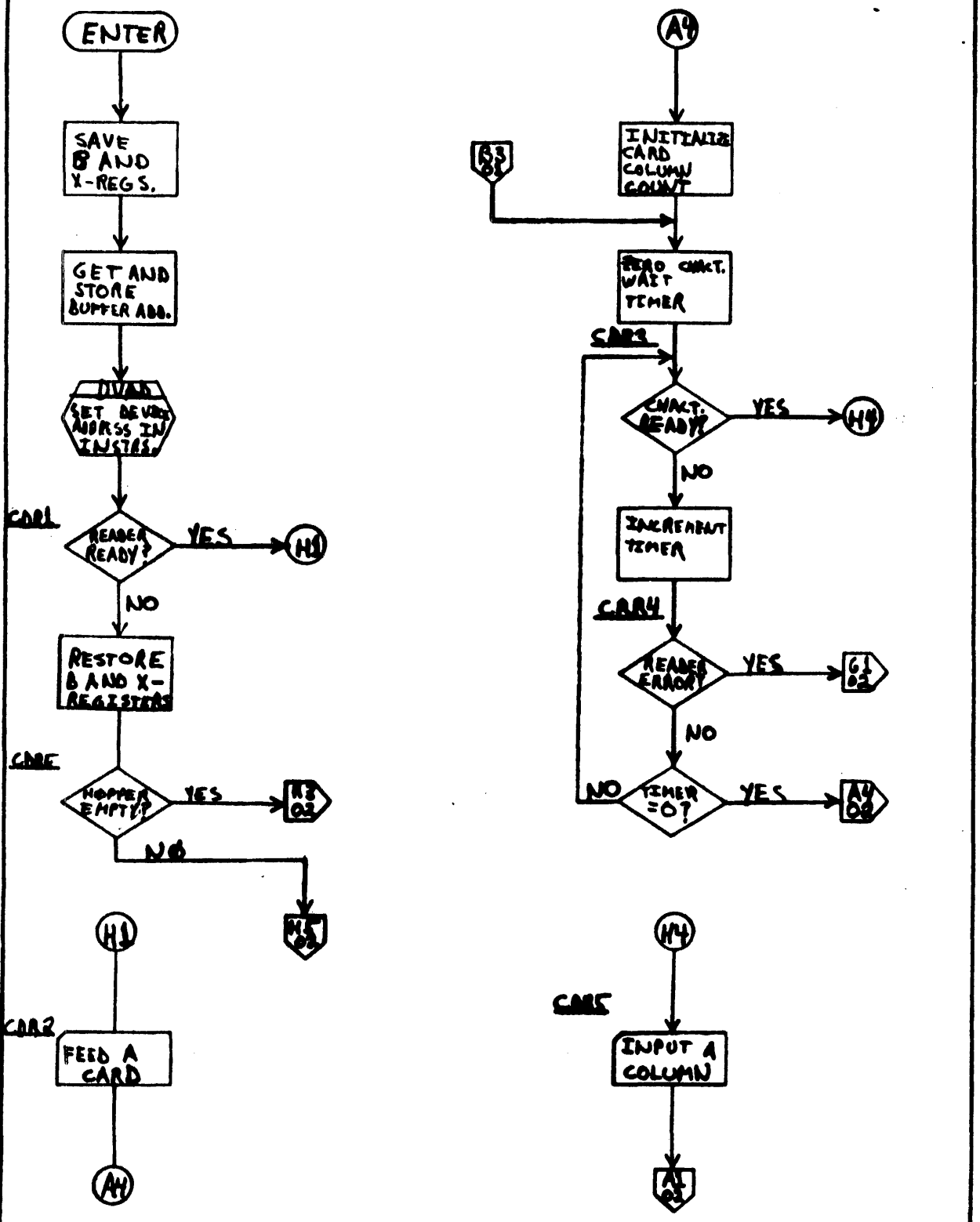
Comments: The user must set $CRD to the card reader device address before calling CDRD. The return points must also contain jumps to the appropriate processors.

Special Notation: **N.A.**

Hardware Details: SEN 0630, SEN 30, SEN 0330, EXC 0230, SEN 0130, SEN 0230 CIA 030 (a device address of 30 assumed).

Flowcharts: **See following sheets.**

PROGRAMMER Purcell	PROGRAM NO.	DATE	PAGE 1
CHART I.D.	CHART NAME	PROGRAM NAME	



varian data machines, a varian subsidiary	DOC. IDENT. NO.	89A0180	REV. D
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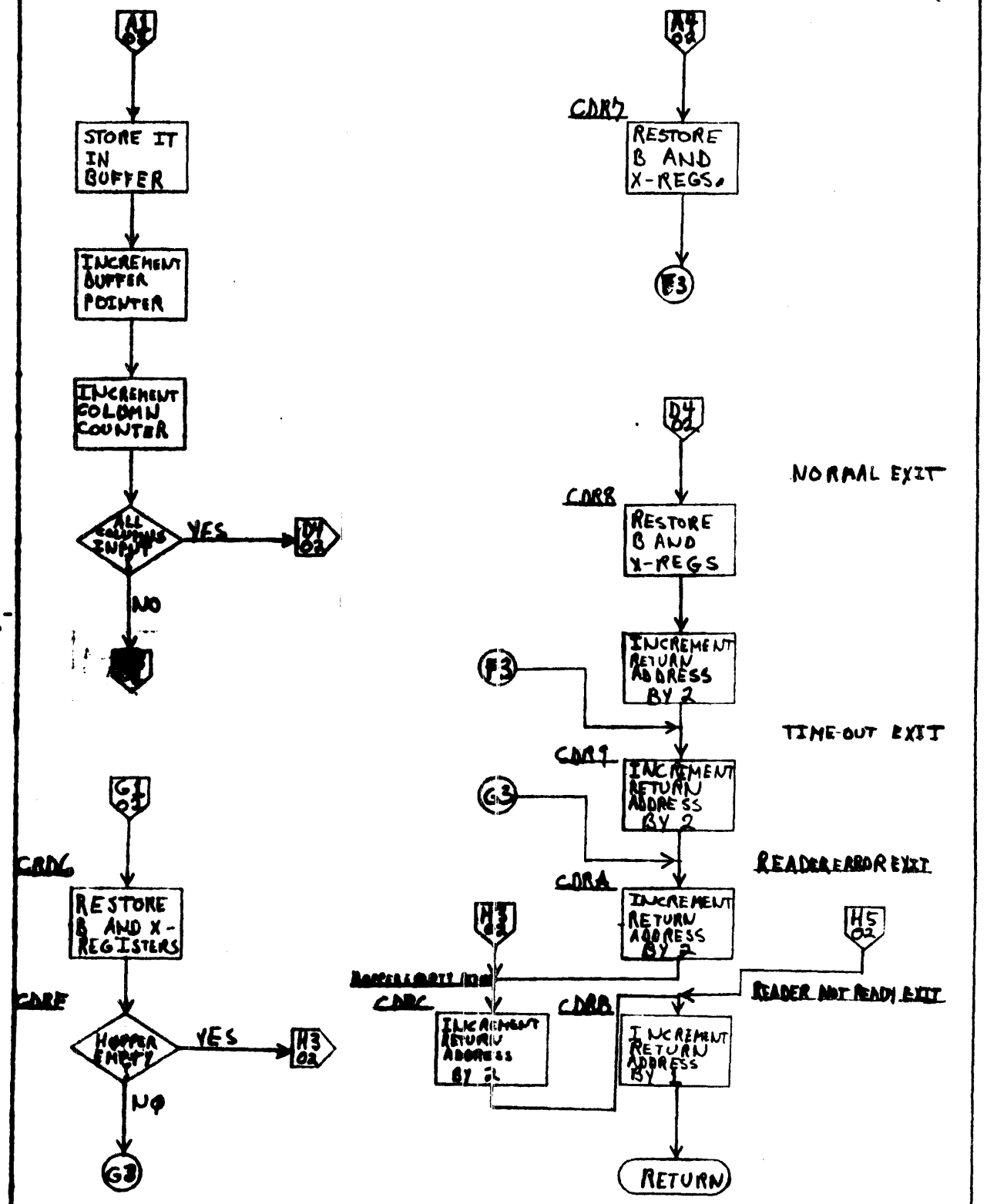

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Title: CARD READER DRIVER (PIM CONTROL)

Symbolic Name: PMRD

Purpose: To input and store 80 columns of data from 1 card using PIM control.

Description: The X and B registers are saved and the card reader and PIM device addresses are set by calls to DVAD. A reader ready is sensed, and if true a card is fed. The PIM is then disabled, the trap branch set, and the PIM enabled. Columns are then input when each interrupt is received. If reader ready was sensed originally, or a reader error is sensed, and/or a hopper empty condition is sensed, or too long is spent waiting for an interrupt - an appropriate error exit is taken. Otherwise a normal exit is taken.

Entry Points: The only entry point is PMRD.

Calling Sequence: CALL PMRD. (Buffer Address)[1 word]; (Reader Not Ready Return)[2 words]; (Hopper Empty Return)[2 words]; (Reader Error Return)[2 words]; (Interrupt Time-out Return)[2 words]; (Normal Return).

Entrance Parameters: The buffer address is specified in the first data word after the call to PMRD. No registers need be set for entry.

Exit Point: The exit points are given in the calling sequence and with the exception of the normal return, must contain JMP instructions.

Exit Parameters: The B and X registers are returned to their original state.

Table or Files
Modified or Read: 80 characters are stored in the given buffer, IBUF starting from the beginning.

Tables or Files
Created: N.A.

Called By: Mainline Program (START)

Called From: Device Address Setter (DVAD)

Exception Conditions: The device address of card reader and PIM and the trap location and interrupt mask must be stored in $CRD, $PIM, INLO, and MASK, respectively.

Timing: 900 cards per minute for 620-22 and 300 cards per minute for 620-25, 620-28.

Size: 0145 words.

Comments: The user must set $CRD, $PIM, INLO, and MASK to the card reader device address, PIM device address, trap location, and interrupt mask, respectively, before calling PMRD. The return points must also contain jumps to the appropriate processors.

Special Notation: N.A.

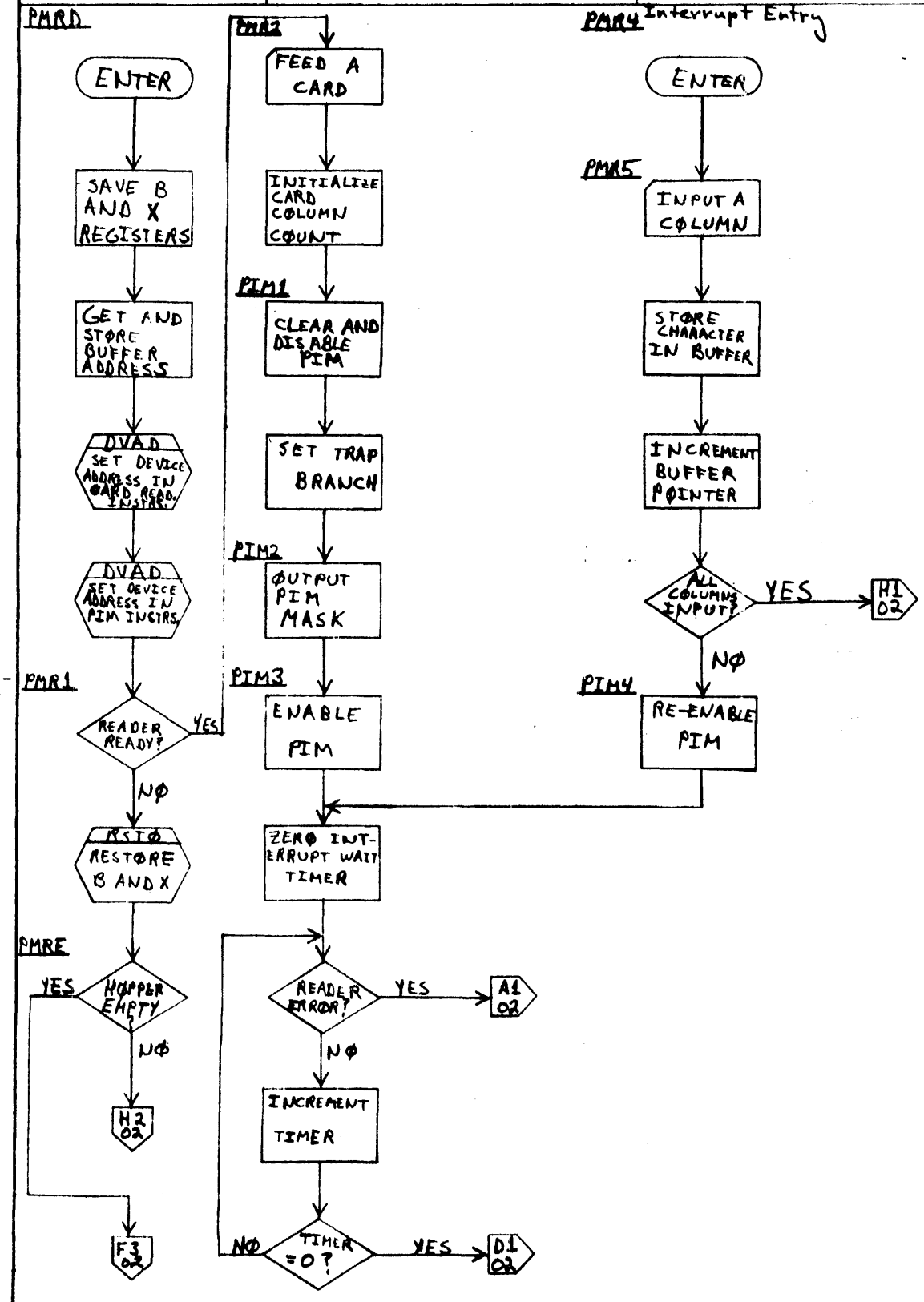
Hardware Details: SEN 0630, SEN 0330, EXC 0230, EXC 0540, OAR 040, EXC 0240, SEN 0230, CIA 030*.

Flowcharts: See following sheets.

* Device addresses of 030 and 040 are assumed for the card reader and PIM, respectively.

Flowchart Worksheet

PROGRAMMER: Purcell	PROGRAM NO.:	DATE	PAGE 1
CHART I.D.	CHART NAME	PROGRAM NAME	



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FOLD UNDER AT DOTTED LINE

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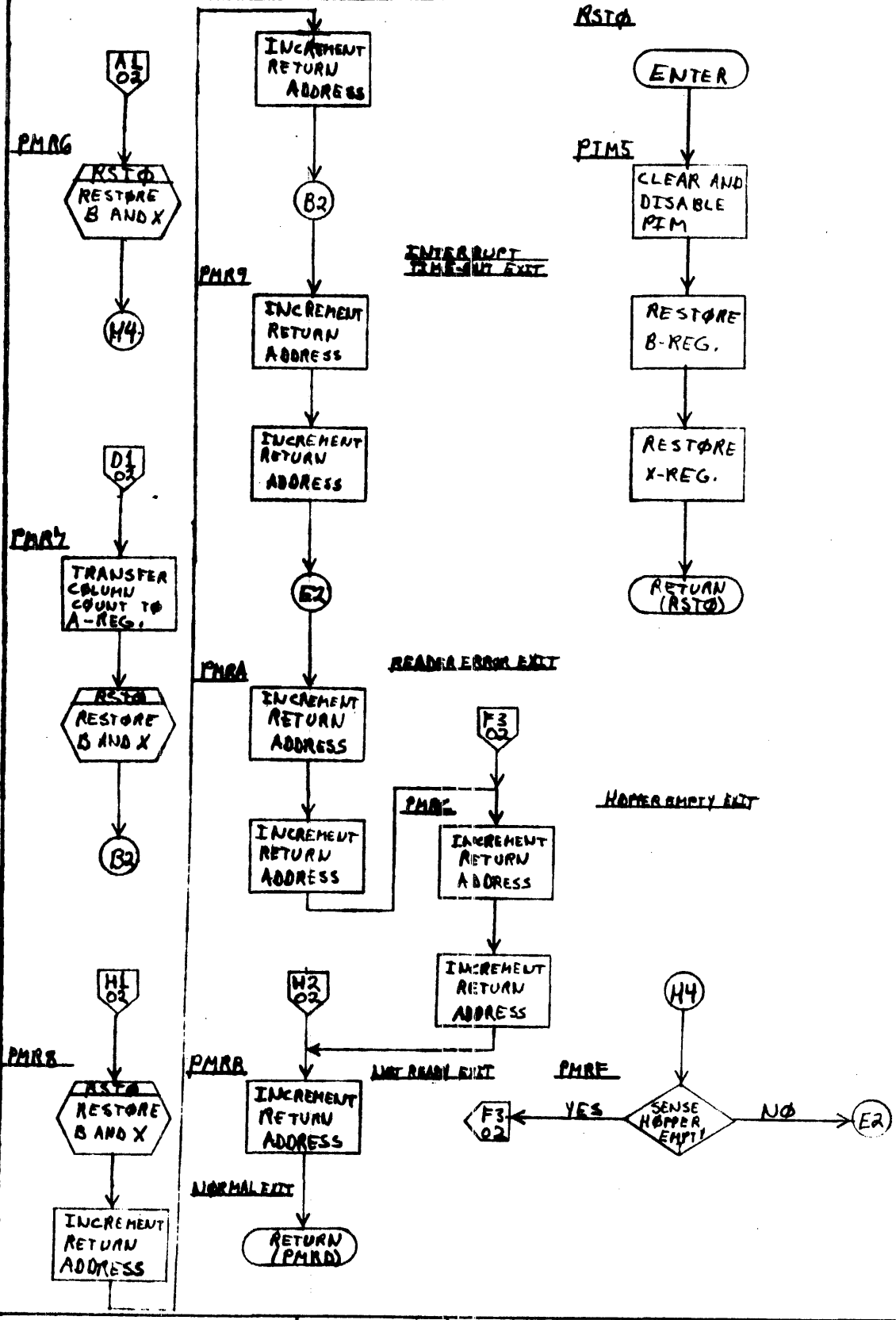
89A0340-000A

Flowchart Worksheet

PROGRAMMER:	PROGRAM NO.:	DATE	PAGE 2
CHART I.D.	CHART NAME	PROGRAM NAME	



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89A0340-000A

Title: CARD READER DRIVER (BIC CONTROL)

Symbolic Name: BCRD

Purpose: To input and store 80 columns of data from 1 card using BIC control.

Description: The X register is preserved and the card reader and BIC device addresses are set by calls to DVAD. A reader ready is sensed, and if true a BIC not busy is sensed. If true the BIC is initialized, an initial and final buffer address are output to the BIC, the BIC is activated and a card is fed. If the BIC goes not busy before a BIC abnormal stop, reader error or time-out occur, a normal exit is taken. These conditions plus the initial conditions of reader not ready and/or hopper empty or BIC busy have separate exits.

Entry Points: The only entry point is BCRD.

Calling Sequence: CALL BCRD; (Buffer Address) (1 word); (Reader Not Ready Return) (2 words); (Hopper Empty Return) (2 words); (BIC Busy Return) (2 words); (Reader Error Return) (2 words); (BIC Abnormal Stop Return) (2 words); (Time-out Return) (2 words); (Normal Return).

Entrance Parameters: The buffer address is specified in the first data word after the call to BCRD. No registers need be set for entry.

Exit Point: The exit points are given in the calling sequence and with the exception of the normal return, must contain JMP instructions.

Exit Parameters: The B and X registers are returned in their original state.

Table or Files Modified or Read: 80 characters are stored in the given buffer, IBUF; starting from the buffer beginning.

Tables or Files Created: N.A.

Called By: Mainline program (START)

Called From: Device Address Setter (DVAD)

Exception Conditions: The device address of card reader and the first device address of BIC must be stored in $CRD and $BIC before entry.

Timing: 900 cards per minute for 620-22 and 300 cards per minute for 620-25, 620-.8.

Size: 0136 words

Comments: The user must set $CRD and $BIC to the card reader device address and first BIC device address before calling BCRD. The return points must also contain jumps to the appropriate processors.

Special Notation: N.A.

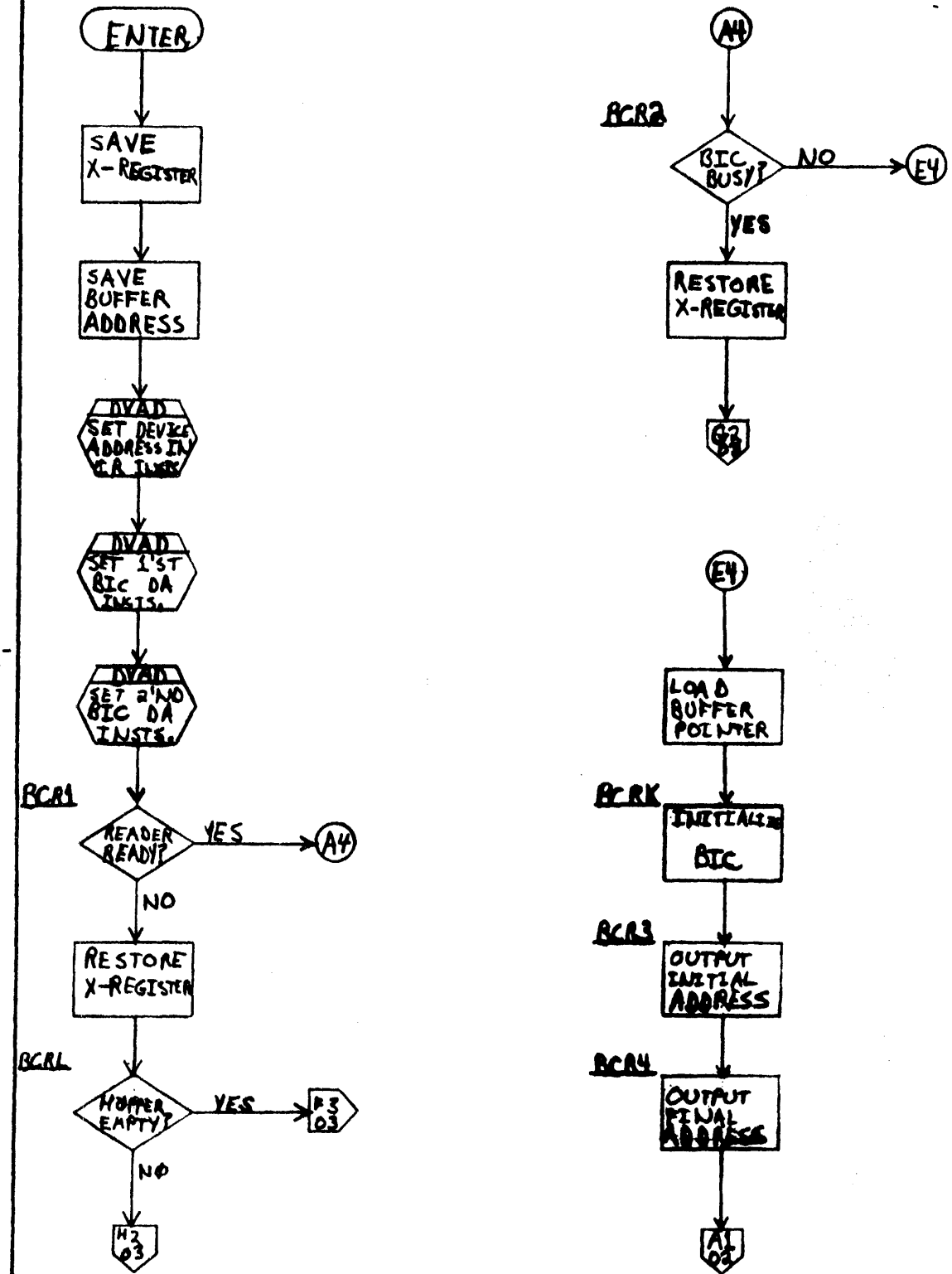
Hardware Details: SEN 0630, SEN 0330, SEN 020, EXC 021, OAR 020, OAR 021, EXC 020, EXC 0230, SEN 0230, SEN 021*

Flowcharts: See following sheets.

*Device addresses of 30 and 20 are assumed for the card reader and BIC, respectively.

PROGRAMMER Purcell	PROGRAM NO.	DATE	PAGE 1
CHART I.D.	CHART NAME	PROGRAM NAME	

BCRD



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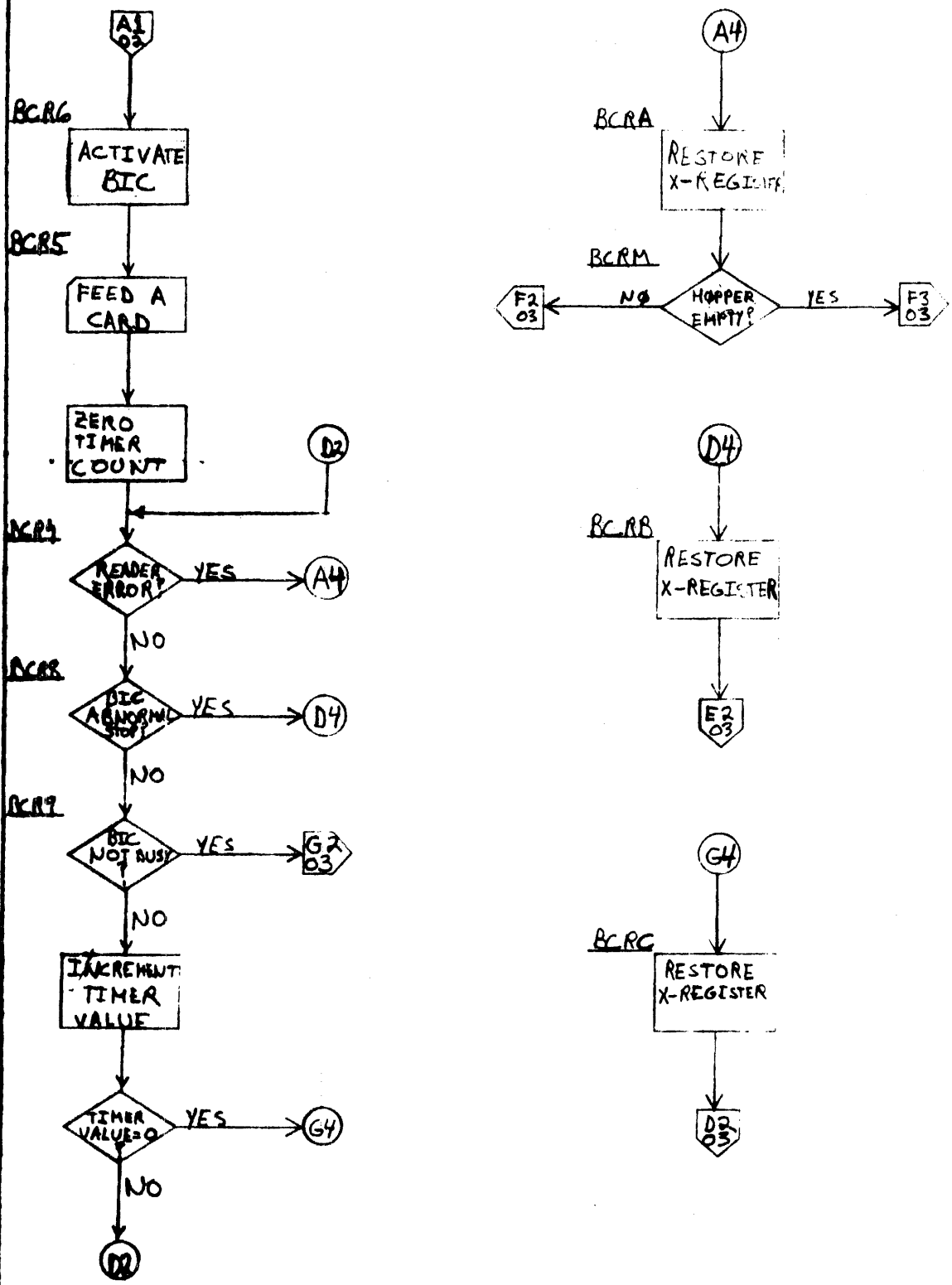
	PREPARED BY	APPROVED BY	SHEET 47 OF 51

04A0540-900A

PROGRAMMER	PROGRAM NO.	DATE	PAGE 2
CHART I.D.	CHART NAME	PROGRAM NAME	



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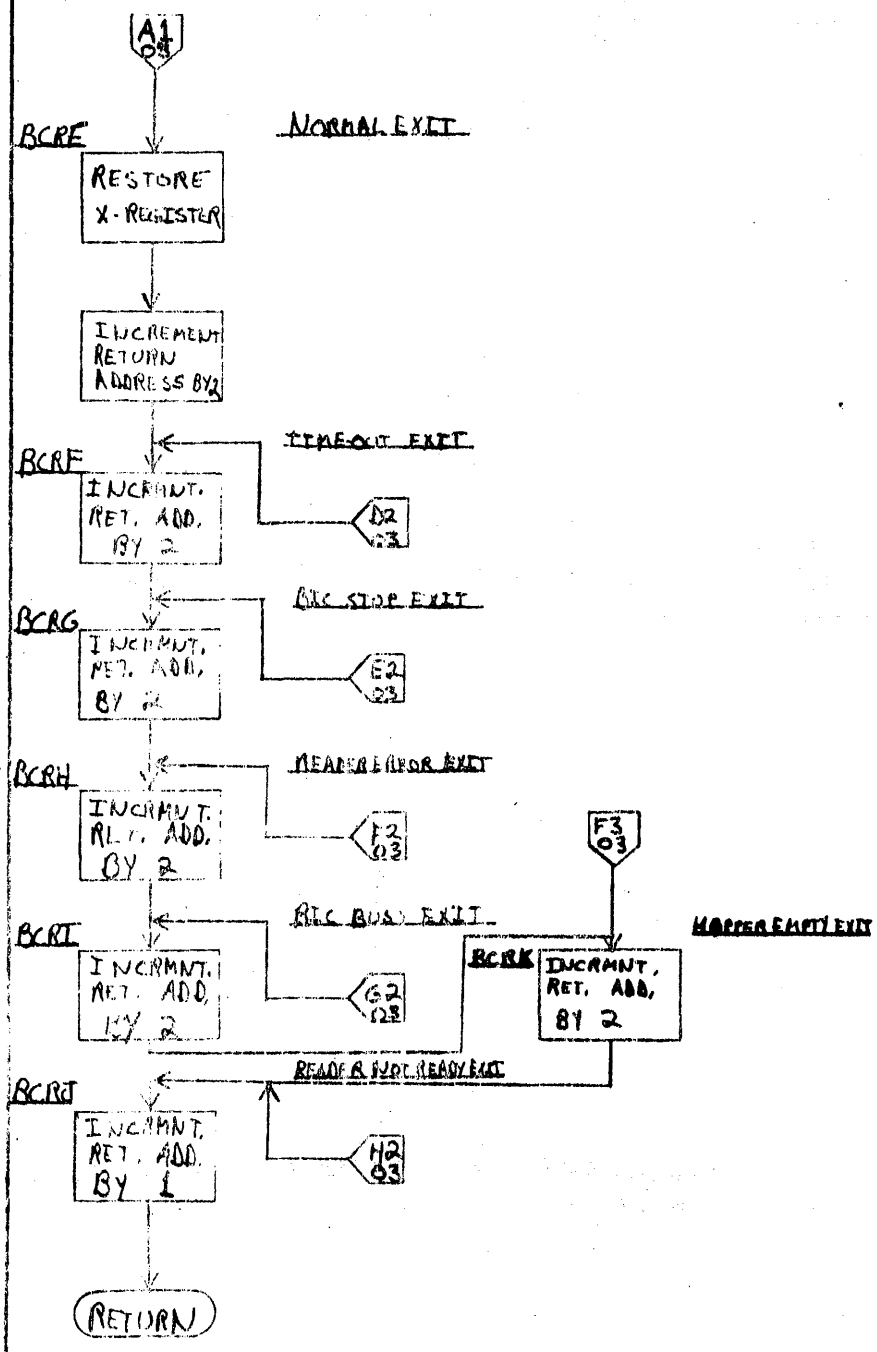
	PREPARED BY	APPROVED BY	SHEET 48 OF 51

PROGRAMMER	PROGRAM NO.	DATE	PAGE 3
CHART I.D.	CHART NAME	PROGRAM NAME	



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89A0346-B00A

SECTION 4: TEST SPECIFICATIONS

4.1 OBJECTIVES

The purpose of this section is to provide the user with information as to which hardware configurations have been run with the 620 Card Reader Test and give hardcopy examples of TTY output as a result of running the test in Teletype Mode. Within reason, a concerted attempt was made to test as many combinations of conditions as possible and provide example output.

4.2 CONFIGURATION

The following hardware configurations were successfully checked out with the program:

620/F-100 with 620-25

620/F-100 with 620-28

4.3 TEST RECOMMENDATIONS

In order to thoroughly test the card reader, it is necessary to simulate certain error conditions to see if a card reader error (or in the case of a dark check reader not ready is sensed) is then sensed. A pick failure is created by placing the thumb below the bottom of the deck in the input hopper during the reading of cards. Produce enough upward pressure to keep the next card from being fetched but do not push-up the deck and thereby produce a hopper empty.

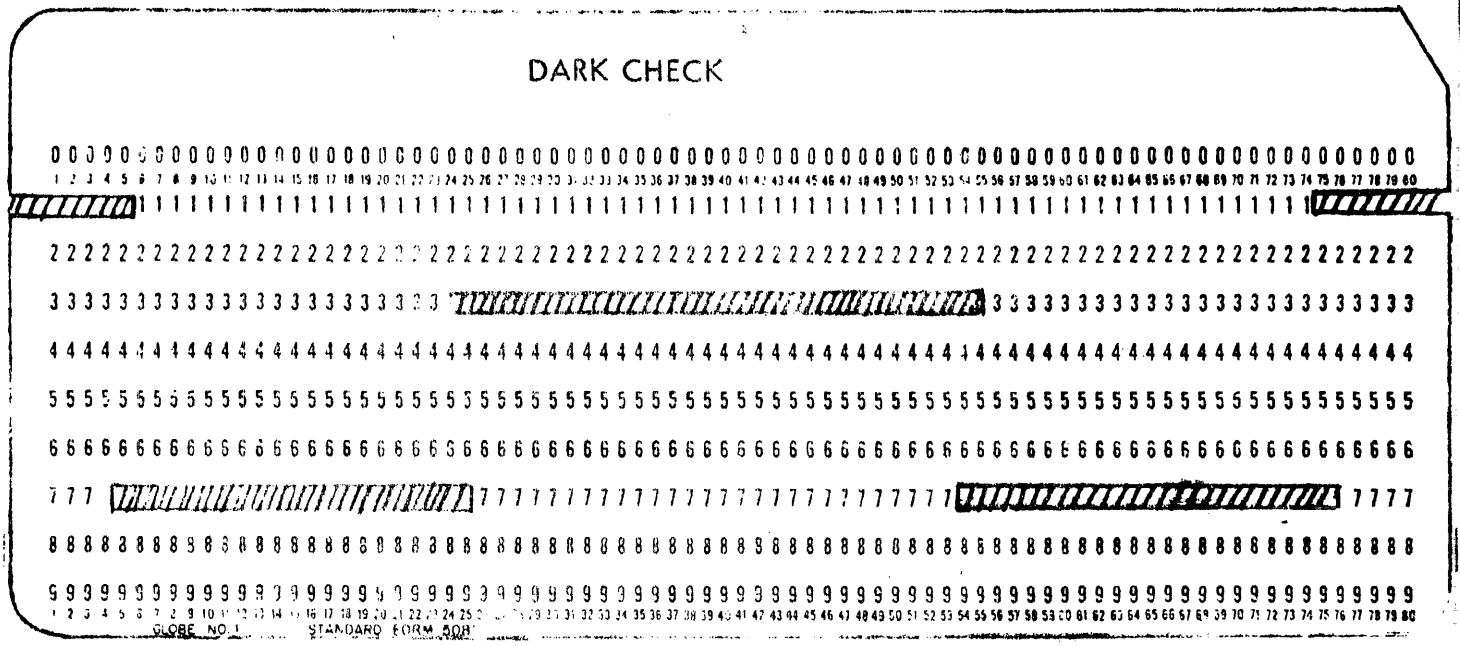
A hopper empty is best produced by allowing the cards to run-out in the input hopper.

The stop button should be pressed (only momentarily, or a time-out will occur) during the reading of cards, and then the reader re-readied to insure that no interference with data transfer takes place.

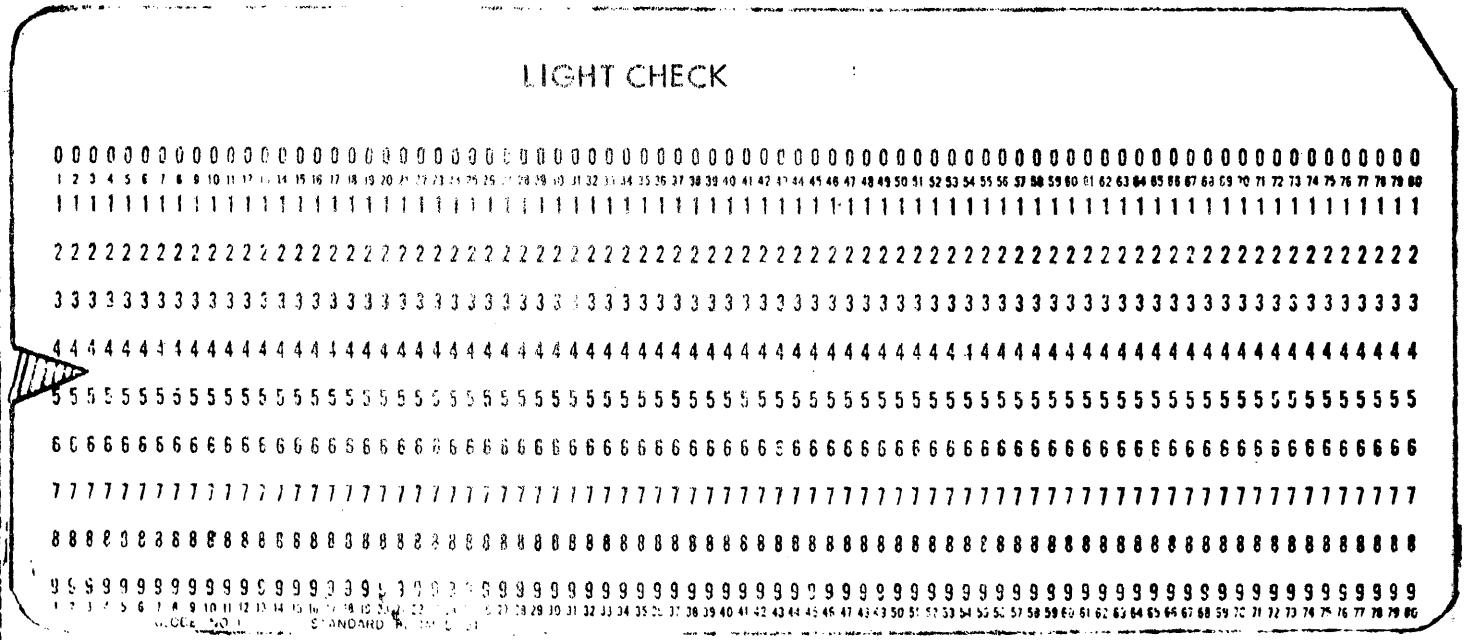
A light check is produced by inputting card A (on the following page) nested in a deck of good cards:

A dark check is produced by inputting card B (on the following page) nested in a deck of good cards:

Card B



Card A



11.1 ← SHADED AREAS ARE CUT-OUT

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USER'S GUIDE
ANALOG-TO-DIGITAL CONVERTER MODULE
for use with
Varian 620 or V73 Series Computers

Publication No. 03-996806D

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1. INTRODUCTION

1.1 GENERAL

The Analog-to-Digital Converter Module (ADCM) is a hardware option that interfaces Varian 620 and V-73 series computers to external analog devices. Two ADCM models are available to provide either 13-bit or 10-bit analog-to-digital resolution. An ADCM includes four functional features:

- An Analog-to-Digital Converter (ADC), which converts analog input signals to either 13-bit or 10-bit digital data words for input to the computer.
- A Sample and Hold Amplifier, which monitors analog input between conversions and provides a constant voltage source representing analog input to the ADC during conversion.
- A Programmable Timer, which generates a train of timing pulses, with the pulse rate determined by a computer program.
- External Sense Input Logic, which allows a computer program to test the status of an external device by sampling the logic level present on an external sense input line.

In a maximum configuration, the ADCM may be used in conjunction with Varian Multiplexer and Multiplexer Expansion Modules to accommodate as many as 256 single-ended or differential analog input channels. As many as eight ADCMs can be attached to a single computer. Refer to the Multiplexer Manual (Varian Publication No. 03-996-807) for details regarding this interface capability.

Simple installation procedures allow the ADCM to be installed either at the factory or on-site at the user's facility. A comprehensive software test package is provided with the ADCM for post-installation checkout of its operational status.

In addition, the module is fully supported by standard Varian software and input/output options.

1.2 FUNCTIONAL DESCRIPTION

The elements responsible for performing the four basic ADCM functions (analog-to-digital conversion, sample and hold, timing pulse generation, and External Sense decode) are shown in Figure 1-1.

Each ADCM has a unique device address, which is set at time of installation, and its own device address decode logic. The unique device address is used by the computer to select a particular ADCM for operation. Eight device addresses (60_8 to 67_8) are reserved for ADCMs.

Sample and Hold

A sample and hold circuit continuously monitors the analog input signal during the intervals between data conversions. At the start of a conversion, it stores the most recent input voltage level and provides the ADC with a constant voltage for the conversion.

Conversion

The actual data conversion can be initiated by one of three means:

- Program Control — Data conversion can be started using an External Control (EXC) Instruction.
- Programmable Timer Control — Pulses from the timer can start the ADC.
- External Control — The ADC can be initiated by an external start signal, whose source is determined by the user.

The ADC performs data conversion as a series of discrete operations. The current amplitude of the analog input signal is converted to either a 13-bit or 10-bit

binary number that corresponds to the input voltage level. The 13 bits include 12 data bits and a sign bit, in two's complement format. Similarly, the 10-bit number consists of nine data bits and a sign bit. Digital outputs from the ADCM are presented to the E-bus via buffer registers, which store the data between conversions.

Data transfers from the ADCM to the computer may be under direct program control or under control of the optional Buffer Interlace Controller (BIC). When operating under program control, the computer initiates data transfer in response to the execution of a programmed input/output control instruction. When operating under the hardware BIC option, data transfers are initiated and executed without program instruction control. Thus, the BIC minimizes software overhead and permits data to be transferred at high speeds without interrupting the processing sequence of the main computer program.

Sense Interface

The ADCM sense interface logic provides the program with three types of sense information — external sense, data sense, and timer sense. The logic level present on the External Sense input line defines the status of an external device. A true level on the Data Sense line informs the program that a new data word has been set into the buffer register. A true level on the Timer Sense line informs the program that the programmable timer has generated a timing pulse.

Note that if the computer is equipped with a Program Interrupt Module (PIM) option, interrupts may be set by the ADC DATA READY signal and the TIME INTERVAL COMPLETE signal. Thus, the PIM option may be used to simplify the programming task of checking the input sense lines.

Programmable Timer

The programmable timer generates a pulse each time its decrementing counter reaches zero in a count cycle. The counter begins counting down from a binary number which is set in its buffer register by a data transfer out program instruction. The original value for this number remains in the buffer register until a new value is received.

The timer may be operated in either a continuous or a single cycle mode. In continuous mode, the timer pulse generated at the end of a count cycle starts a new cycle. In single cycle mode, each new count cycle must be started by a signal from an external device which is connected to the timer. In either mode of operation, the duration of the timer interval is set in the buffer register by programmed instructions.

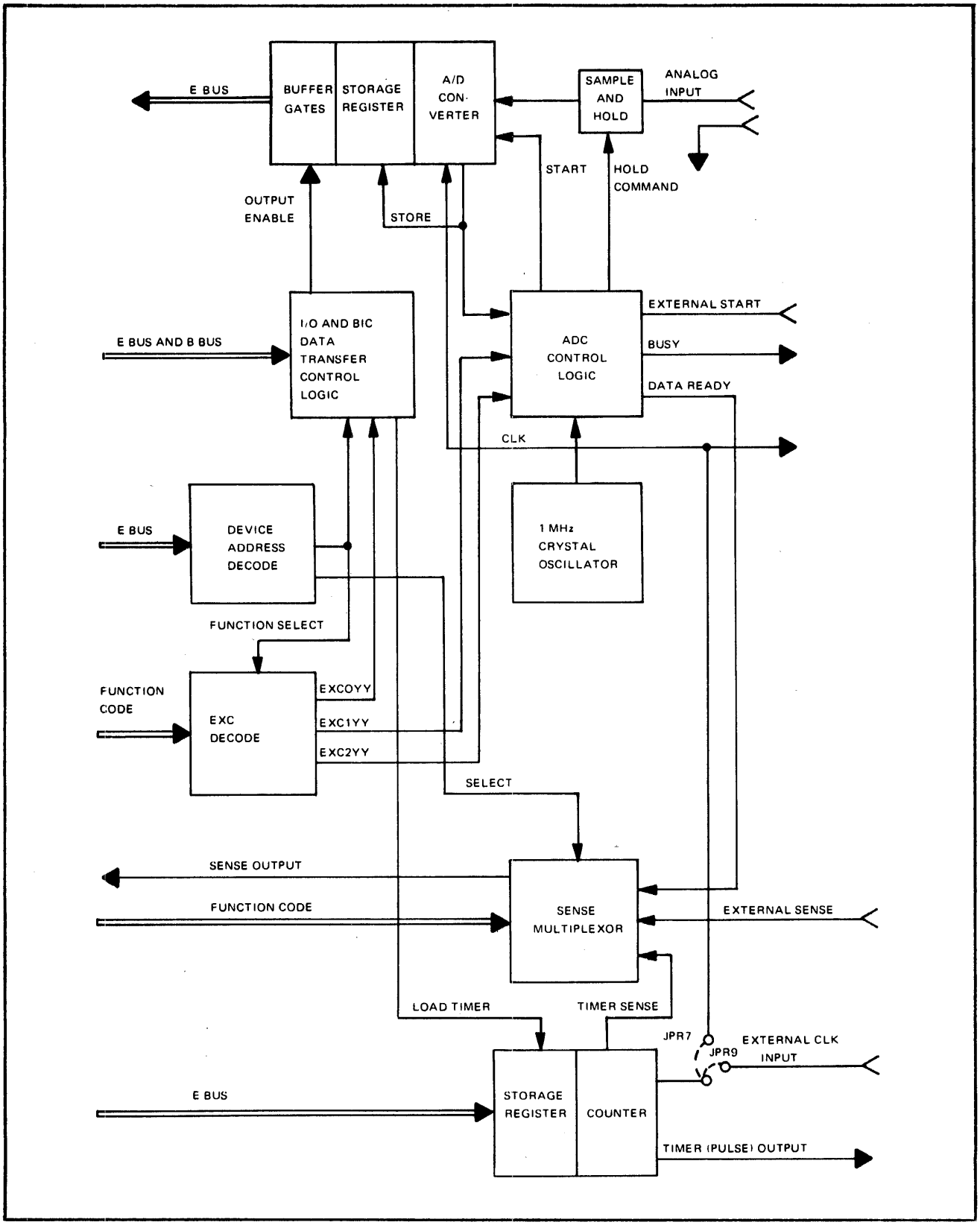


Figure 1-1. ADCM Block Diagram

2. PROGRAMMING

2.1 INTRODUCTION

This section describes Assembly Language programming techniques for operating the ADCM and presents instructions for using the software test package for checkout of the ADCM. The ADCM functions which are programmed include setting the timer pulse interval, checking the status of a sense line, and directing ADC operations. More detailed programming information may be found in the 620 series or V-73 system handbooks.

2.2 CHECKING SENSE LINES

Three programming instructions are used to check the status of sense lines associated with the ADCM:

SEN 0YY	Checks if a data word is ready to be transmitted to the computer.
SEN 01YY	Senses if the timer has counted down to zero.
SEN 02YY	Tests the state of the external sense input line, which indicates the status of some external device.

where YY specifies the ADCM device address, which may be any octal number from 60 to 67.

2.3 SETTING TIMER INTERVAL

The ADCM timer may be programmed to provide a timing pulse at a predefined interval. This is accomplished by using assembly language programming instructions to define the interval to the computer and to transfer the defined value from the computer to the timer buffer register.

The defined value for the timer interval is transmitted from the computer to the timer buffer register as a 16-bit number (less than or equal to 65535). The clock decrements this number at the rate of one count per microsecond (two counts per microsecond in a 10-bit converter) and issues a timer pulse when the count reaches zero. In continuous mode, the timer automatically resets itself to the value in the buffer register and begins a new cycle. In single cycle mode, the next cycle must be initiated by an external signal. The timer mode is prewired to user specifications, but may be changed after installation.

The DATA assembler directive may be used to define the timer interval value to the computer. After this value has been defined, it may be loaded into the timer buffer register either directly from memory or via the computer's input/output registers. Thus, one of three statements is used to load the buffer register:

OAR 0YY	Output value from A Register to buffer registers
OBR 0YY	Output value from B Register to buffer registers
OME 0YY	Output value from memory to buffer registers

where YY is the device address of timer buffer register, which may be any octal number from 60 to 67. Note that when the OAR or OBR instruction is used, it must be preceded by the appropriate load instruction (LDA or LDB) to load the computer input/output register.

The status of the timer can be sensed by issuing a SEN 01YY instruction. A true sense response on the ADCM Sense line 1 indicates that the timer has decremented to zero; a false level indicates that it has not. The timer continues operation whether or not the sense line is sampled. A true sense response resets the line to false after completion of the sense instruction.

2.4 PROGRAMMING ADC OPERATION

Data may be transferred from the analog input into the computer in one of three ways:

1. Under total control of a user program. In this mode of operation, the program continuously monitors the ADC to provide correct timing.
2. Under control of a Buffer Interlace Controller (BIC). The BIC implicitly utilizes the computer's interrupt structure to eliminate the need for the program to wait for ready signals from the ADC.
3. Under control of an interrupt service routine which is initiated by the Real Time Clock or an input to a Priority Interrupt Module (PIM). This method makes explicit use of the interrupt structure. This method of programming is difficult and should not be attempted by beginners. The service routine itself uses program control and is similar to method number 1. The difference in this method is in the interaction of the service routines with other sequences of instructions being executed in the computer. This interaction is not unique to the ADC module and, for that reason, is not described in this manual.

All of the computer instructions which are used to program the ADCM are described in this section. Note that all of these instructions are not required in any single mode of operation. In the descriptions of program instructions, the symbol YY is used to designate the two octal digits of the device address wired for the module.

Several options are possible by placing jumper connections both on the ADCM and on the backplane of the slot. These options are mentioned in other sections of this manual. The programming instructions given in this section apply to the wiring combinations which are used most frequently.

These combinations are:

- The timer output pulse is wired to the external start (conversion) of the ADC.

- The timer counter is wired to accept pulses from the clock circuit on the module. Pulses are generated at the rate of one per microsecond. Hence the maximum timer interval is 65,535 microseconds.

Note that, therefore, the external start input is always receiving inputs since the timer is always running. Therefore, this input should be gated out by EXC 03YY if it is not going to be used.

Analog to Digital Conversion

The following program instructions are used to initilize and direct analog-to-digital conversion:

EXC 01YY — Begins analog-to-digital conversion. Input is sampled continuously until conversion begins, at which time the analog value is fixed by a "hold" circuit until conversion is complete.

EXC 02YY — Opens a gate circuit which permits conversion to be initiated by the external start input (normally wired to the timer output pulse). An open gate does not prevent EXC 01YY from also starting the conversion cycle.

EXC 03YY — Closes the gate circuit opened by EXC 02YY. EXC 03YY should be used prior to a data run when it is desired to initiate each conversion by EXC 01YY only. That is, possible false starts are locked out.

SEN 0YY — Indicates data is ready as a result of an analog-to-digital conversion. This data ready line is set false (not ready) when conversion begins and resumes its true condition (ready)

when conversion is complete. It remains true until reset by an input instruction. The conversion process requires about 13 to 14 microseconds. Another conversion should not begin until the input circuit has sufficient time to settle on a new value (approximately 6 microseconds).

Data Input

Data may be input to the computer using the following program instructions:

CIA (INA) 0YY
CIB (INB) 0YY
CIAB (INAB) 0YY
IME 0YY, < MEM LOC>

These instructions enter the result of a conversion cycle into (respectively):

A register
B register
A and B registers
Memory location (MEM LOC)

Each of the instructions resets the data ready input (SEN 0YY). Therefore a "dummy" input instruction should be given prior to a data run. The dummy input acquired in this manner may be ignored.

Timer Control

The timer control instructions are as follows:

OAR 0YY
OBR 0YY
OME 0YY, < MEM LOC>

Enters a 16-bit word (0 to 65,535) into the timer register, synchronizes the start of the timed interval, and resets the timer ready signal. The timer register represents the

number of clock periods in the interval. Normally, the timer is driven by an internally generated clock cycle of one microsecond.

SEN 01YY — Senses timer ready (interval complete). If found ready, the timer ready signal is reset to "not ready." The timer cycles continuously, setting the ready signal at the end of each cycle.

BIC Data Transfer

The following instruction is used to connect the ADCM to a BIC:

EXC 0YY — Connects the ADCM for BIC transfer. The BIC set-up sequence must be performed prior to connecting the BIC.

2.5 PROGRAMMING EXAMPLES

The following examples illustrate typical program instructions which may be used to direct ADCM operation. The examples assume a 13-bit ADCM with device address 60_8.

Example 1 — High Speed Under Program Control

In this example, each conversion cycle is begun by a computer instruction at the maximum acquisition rate (50 kHz). One hundred data points are acquired and stored in memory beginning at the memory address labelled FIRST. The program runs from the address labelled START. When all data is acquired, the computer halts at the address labelled DONE.

```
        ,ORG        ,0500
*       This Example Uses Program Control Exclusively
*       Data is Acquired at the Maximum Rate = 1 Sample Every 20
*       Microseconds. The Timer on the ADC Module is Used to Time
```

```
*       Conversion Cycle.  Of the Total 20 Microseconds, 13 — 14
*       Microseconds are Required for Conversion and 6 Microseconds
*       Are Required for the Sample and Hold Input to Settle on the
*       Analog Input.
ADC     ,SET     ,0060          Define Device Address for the ADC Module
START,  EXC      ,0300+ADC      Close the External Start Gate
        ,LDB     ,COUNT         Use B Register as Counter for # Sample Points
        ,LDX     ,FIRST         Use X Register to Point to Data Buffer
        ,CIA     ,ADC           Clear Data Ready Line with Dummy Input
        ,LDA     ,TIME
        ,OAR     ,ADC           Load and Synchronize Timer for Sample Rate
LOOP    ,EXC     ,0100+ADC      Start A to D Conversion Cycle
        ,NOP     ,              Need Two NOP's in Loop to Permit Operation
        ,NOP     ,              Of System Interrupts (Like BIC and PF/R)
        ,SEN     ,ADC, TAKE     Go Take Data When Conversion Cycle Complete
        ,JMP     ,LOOP+1        Else Wait
TAKE    ,JBZ     ,DONE          All Data Taken When B REG = 0
        ,CIA     ,ADC           Take Digital Value From Conversion Process
        ,STA     ,0, 1          Store in Memory (Data Buffer)
        ,IXR     ,              Point to Next Location in Buffer
        ,DBR     ,              Count the Sample Point Taken
CHECK,  SEN      ,0100+ADC, LOOP  Wait for Timer Interval Complete
        ,NOP     ,              NOP's Make This an Interruptible Loop
        ,NOP     ,
        ,JMP     ,CHECK         Wait in Check Loop Until Interval Up
DONE    ,HLT     ,0             Finished
COUNT,  DATA     ,100           #Sample Point in this Data Run
FIRST   ,DATA    ,BUFF          Beginning Address of Data Buffer in Memory
TIME    ,DATA    ,20            20 Microseconds = Min Conversion Cycle
BUFF    ,BSS     ,100           Reserve 100 Locations for Data (Data Buffer)
        ,END     ,
```

Example 2 - Data Acquired Via BIC Transfer

In this example, the BIC is used to acquire data. Note the following points:

1. The first data point is acquired through a programmed start (EXC 0100 + ADC). All other conversion cycles are started by the timer. This command could be omitted; in which case, the first conversion cycle would not take place until one timer interval was completed.

2. A BIC can be wired to multiple devices but may be used by only one device at a time. Therefore, it is necessary to check for BIC busy before setting up for this operation. Normally, after connecting a device to a BIC, the program does not simply wait for the BIC to complete its job; it usually executes some other sequence of instructions.

```
        ,ORG     ,01000
*       This Example Shows Data Transfer Under BIC Control
ADC     ,SET     ,060          Define Device Address for ADC Module
BIC     ,SET     ,020          Define Device Address for BIC
*       Close External Start Gate to Prevent Inadvertant Input
        ,EXC     ,0300+ADC     Close Gate
BRDY    ,SEN     ,BIC, GO      Go If BIC Not Busy With Some Other Device
        ,NOP     ,             Provide Interruptible Loop for Wait
        ,NOP     ,
        ,JMP     ,BRDY         Check BIC Again
GO      ,EXC     ,BIC + 1      Prepare BIC to Receive Instructions
        ,LDA     ,FIRST        Get First Location of Data Buffer
        ,LDB     ,LAST         Get Last Address of Data Buffer
        ,OAR     ,BIC          Output First to BIC
```

```
        ,OBR     ,BIC + 1          Output Last to BIC
        ,CIA     ,ADC              Reset Data Ready Input From ADC
        ,LDA     ,TIME             Get Timer Interval
        ,OAR     ,ADC              Reset Timer to Known Interval
        ,EXC     ,0200 + ADC       Open Ext Start Gate to Let Timer Pulses In
        ,EXC     ,BIC              Enable the BIC - But Don't Go Yet
        ,EXC     ,ADC              Connect ADC to BIC - Begin Transfer
        ,OAR     ,ADC              Start and Synchronize Timer for Real
        ,EXC     ,0100 + ADC       Start First Conversion Cycle
WAIT    ,SEN     ,BIC + 1, ERROR   Error if Can't Complete all Data Transfers
        ,SEN     ,BIC, DONE        Finished with all Data Transfers
        ,NOP     ,                 Interruptible Loop
        ,NOP     ,
        ,JMP     ,WAIT             Instead of Wait, Could Do Other Things
ERROR,  CIA      ,BIC              Get Address for Last Successful Transfer
        ,HLT     ,07               A Reg Should be Less than Contents of Last
DONE    ,TZA     ,                 Normal Finish With A = 0
        ,HLT     ,0
FIRST   ,DATA    ,BUFF             First Word of Data Buffer
LAST    ,DATA    ,BEND             Last Word of Data Buffer
TIME    ,DATA    ,1000             Min = 20 Microsecs; Max = 65,535 Microsecs
BUFF    ,BSS     ,100              Reserve 100 Words for Data Buffer
BEND    ,BES     ,0                Label Last Word of Buffer
        ,END     ,
```

2.6 ADC/MULTIPLEXER SOFTWARE DRIVERS

The software support modules supplied with the ADCM provide a means of convenient access to an ADCM/Multiplexer combination without detailed user knowledge of hardware. The modules may be used by themselves or embedded in an operating system.

Two types of software modules are supplied to accommodate both programmed data transfers and direct memory access data transfers. These two types of modules may be coresident in memory or they may be used individually. The programmed data transfer module provides a higher degree of flexibility in the order of channel selection, timing, and data synchronization with an external source transfer mode. This flexibility is paid for in software overhead which limits the maximum data acquisition rate to 10 kHz (20 kHz for 10-bit version) using a 620/i or 620/L. Proportionally higher rates can be achieved using the faster 620/f or V-73. The direct memory transfer technique (using a BIC) will provide data rates up to 50 kHz (100 kHz for 10-bit version), with other processing proceeding concurrently. This mode is limited to sequential channel or single channel input.

This section describes these software modules and presents programming examples of their use. In the descriptions and examples, the following device address assignments are assumed:

Address (Octal)	Device
060	ADCM
040	Multiplexer
020-021	BIC, No. 1
022-023	BIC, No. 2
024-025	BIC, No. 3
026-027	BIC, No. 4

Programmed Data Transfer

The programmed ADC data transfer module (PADC) permits the user to specify:

- Channel selection technique (random or sequential).
- Last channel to be read for sequential mode or channel list specification for random mode.

- Quantity of input data and location at which the data is to be stored in the computer memory.
- Time interval between the sampling of individual channels within the scan.
- Time interval between successive starts of the channel-scanning process.
- An error address to which control is to pass if an error is detected in the module arguments.

The PADC module is called with the following assembly language sequence:

CALL PADC, MODE, CHANNELS, TIME, TIME PERIODS, NUM, DESTINATION, EXIT

All entries in the calling sequence are either direct addresses or indirect addresses which point to the actual arguments. Multiple levels of indirect addresses are permitted. The arguments are defined as follows:

MODE — An integer value which specifies the technique for channel selection. A value of zero specifies sequential channel selection starting at channel 1 and ending at the value of CHANNELS for each scan. A value greater than zero specifies random channel selection and the number of entries in the CHANNELS array. For each scan in a random selection, the CHANNELS vector determines the order of selection.

CHANNELS — An integer vector; the values in the CHANNELS array determine the channel and order of selection for each scan. The size of this vector is determined by the value of MODE. When MODE = 0 (sequential channel selection), the size is one element which represents the number of the last channel to be collected during each scan. When MODE is greater than zero, its value represents the size of the CHANNELS vector.

TIME — An integer value which specifies the number of microseconds between each data sample in the scan. Therefore, TIME represents the elapsed time

between the start of each frame. If TIME is zero, each sampling will be synchronized to an external signal. The user should allow 50 microseconds (25 microseconds for 10-bit version) per channel collected within a scan to maintain proper time sychronization. For example, if seven channels are to be collected during each scan, the value of TIME should be at least 350 microseconds (175 microseconds for the 10-bit version).

TIME PERIODS — An integer value which specifies the number of time periods of TIME microseconds to elapse between each start of the channel-scanning process. That is, the scan interval, or time between scan starts, is (TIME x TIME PERIODS) microseconds in length.

NUM — An integer value which specifies the total number of data values to be collected and transferred to the DESTINATION vector.

DESTINATION — An integer array which is to receive the incoming data. At least NUM words must be allocated to accommodate the data. As each data value is input, it is placed in the next sequential location of DESTINATION.

EXIT — A program label to which control is to be transferred when illegal arguments are detected. The following conditions cause an error exit:

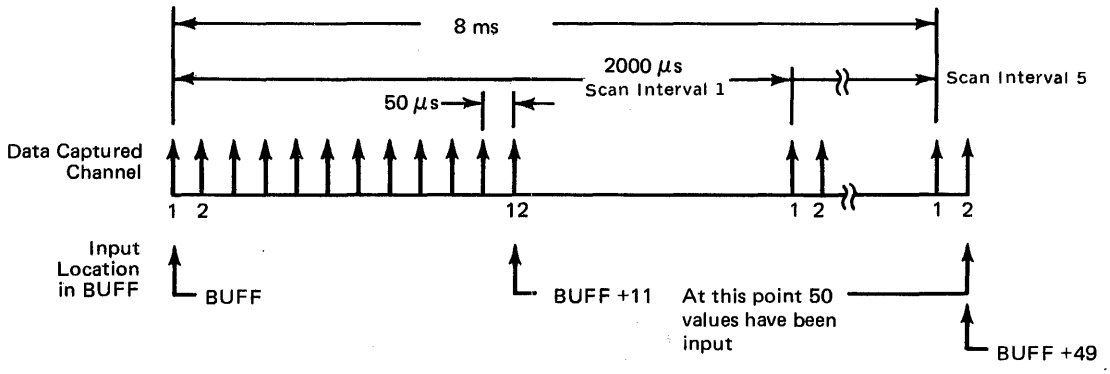
MODE less than 0.
CHANNELS not between 1 and 256, inclusive.
TIME PERIODS less than MODE for random mode.
TIME PERIODS less than CHANNELS for sequential mode.
TIME less than 0.
NUM less than or equal to 0.

Figures 2-1 and 2-2 show examples of the use of the PADC module to perform both sequential and random channel collection.

Problem Statement:

Acquire 50 data values from channels 1 through 12, with an individual channel data rate of 500 Hz. Scan interval is 2000 microseconds.

Timing Diagram:



Programmed Solution:

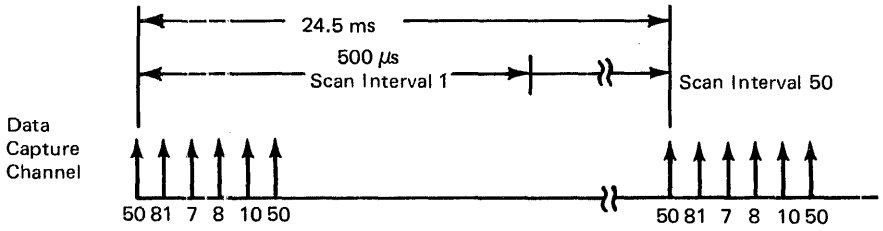
```
                ...
                CALL PADC, S, CADR, T, TP, NR, BUFF, ERR
                ...
ERR     HLT             HLT COMPUTER IF ARG ER
                ...
S       DATA 0          SELECT SEQUENTIAL MODE
CADR    DATA 12         LAST CHANNEL ADDRESS
T       DATA 50         50 MICROSECONDS/CHANNEL
TP      DATA 40         SCAN INTERVAL IS 40 TIME PERIODS
NR      DATA 50         ACQUIRE 50 VALUES
BUFF    BSS 50          RESERVE 50 WORDS OF STORAGE
```

Figure 2-1. Programmed Data Transfer-Sequential Selection

Problem Statement:

Acquire 300 data values from channels 10, 7, 8, 50, and 81. The individual channel data rate should be 2 kHz for channels 10, 7, 8, and 81, and 4 kHz for channel 50. The order of channel selection is 50, 81, 7, 8, and 10 for each scan.

Timing Diagram:



Programmed Solution:

```
                ...
                CALL    PADC,R,ADRS,T,TP,N,(BADR)*,BADARG
                ...
BADARG          CALL    ERPT        PRINT ERROR MESSAGE
                ...
R               DATA    6           LENGTH OF 'ADRS'
*    CHANNEL SELECT VECTOR
ADRS            DATA    50
                DATA    81
                DATA    7
                DATA    8
                DATA    10
                DATA    50          REPEAT FOR TWICE DATA RATE
*
T               DATA    500         50 MICROSECONDS PER READ
TP              DATA    10          10 TIME PERIODS PER INTERVAL
N               DATA    300         300 INPUT VALUES
BADR            DATA    BUFFER POINTER TO BUFFER
                ...
BUFFER          BSS     300         RESERVE 300 WORDS
```

Figure 2-2. Programmed Data Transfer — Random Selection

Direct Memory Data Transfer

Two direct memory transfer modules (DADC and SADC) utilize the BIC option and permit the user to acquire data from the ADCM/Multiplexer at a maximum rate (50 kHz for 13-bit or 100 kHz for 10-bit conversion), while the CPU can be working on an entirely different process. To do this, the user calls DADC to initiate the data transfer. Control will be returned immediately after initiation so that the user may proceed with independent processing. At the user's convenience, SADC may be called to determine whether or not the data transfer is complete.

DADC Module

The DADC module is called with following assembly language sequence:

```
CALL DADC, BICNR, MODE, CHAN, TIME, NUM, DEST, EXIT
```

All entries in the calling sequence are either direct or indirect addresses of the actual arguments. Multiple levels of indirect addresses are permitted. The arguments are defined as follows:

BICNR — An integer value which specifies the BIC that is to be used for the data transfer. The range of BICNR is from one to four corresponding to BICs using device addresses $20\text{-}21_8$ to $26\text{-}27_8$.

MODE — An integer value which specifies whether sequential channels are to be scanned (MODE = 0) or data from an individual channel is to be acquired (MODE $\neq$ 0).

CHAN — An integer value which determines the channels to be acquired. If MODE = 0 (sequential scan), CHAN represents the number of the last channel to be collected. If MODE $\neq$ 0 (single channel input), CHAN represents the number of the channel to be acquired.

TIME — An integer value which specifies the time in microseconds

between each data input. This value must be greater than or equal to 20 to prevent invalid conversions.

NUM - An integer value which specifies the total number of data values to be collected and transferred to the DEST vector.

DEST- An integer array which is to receive the incoming data. At least NUM words must be allocated to accommodate the data. As each data value is input, it is placed in the next sequential location of DEST.

EXIT - A program label to which control is to be transferred when illegal arguments are detected. The following conditions cause an error exit:

BICNR not between 1 and 4, inclusive.
CHAN not between 1 and 256, inclusive.
TIME less than 20.
NUM less than or equal to 0.

Figures 2-3 and 2-4 show examples of the use of DADC, in conjunction with SADC, to perform direct memory data transfers.

SADC Module

The SADC module checks the status of a previously initiated direct memory data transfer. SADC is called with the following assembly language sequence:

```
CALL SADC, STATUS
```

The single entry in the calling sequence can be either a direct address or an indirect address which points to the actual argument. The argument is defined as follows:

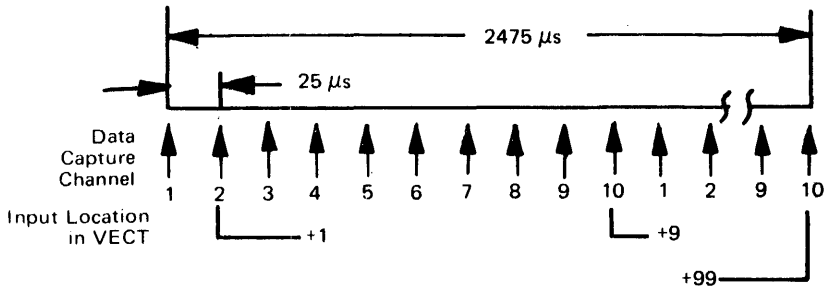
STATUS - This argument receives a value of 0, 1, or 2 to indicate the status of the transfer operation:

Value	Meaning
0	Operation not complete
1	Operation complete; no errors
2	Operation aborted

Problem Statement:

Acquire 100 data values using the sequential scan mode starting from channel 1 through channel 10. The time between each data input should be 25 microseconds. The BIC with device address 20_8 - 21_8 will be used for the data transfer.

Timing Diagram:



Programmed Solution:

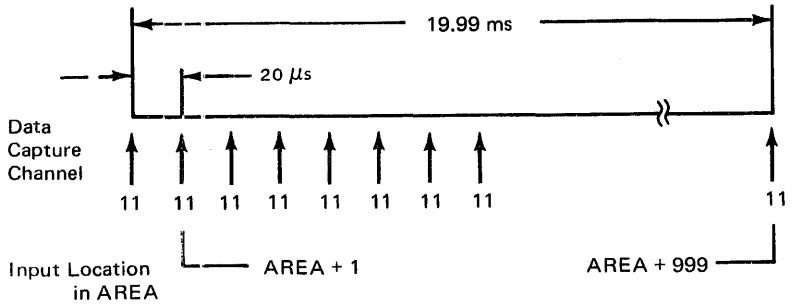
```
*INITIATE DATA TRANSFER
    CALL  DADC = 1, =0, =10, =25, =100, VECT, ERR
    ...
    ...    Concurrent processing
    ...

*WAIT FOR COMPLETION
WAIT    CALL SADC, STATE        CHECK STATUS
        LDA STATE               TEST STATUS WORD
        JAZ WAIT                IF 0 CONTINUE WAITING
        . . .
        . . .
STATE   DATA**.                 STATUS WORD
ERR     HLT                     HALT ON ERROR
VECT    BSS    100              RESERVE 100 WORDS
```

Figure 2-3. Direct Memory Transfer — Sequential Scan

Problem Statement:

Acquire 1000 points at the fastest possible rate from channel 11. The BIC with device address 24_8-25_8 should be used to accomplish the direct memory transfer.

Timing Diagram:



Programmed Solution:

```
* INITIATE DATA TRANSFER
          CALL DADC, = 3, M, = 11, T, = 1000, (BUFF)*, GOOF
          ...
* TEST FOR TRANSFER COMPLETION
NO        CALL SADC, FLAG
          LDA  FLAG
          JAZ  NO          WAIT FOR COMPLETION
          ...
GOOF      HLT              ERROR HALT
M         DATA 5           SELECT ONE CHANNEL INPUT
T         DATA 20          MIN TIME = 20 MICROSECONDS
FLAG      DATA**           STATE FLAG
BUFF      DATA (AREA)
AREA      BSS 1000         RESERVE 1000 WORDS
```

Figure 2-4. Direct Memory Transfer - Single Channel

2.7 TEST PROGRAMS

A set of test programs (binary paper tape, Part No. 03-994092) is provided for ADCM checkout. The set consists of six programs which may be selected through the Test Executive Program. The programs, numbered 0 through 6, are as follows:

Test No.	Description
0	Returns control to the Test Executive Program after performing other tests.
1	Reads one channel in random mode.
2	Reads N channels in sequential mode.
3	Reads N channels in random mode under timer control.
4	Reads one channel in random mode under BIC control.
5	Reads N channels in random mode under BIC control.
6	Tests timer.

These programs may be selected in any order and may be run as often as desired with different parameters. The device addresses of the modules need be entered only once but may be changed by re-entering the supervisor from the Test Executive Program.

Note that these tests accommodate a full complement of hardware consisting of the following modules: ADCM, Multiplexer, and BIC. The following table indicates which tests should be run with various hardware configurations.

	Test Number					
	1	2	3	4	5	6
ADCM, MUX, BIC	x	x	x	x	x	x
ADCM, MUX	x	x	x			x
ADCM, BIC	x			x		x
ADCM	x					x

The minimum computer configuration on which the tests may be run is a 620 or V-73 series computer with 4K of memory and a teletype or other terminal on device code 01.

An ADCM/MUX test shoe is required for running these tests. It can be purchased from Varian (Part No. 03-950399).

Supervisor Program

A simple supervisor or test program selector is provided as part of the test package to allow the user to select individual tests and return control to the Test Executive Program. The Test Executive Program is a standard Varian software option which must be loaded and run prior to initiation of the ADCM test package. Instructions for operating this program are given in the Test Program Manual. The ADCM test package is loaded through the Test Executive.

When the Test Executive Program is running, the "L." command may be used to load the test package and transfer control to its supervisor. If the test package is already loaded, the "G500." command may be used to transfer control to the supervisor.

When the supervisor is activated, it responds by issuing a carriage return/line feed and by starting to print a series of prompting messages. The user must enter a valid response to each message as it is printed. An invalid response causes the message to be repeated. The first message is:

ADC, MUX AND TIMER TEST SUPERVISOR
ENTER ADC-TIMER DEVICE ADDRESS?

The user must enter the assigned octal number between 060 and 067 followed by a period. The supervisor will then print:

ENTER MUX DEVICE ADDRESS?

The user must enter the assigned octal number between 040 and 077 followed by a period. The supervisor will then print:

ENTER BIC DEVICE ADDRESS?

The user must enter any of the following assigned octal numbers: 020, 022, 024, or 026 followed by a period.

The three device addresses entered at this time will be used throughout the six tests, where applicable. To change address selections, the supervisor must be reactivated from the Test Executive Program or run from location 500. After the device addresses have been entered, the supervisor will print:

ENTER TEST NO. ?

The user should enter any number between 0 and 6 followed by a period. The supervisor will then transfer control to the selected test program, which will request additional parameters and perform its specified functions.

Sense Switches

Throughout the operation of all ADCM tests, the sense switches may be used to perform special functions. The normal mode of operation is to reset all sense switches, but the following functions may be performed by setting the sense switches:

SS1	Sense switch 1 suppresses teletype printouts of test results and error messages. This function is useful to speed up the continuous execution of a test so that an oscilloscope may be used to monitor signals.
SS2	Sense switch 2 causes a test to repeat indefinitely without user intervention.

SS3 — Sense switch 3 terminates the execution of a test and returns control to the supervisor. If sense switch 3 is set when the supervisor requests a new test number, the following message will be printed:

RESET SENSE SWITCH 3

A new test may be selected after SS3 is reset.

Test Program Results

The same set of statistics is printed by the test programs for Tests 1, 2, 3, 4, and 5. After accepting the input readings, the test programs calculate and print the following items:

Minimum value in millivolts
Average value in millivolts
Maximum value in millivolts

The following frequency of occurrence readings are also calculated and printed:

Below (average value minus one count)
Average value minus one count
Average value
Average value plus one count
Above (average value plus one count)

In tests 2, 3, and 5, where several multiplexer channels are read, the statistics for odd and even numbered channels are calculated separately since their values are of opposite signs.

Test 1 — Read One Channel in Random Mode

In this test, the ADC is used to read a selected channel under program control in random mode 64 times. When the test program is activated, it will print:

ENTER CHANNEL NO. ?

The user should enter any channel number between 1 and 256 in decimal format followed by a period. Any other response will cause the message to be repeated. If no multiplexer is being used, any channel number may be entered since it will have no effect. In this case, the test signal must be connected directly to the ADC across pins J2-37 and J2-38.

The program acquires 64 input readings before printing the test statistics. Note that in all data printouts, the ADC quantizes the signal input at 2.4 millivolts per bit, but the printout omits references to fractional data. (In the 10-bit converter, ADC resolution is 19.5 millivolts per bit.)

Test 2 — Read N Channels in Sequential Mode

In this test, the ADC is used to read N sequential multiplexer channels. One word is read on each channel under program control and stored in a core buffer. The test statistics are printed on the teletype along with each channel reading. Using the test shoe, all odd numbered channels are wired together and all even numbered channels are wired together. Therefore, all even channels will have one reading and all odd numbered will have another. When the test program is activated, it will print:

ENTER NO. OF CHANNELS?

The user should enter any decimal number between 1 and 256 followed by a period to indicate the highest numbered channel. Any other response will cause the message to be repeated.

The program then reads the selected channels from channel 1 to the selected upper limit sequentially. The test results are printed first for the odd numbered channels and then for the even numbered channels. The value of each channel input is then printed eight readings per line. The first number of each line is the initial channel number on that line of print.

Test 3 — Read N Channels in Random Mode Under Timer Control

This test exercises the ability of the multiplexer to receive random channel addresses from the program and for the ADC to read the specified channels under program control. The timer is used to start an ADC conversion every 500 microseconds. A table of multiplexer channel addresses is used to direct the multiplexer selection. Each channel on a multiplexer card is read and stored into another core buffer for statistical reduction. The test will accommodate up to 16 cards having 16 channels each.

The test results are found for the odd and even numbered channels and are printed on the teletype. All readings that are not within plus or minus one count of the averages will be printed on the teletype.

To perform this test, a test shoe must be installed on all of the multiplexer cards being tested so that test voltages will be provided to all channels. The test shoe must be installed on J1 of the ADC to cause external ADC starts with the timer.

When the test program is activated, it will print:

ENTER NO. OF MUX CARDS?

The user should enter any decimal number between 1 and 16 followed by a period. Any other response will cause the message to be repeated. The program will read the data into the core buffer and list the odd statistics and then the even statistics. Then all channels which deviate by more than plus or minus one count from the average will be listed. The channels are listed in the order in which they are acquired. The odd numbered channels are read in ascending order interlaced with the even channels in descending order for each card one at a time. Card one will have the following channel selection sequence: 1, 16, 3, 14, 5, 12, 7, 10, 9, 8, 11, 6, 13, 4, 15, and 2.

Test 4 — Read One Channel in Random Mode Under BIC Control

This test program reads a specified channel on the multiplexer 64 times under BIC control. The 64 words are automatically transferred to a memory buffer via the BIC at the maximum ADC data conversion rate of 50 kHz (100 kHz for the 10-bit converter). The timer is used to initiate the acquisition of each word. The test results are printed at the conclusion of data acquisition.

Note that to cause external ADC starts with the timer, the special test shoe must be plugged into the ADC connecting J1-37 to J1-39 and J1-27 to J1-41.

When the program is activated, it will print:

ENTER CHANNEL NO. ?

The user should enter any decimal number between 1 and 256 followed by a period. Any other response will cause the message to be repeated. The program then reads the data, computes the results, and prints them on the teletype.

Test 5 — Read N Channels Random Mode Under BIC Control

This test exercises the ability of the multiplexer to receive random channel addresses under BIC control. Each time the ADC is started, the BIC transfers a new channel address to the multiplexer from a table of channel addresses in core. The channel is read by the ADC under program control and stored into a table in memory. The test program will accommodate up to 16 multiplexer cards having 16 channels each.

Note that a test shoe must be installed on all of the multiplexer cards being tested so that test voltages will be provided to all channels.

When the test program is activated, it will print:

ENTER NO. OF MUX CARDS?

The user should enter any decimal number between 1 and 16 followed by a period. Any other response will cause the message to be repeated. The program will read the data into the core buffer and list the odd statistics followed by the even statistics. Then all channels which deviate by more than plus or minus one count from the average will be listed. The channels are listed in the order in which they are acquired. The odd channels are read in ascending order interlaced with even channels in descending order for each card one at a time. Card one will have the following channel selection sequence: 1, 16, 3, 14, 5, 12, 7, 10, 9, 8, 11, 6, 13, 4, 15, and 2.

Test 6 — Timer Test

This test program checks the ADCM programmable timer. The test program sets the timer to time out every 50 milliseconds. The program counts 100 of these intervals and indicates the end of the cycle by ringing the teletype bell and printing an asterisk, "*". Six of these 5-second intervals are exercised. The last teletype bell should occur exactly 30 seconds after the test is started.

Note that the timer test runs twice as fast with the 10-bit ACDM. The teletype bell will ring every 2.5 seconds and the last bell should occur exactly 15 seconds after the test is started.

In order for the timer to run, it is necessary to install the special test shoe which connects ADC J1-27 to J1-41. This has the effect of connecting the 1 MHz oscillator to the counter. If an external time base is used, it should be connected at J1-41.

3. THEORY OF OPERATION

3.1 INTRODUCTION

The theory of operation presented in this section and in Section 4 assumes an ADCM with a 13-bit converter. The basic principles of operation are the same for the 10-bit version even though slight hardware differences exist between the two modules.

3.2 GENERAL THEORY

The amplitude of the analog input signal is represented to the computer in 16-bit binary two's complement by a 12-bit binary number and an extended sign bit. The value of the number is determined by bits 0 through 11 and the sign by bits 12 through 15. A logical 1 in bit positions 12 through 15 indicates that the number is negative, and a logical 0 indicates that the number is positive or zero.

> **NOTE**
>
> In this manual, logical 1 and logical 0 will each have two definitions. Their use is determined by where the signals appear; all logic signals that leave or enter the ADC are ground-true and all signals internal to the module are +5 Vdc-true.

	E-bus (nominal)	ADCM (nominal)
Logical 1	0 Vdc	+5 Vdc
Logical 0	+3 Vdc	0 Vdc

The binary value of each bit position is determined by the successive approximation technique. For each approximation, a comparison is made between a current proportional to the analog input voltage and the current generated in a ladder network. The successive approximation is carried out in 13 stages.

At State 1, the polarity of the input current sets the sign bit. At each of the succeeding stages, a new comparison is made that determines the binary level of the corresponding bit (logical 1 or logical 0). The level is determined by removing an amount of positive reference current that is proportional to the weighted value of the bit. If the polarity of the remaining current is still positive, the bit is set to 1; if the polarity is negative, the bit is set to 0 and the current that was removed is restored. After the thirteenth comparison is made, all 13 bits are set into the data buffer register, where they are stored until the next conversion is complete.

The following paragraphs provide a detailed discussion of the analog-to-digital conversion.

3.3 DETAILED THEORY

Figure 3-1 illustrates the principal elements responsible for carrying out the analog-to-digital conversion.

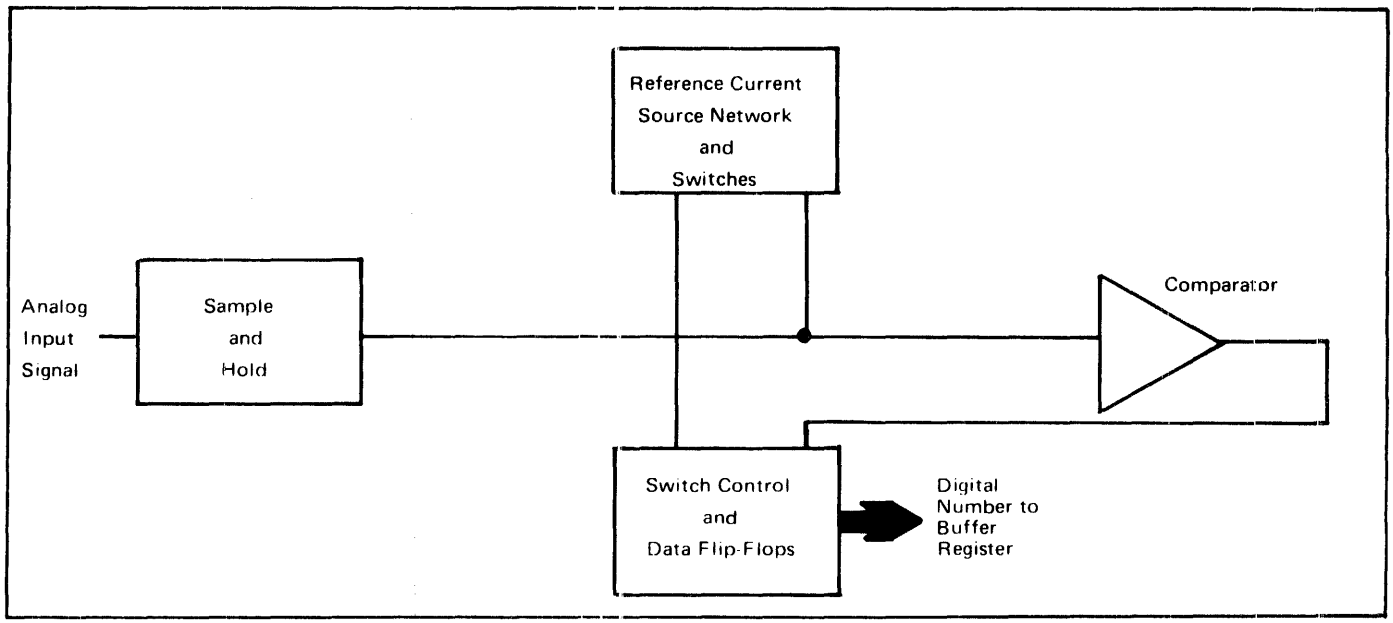


Figure 3-1. ADC Block Diagram

Reference Current and Switches

The reference current is provided to the summing junction by two stable reference voltage sources: -10 Vdc and +10 Vdc.

The negative reference current is provided through a partially variable resistor that is calibrated to match the positive reference current of bits positions 0 through 11. The negative reference current remains constant through all 13 stages of the conversion. The positive reference current is provided through 13 resistors, one for each bit position of the digital number. The resistor values are related in binary fashion, with the smallest resistor at bit position 12 (sign bit) and the largest at bit position 0 (least significant bit).

The current from the negative reference voltage offsets the summing junction by an equivalent of −9.9976 volts. The parallel resistance of the resistors for bit positions 0 through 11 is equivalent to the resistance of the negative reference resistor; thus, the resistor network for bits 0 through 11 will null the negative offset when all the switches controlling current through these resistors are closed.

During data conversion, current is provided to the summing junction by three sources: −10 Vdc reference, +10 Vdc reference, and the analog input voltage of unknown amplitude and polarity. The positive reference current is increased or decreased in an attempt to null the effect of the three voltages on the summing junction. If the analog input voltage is plus full scale (+9.9976 volts), it will exactly null the negative reference. All switches will be open by the end of the conversion, removing all positive reference current from the summing junction. If the analog input voltage is minus full scale (−10 volts), all positive reference current is needed to null the combined effect of the input voltage and the negative reference. All switches will be closed by the end of the conversion, adding full positive reference current to the summing junction.

Table 3-1 compares the bit values of ADCM binary output for key analog input values; the corresponding states of each bit switch and the octal and decimal values of the digital output are also shown.

The current through each bit position resistor is controlled by a current steering switch. Figure 3-2 illustrates a current steering switch for a single bit position.

When the flip-flop controlling the switch is set, diode CR1 is back biased and current through resistor R1 flows to the summing junction. If the flip-flop is reset, CR1 is forward biased and the reference current is steered through CR1 to the −15 Vdc sink.

Current provided by the analog input voltage is algebraically summed with the current provided by the positive and negative precision references.

This sum determines the polarity of the output of an inverting amplifier and comparator that are connected in series. (See Figure 3-2.) If the algebraic sum is positive, the output of the comparator will be a logical 1 and, if the sum is negative,

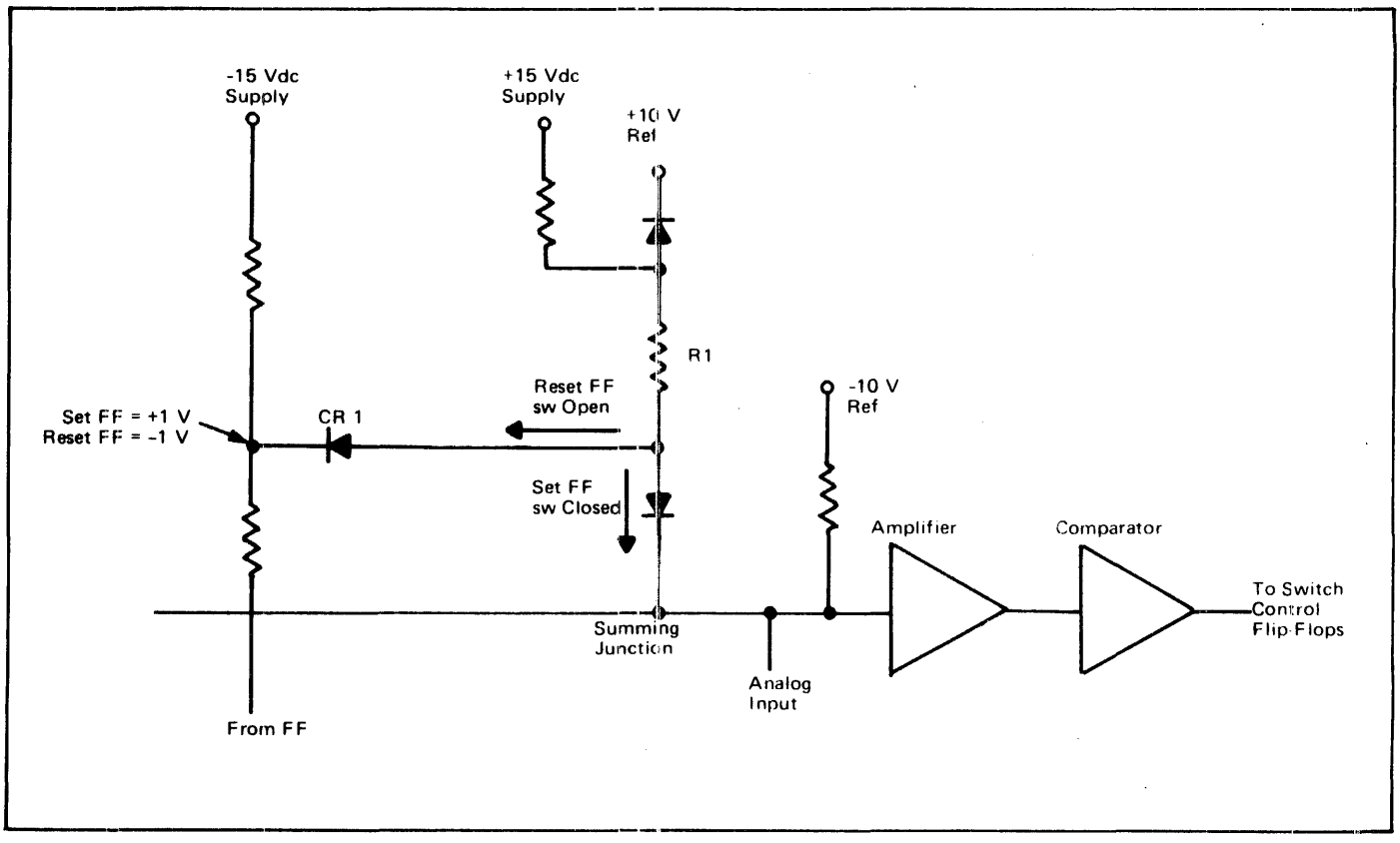


Figure 3-2. Current Steering Switch

the output will be a logical 0. The comparator output is buffered and applied to the D input of the set of flip-flops that control the current steering switches. The following paragraphs describe the logic that controls the current steering switches through a data conversion sequence.

Switch Control

A set of 13 D-type flip-flops and a 12-stage shift register form the heart of the logic that controls an analog-to-digital conversion. All the flip-flops, except flip-flop 2_0, open and close the current steering swtiches in the positive reference current source network. They also set logical 1's or 0's into the data buffer register. The flip-flops are controlled, in turn, by the shift register.

Between conversion operations, the flip-flops are prepared for the start of a new conversion. Relative high levels on Clk, Hold, Store and Sample cause flip-flops 2^1 through 2^{11} to be set and flip-flop 2^{12} to be reset. Flip-flop 2^0 is part of the data buffer register.

The Q output of those flip-flops that are set (high) close the current steering switches that they control. The Q output of a reset flip-flop (low) opens its switch. Consequently, before the start of a conversion, switch 12 (sign bit) is open and switches 0 through 11 are closed.

When the Start ADC logic is initiated (refer to Section 4), the signal Hold goes low and sets a logical 0 into position 11 of the shift register and logical 1's into positions 0 through 10. Busy and Clock go high when Hold goes low, with the trailing edge of Clock, the 0 set into position 11 of the shift register is clocked to the shift register's output and resets flip-flop 2^{11}. The Q output of flip-flop 2^{11} clocks flip-flop 2^{12}.

At this time, flip-flop 2^{12} is set or reset according to the logic level present at its D input. This input will be high if the analog input voltage has negative polarity and will be low if the analog input voltage has positive polarity.

If flip-flop 2^{12} is set, the sign bit switch is closed and a logical 0 will be set into bit position 12 (sign bit) of the data buffer register at the end of the conversion. If it is reset, the sign bit switch remains open and a logical 1 is set into position 12 of the buffer register at the end of the conversion.

When flip-flop 2^{11} resets, it also opens the switch in bit position 11. This removes the positive reference current contributed by that bit position. This initiates the second attempt at nulling the summing junction.

The trailing edge of the next clock pulse moves the 0 in the shift register to position 10, resetting flip-flop 2^{10}. The Q output of flip-flop 2^{10} clocks flip-flop 2^{11}. Flip-flop 2^{11} sets or resets according to the logic level present at its D input. If flip-flop 2^{11} sets, switch 11 closes and a logical 0 is set into position 11 of the data buffer register at the end of the conversion, If flip-flop 2^{11} resets, switch 11 remains open and a logical 1 is set into position 11 of the data buffer register at the end of the conversion. This sequence is repeated with the trailing edge of each clock pulse until flip-flop 2^{1} is reset.

The trailing edge of the last (twelfth) clock pulse in the conversion opens switch 0 directly (via two inverters) for the final approximation. Flip-flop 2^{0} is clocked by the transistion of the Start ADC logic from the conversion (Busy) state to the Sample state. This transition occurs when the last clock pulse generates the signal Store. When flip-flop 2^{0} is clocked, it sets or resets in the same manner as the other flip-flops in the sequence. Flip-flop 2^{0} is the buffer register for bit position 0 of the digital number.

Sample and Hold

The amplitude of the analog input voltage is continuously monitored between conversions by the sample circuit shown in sheet 1 of Appendix D. This circuit is capable of tracking a waveform of 20 volts peak-to-peak.

During the Sample period, the signals Sample and Hold, which originate in the Start ADC logic, are both high and test point 6 is low. This switches off transistors Q1 and Q2. With Q2 off, the field-effect transistor switches Q3 and Q4, which control the analog input to the storage capacitors, are conducting. As long as they are conducting, the voltage at the storage capacitors follows the input voltage.

When the Start ADC logic is set, Hold goes low and test point 6 goes high (sample goes low on the leading edge of the next clock pulse). This turns Q1 and Q2 on, switching Q3 and Q4 off. The voltage present at the storage capacitors at the instant Q3 and Q4 stop conducting is held during the Hold period.

During the Hold period, the stored potential in the capacitors provides the summing junction with a steady current that represents the input voltage. The period from the initiation of the conversion (Start ADC signal) to the time Q3 and Q4 are fully open is less than 100 nanoseconds. This period is called the aperture time. When the conversion cycle is complete, Q3 and Q4 close again. The time it takes the voltage level at the storage capacitors to reach the new analog input voltage level is called the recovery or acquisition time. The maximum recovery time for the Sample and Hold Circuit is 7 μs. This time would be required if the potential at the storage capacitor were at either plus or minus full scale when Q3 and Q4 closed and the input voltage were at the other end of the scale.

Power Supplies and Reference Voltages

Four regulated power supplies, +5 Vdc, +15 Vdc, −15 Vdc, and −22 Vdc are provided by circuits located on a power supply module.

The +10 Vdc and −10 Vdc precision reference voltages are provided by voltage regulators contained on the ADCM.

Output of the negative reference, as measured at test point 3, is within the range +8.5 Vdc to +9.5 Vdc. This output is stable to within $\pm$0.1 mV. Coarse and

fine adjustments set the amount of constant offset current provided to the summing junction by the negative reference. With all the switches open, this offset current is provided entirely by the output amplifier feedback loop, and the amplifier output voltage is at plus full scale.

Output of the plus reference source is +10 Vdc $\pm$ 0.1 mV. The feedback resistance of this circuit may be calibrated with both coarse and fine adjustment.

				COMPUTER INPUT AND SWITCH SETTINGS												
Scale Values				EB12 EB15	EB 11	EB 10	EB 09	EB 08	EB 07	EB 06	EB 05	EB 04	EB 03	EB 02	EB 01	EB 00
RANGE	DECIMAL	OCTAL	V_{in}	SW 12	SW 11	SW 10	SW 09	SW 08	SW 07	SW 06	SW 05	SW 04	SW 03	SW 02	SW 01	SW 00
+ Full Scale	+4095	007777	+ 9.9976	0	1	1	1	1	1	1	1	1	1	1	1	1
				0	0	0	0	0	0	0	0	0	0	0	0	0
+ Half Scale	+2048	004000	+ 5.0000	0	1	0	0	0	0	0	0	0	0	0	0	0
				0	0	1	1	1	1	1	1	1	1	1	1	1
+ 1 LSB	+1	000001	+ 0.0024	0	0	0	0	0	0	0	0	0	0	0	0	1
				0	1	1	1	1	1	1	1	1	1	1	1	0
0	0	000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0
				0	1	1	1	1	1	1	1	1	1	1	1	1
- 1 LSB	-1	177777	- 0.0024	1	1	1	1	1	1	1	1	1	1	1	1	1
				1	0	0	0	0	0	0	0	0	0	0	0	0
- Half Scale	-2048	174000	- 5.0000	1	1	0	0	0	0	0	0	0	0	0	0	0
				1	0	1	1	1	1	1	1	1	1	1	1	1
- Full Scale +1	-4095	170001	- 9.9976	1	0	0	0	0	0	0	0	0	0	0	0	1
				1	1	1	1	1	1	1	1	1	1	1	1	0
- Full Scale	-4096	170000	-10.000	1	0	0	0	0	0	0	0	0	0	0	0	0
				1	1	1	1	1	1	1	1	1	1	1	1	1

Table 3-1. ADC Output Scale

4. I/O INTERFACE THEORY OF OPERATION

4.1 PROGRAM CONTROLLED DATA TRANSFER

Program controlled data transfer in operations occur in three stages:

A. Start ADC – An EXC instruction starts the ADC and an analog-to-digital conversion cycle takes place.

B. Data Sense – A Sense instruction tests for the availability of a new data word.

C. Data Transfer In – A data transfer in instruction is executed.

The ADCM logic involved in these stages of a data transfer operation is described in the following paragraphs.

Start ADC

The program instruction EXC 01YY sets the appropriate device address on E-bus lines EB00 through EB05, places function code 1 on EB06 through EB08, and places a logical 1 on EB11. The control pulse, FRYX, then strobes the function code into the function decode logic.

The decode logic output $\overline{\text{EXC1}}$ is selected and sets the Hold flip-flop. The low Q output of this flip-flop causes the control switches in the Sample and Hold circuit to be turned off, capturing the instantaneous analog input voltage.

On the next leading edge of a clock pulse, the Sample/Busy flip-flop resets. The high Busy output gates clock pulses into the shift register that sequences the ADC logic through the conversion cycle.

Each succeeding clock pulse causes a bit (logical 1 or logical 0) to be set into the control flip-flop register. The last clock pulse in the conversion sequence generates a Store pulse, indicating that the data word is complete and is being stored.

The Store pulse conditions the Sample/Busy flip-flop to be set with the trailing edge of the clock pulse that generated Store. When this flip-flop sets, the low-to-high transition of Sample clocks the least significant bit into its latch.

Data Sense

The leading edge of Store sets the Data Sense flip-flop. Data Sense conditions the Sense 0 gate in preparation for a Sense 0 instruction from the program.

When the program issues a Sense 0 instruction, the function decode logic selects the line Select 0.

This enables the Sense 0 gate, providing a logical 1 to the SERX line on the I/O bus. The Data Sense flip-flop remains set until a data transfer in operation is completed.

Data Transfer

The program executes a data transfer in operation from an ADCM with one of the assembler data transfer-in instructions (refer to Section 2). The ADCM is selected and a logical 1 on EB13 sets the DTIS (Data Transfer In) flip-flop. DTOS (Output Enable) gates the contents of the data buffer register onto the E-bus lines EB00 through EB15. EB00 through EB11 carry the data bits, with the least significant bit on EB00 and the most significant bit on EB11. The sign bit is gated onto EB12 through EB15 via four line drivers. This is done to accommodate the 13-bit data word format to the 16-bit format required by the computer.

Output Enable resets the Data Sense flip-flop in preparation for a new conversion sequence.

4.2 BIC CONTROLLED DATA TRANSFER

BIC-controlled data transfer in operations may be started by the program, the programmable timer, or EXT Start.

If the program is used to start the ADC, the EXC 01YY instructions will occur at intervals determined by program delays or from sensing the timer. If the output of the timer is used, J1-37 must be connected to J1-39, or optionally, jumper 5 must be installed.

For timer starts or external starts, the data transfer operation must be preceded by an EXC 02YY instruction to set the Program flip-flop. This places the clock input to the Hold flip-flop under the influence of either the timer output or Ext Start.

An EXC 02YY instruction is followed by an EXC 0YY instruction. This sets the BIC Enable flip-flop, preparing the ADCM's BIC interface logic to be connected to the BIC. The ADCM is connected to the BIC when DCEX from the BIC sets the Connected flip-flop. When the BIC receives the output of the Connected flip-flop, CDCX, indicating that the ADCM has been connected, it resets DCEX. The Connected flip-flop remains set, however, until the BIC requests a disconnect by issuing DESX.

The logic remains in this state until the Data Sense flip-flop is set at the end of a conversion. When Data Sense goes true, the output of the Connected flip-flop is gated through to the BIC as TRQX. This pulse requests the BIC to transfer the data word just converted to the computer. The BIC responds to TRQX and TAKX, which results in the data gating signal, Output Enable.

The sequence is repeated each time a new Start ADC signal initiates another conversion cycle. When Data Sense again goes true, the data transfer phase begins. The BIC interrupts the sequence by resetting the Connected flip-flop with DESX.

When the Connected flip-flop resets, the low-to-high transition of its Q output resets the BIC Enable and Program flip-flops.

4.3 PROGRAMMABLE TIMER

The programmable timer consists of a 16-bit down counter and a buffer register. The counter decrements from some number provided by the computer program until

the contents of the counter equal zero. At zero, a 100 nanosecond negative going pulse called TMR is generated.

The 16-bit starting number is transferred to the buffer register on EB00 through EB15 with a data transfer out operation. The data transfer must be under program control.

At the start of a data transfer out operation, the ADCM is selected with its device address; Function Select and EB14 set the DTOS flip-flop. The program sets the output word on the E-bus and loads it into the timer buffer register with control pulse DRYX.

One-microsecond (0.5-microsecond in 10-bit version) clock pulses cause the timer to count to zero and generate a TMR pulse. When operating in a continuous mode, the pulse gates the starting number from the buffer register into the timer and the count begins again. In the single-cycle mode, the EXT TMR Control jumper is connected, a relative high level is then required on the EXT TMR Control input to reload the timer. After the timer is reloaded, EXT TMR Control returns to ground.

Timer Sense

The TMR pulse also resets the Timer Sense flip-flop. Output of the Timer Sense flip-flop conditions the Sense 1 flip-flop to be set by a Sense 1 instruction from the program.

The output of the Sense 1 flip-flop goes true with the trailing edge of the Sense 1 instruction. This indicates to the program that the timer has counted to zero but prevents that signal from reaching the computer until the computer is ready to receive it. This synchronizing is necessary to avoid starting a signal race in the computer logic.

The TMR Sense and Sense 1 flip-flops are both reset the next time a new starting number is loaded into the timer.

5. INSTALLATION

5.1 PREREQUISITES

Each ADCM requires one card slot in either the mainframe or Memory Expansion/Peripheral Controller frame. No special slots are reserved for use by ADCM; its location in the frame is determined solely by considerations of convenience in backplane wiring.

A Power Supply Module (Part No. 620-88) must be installed when using an ADCM. If a Power Supply Module has been previously installed and sufficient current is available, an additional module need not be installed.

5.2 INSTALLATION AND INTERCONNECTION

An ADCM is installed vertically, with its component side to the installer's left in 620/i and 620/L computers, and horizontally in the 620/f computer. Figure 5-1 illustrates a typical installation.

> **CAUTION**
>
> Do not install ADCMs in slots that have been previously wired for power; if the intended slot is already wired, remove any connections to power before installing the ADCM to protect its components. Refer to Table 5-1 for proper power connections.

The card is installed with the double pin edge pointing toward the installer. Proper orientation is important since the cards are not keyed.

Connection to the computer I/O-bus and to the BIC option B-bus is provided through backplane wiring. All pin assignments for I/O-bus and B-bus are listed in Appendix B of this manual.

Connections to external instruments include, for each ADCM, one analog signal input, one external sense input, and one programmable timer pulse output. Connector pins are also available for external control inputs to the ADC start logic and the programmable timer. Pin assignments for these connections are also listed in Appendix B. Recommended connector types for J1 and J2 are identified in the summary of key specifications in Appendix C.

Power Supply Wiring

Connections to the ADCM must be made for four power supply voltages and senses, an analog ground, a digital ground, and digital ground sense. Table 5-1 lists the pin assignments on the ADCM wirewrap backplane for these connections. When the ADCM is used with other modules (AOMs, MUXs, etc.) similar voltages should be tied together, and the voltage sense line should be brought from the midpoint of the voltage tie-line to a voltage sense line on the power supply wirewrap backplane. The voltage and sense points for the power supply backplane are given in the Power Supply Manual (Publication No. 03-996-812). This manual also contains detailed information regarding power supply checkout.

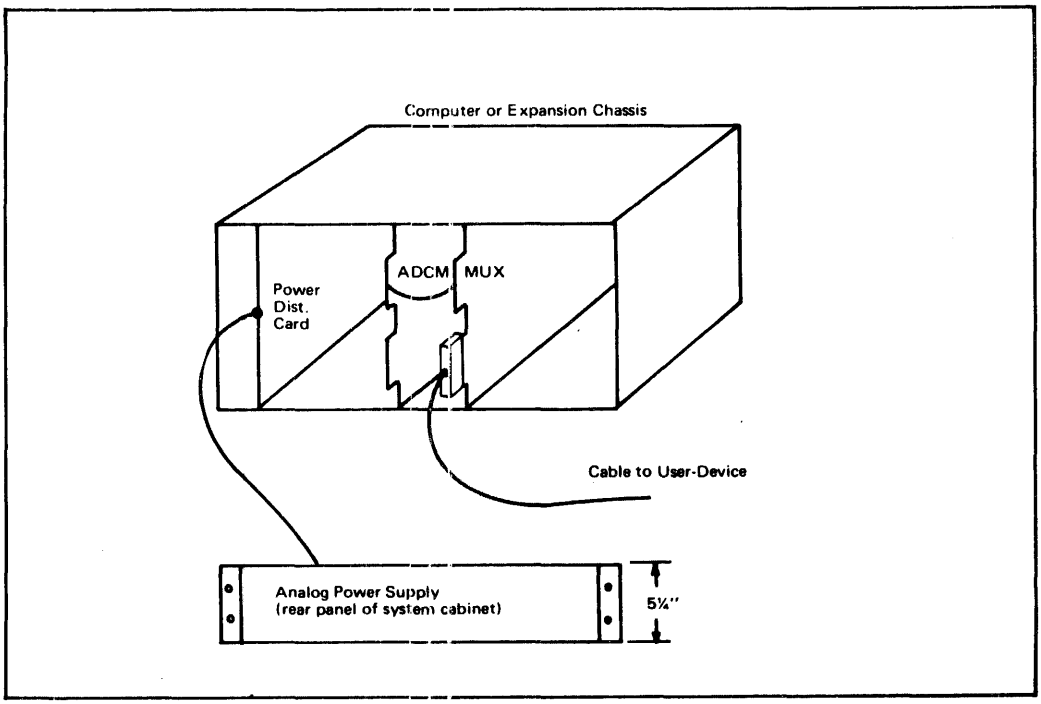


Figure 5-1. Typical Module Installation

Table 5-1. ADCM Wirewrap Backplane Pin Connections for Power Supply

Power Supply Voltage	ADCM Pins
Digital Ground	P1-1, 22, 48, 51, 100, 122, and J1-2
+ 5 Vdc	P1-118, 121
+15 Vdc	P1-111
−15 Vdc	P1-113
−22 Vdc	P1-109
Analog Ground	P1-115

Device Address Wiring

Table 5-2 lists the jumper connections required to wire a device address for an ADCM. Note that P1-74 (Enable) is not normally used. It is available, however, and may be used as an additional addressing condition. For example, if two ADCM modules have the same device address, the Enable input can be used to permit only one module to respond to that address at a given time.

Table 5-2. Device Address Wiring

Address	Wire Wrap Jumpers		
060	P1-71 to P1-72	P1-68 to P1-69	P1-65 to P1-66
061	P1-71 to P1-72	P1-68 to P1-69	P1-64 to P1-66
062	P1-71 to P1-72	P1-67 to P1-69	P1-65 to P1-66
063	P1-71 to P1-72	P1-67 to P1-69	P1-64 to P1-66
064	P1-70 to P1-72	P1-68 to P1-69	P1-65 to P1-66
065	P1-70 to P1-72	P1-68 to P1-69	P1-64 to P1-66
066	P1-70 to P1-72	P1-67 to P1-69	P1-64 to P1-66
067	P1-70 to P1-72	P1-67 to P1-69	P1-64 to P1-66

PIM Wiring

If the computer has the PIM option, then interrupts may be provided by wiring P1-84 to the PIM to enable an interrupt at the completion of an analog-to-digital conversion, and by wiring P1-73 to the PIM to enable an interrupt at the completion of a timer interval.

5.3 INSTALLATION EXAMPLE

Frequently, an ADCM is installed in conjunction with a Multiplexer Module. The following example illustrates typical steps involved in wiring a system which consists of an ADCM, a 16-channel MUX, and a Power Supply Module. These steps are:

1. Wire ADCM and MUX Power Supply
2. Wire ADCM device address
3. Wire MUX device address
4. Wire MUX channel address for 16-channel operation
5. Wire MUX output to ADCM
6. Attach analog input cable to MUX

The interconnections involved in Steps 1 through 4 are shown in Tables 5-3 through 5-5. Step 5 is shown in Figure 5-2, and Step 6 is shown in Figure 5-3. More detailed information on MUX installation may be found in the Multiplexer Manual. Note that to simplify backplane wiring, the ADCM and MUX should be installed in adjacent card slots.

DC Power

The wirewrap interconnections for the power supply for this sample configuration are shown in Table 5-3.

Table 5-3. Typical Power Supply Wiring

From Power Supply Patchboard		To ADC	To MUX
+15 V	P1-102	P1-111	P1-111
-15 V	P1-106	P1-113	P1-113
+20 V	P1-75		P1-107
-22 V	P1-79	P1-109	P1-109
+5 V	P1-89	P1-118	
+5 V	P1-90		P1-118
AGND	P1-111	P1-115	
AGND	P1-112		P1-115
DGND	P1-97	P1-122	
DGND	P1-98		P1-122

Device Address

In this example the ADCM is assigned device address 60_8, and the MUX is assigned device address 61_8, as shown in Table 5-4.

Table 5-4. Typical Device Address Assignments

Signal Name	ADC to ADC		MUX to MUX	
EB-0	P1-65	P1-66		
EB-1	P1-68	P1-69		
EB-2	P1-71	P1-72		
EB-0			P1-65	P1-66
EB-1			P1-68	P1-69
EB-2			P1-71	P1-72
EB-3			P1-74	P1-78
EB-4			P1-77	P1-78

MUX Channel Addresses Wiring

The MUX channel address jumpers for 16-channel operation are shown in Table 5-5.

Table 5-5. Wirewrap Jumpers for 16-Channel MUX Operation

Signal Name	MUX to MUX		ADC
Decode-0	P1-91	P1-80	
Decode-1	P1-93	P1-81	
BUSY		P1-101	P1-75

MUX Output to ADCM

The MUX output signal is provided by means of a shielded twisted pair cable from the MUX to the ADCM, as shown in Figure 5-2.

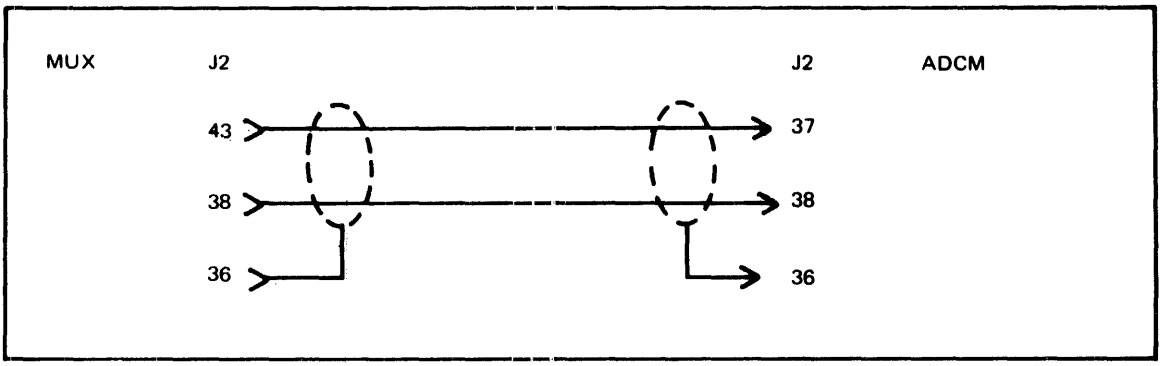


Figure 5-2. MUX Output to ADCM

Analog Input Wiring

Figure 5-3 shows typical input wiring where differential input leads are connected to MUX J1-9 (high) and J1-7 (low) and the ground line is connected to J1-8 (analog ground).

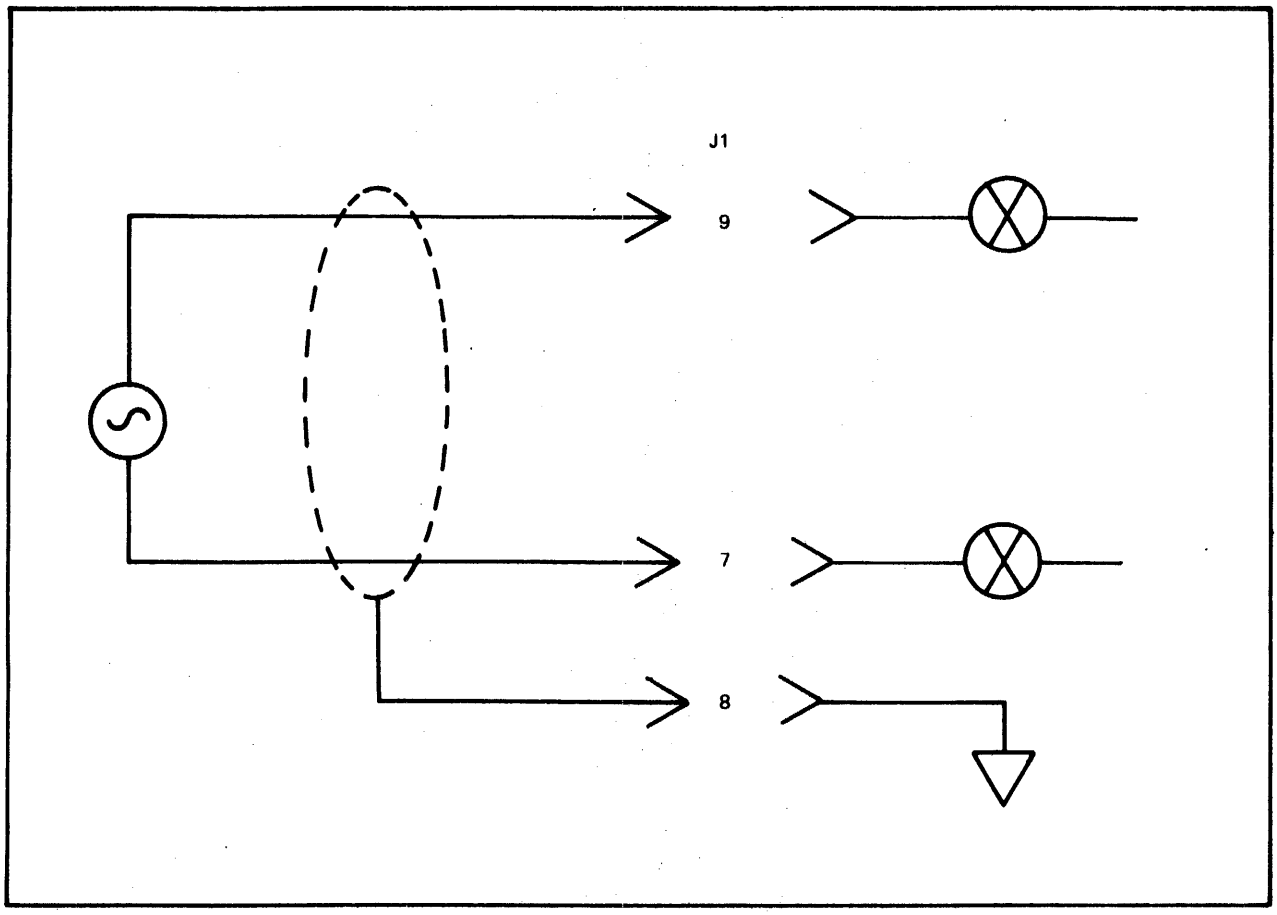
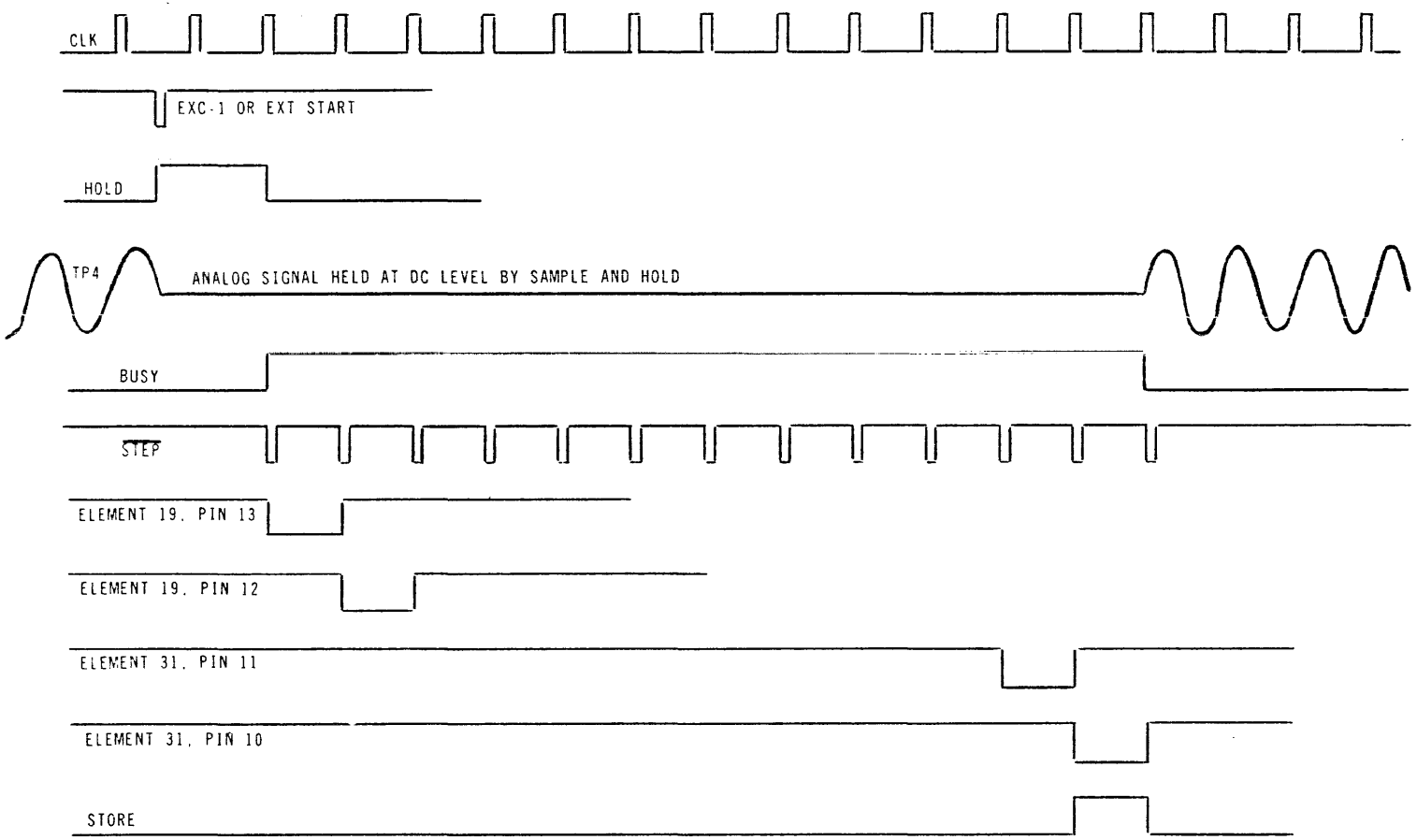


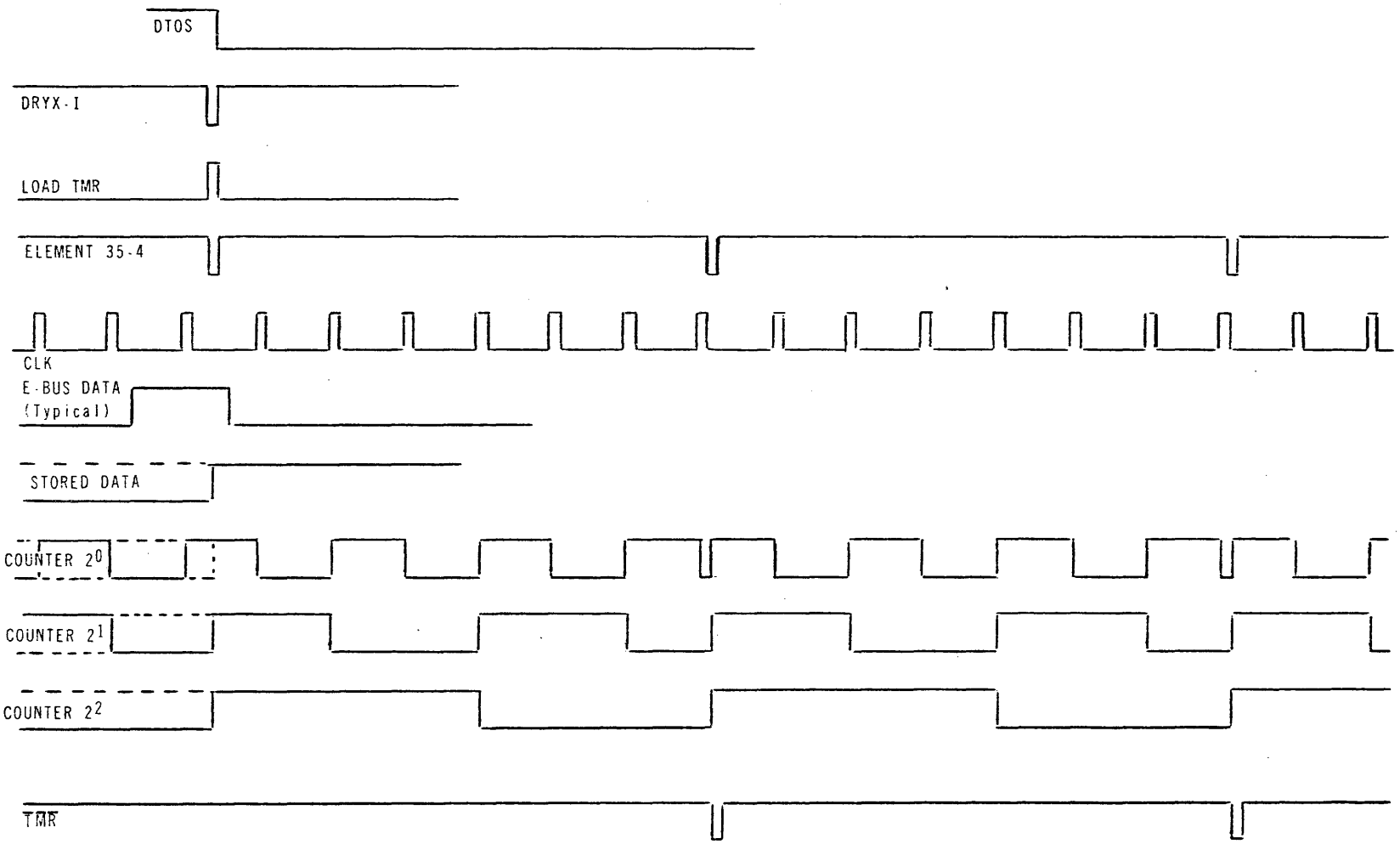
Figure 5-3. Differential Input Connections to MUX

APPENDIX A

TIMING DIAGRAMS



Timing Diagram: ADC Module



NOTE: In this example, the Timer is loaded with a count of 7 and subsequently emits a pulse every 7 μSEC

APPENDIX B

ADCM PIN ASSIGNMENTS

BACKPLANE WIRING

Pin No.	Name	Name Function
P1-1	Digital Ground	Digital Ground
-2	EB00-I	EB00-I One bit of device address, timer word or data word
-3	Digital Ground	Digital Ground
-4	EB01-I	EB01-I One bit of device address, timer word or data word
-5	Digital Ground	Digital Ground
-6	EB02-I	EB02-I One bit of device address, timer word or data word
-7	Digital Ground	Digital Ground
-8	EB03-I	EB03-I One bit of device address, timer word or data word
-9	Digital Ground	Digital Ground
-10	EB04-I	EB04-I One bit of device address, timer word or data word
-11	EB05-I	EB05-I One bit of device address, timer word or data word
-12	EB06-I	EB06-I One bit of EXC or SEN code, timer word or data word
-13	EB07-I	EB07-I One bit of EXC or SEN code, timer word or data word
-14	EB08-I	EB08-I One bit of EXC or SEN code, timer word or data word
-15	EB09-I	EB09-I One bit of timer word or data word
-16	EB10-I	EB10-I One bit of timer word or data word
-17	EB11-I	EB11-I One bit of timer word or data word
-18	EB12-I	EB12-I One bit of timer word or sign bit
-19	EB13-I	EB13-I One bit of timer word or sign bit
-20	EB14-I	EB14-I One bit of timer word or sign bit
-21	EB15-I	EB15-I One bit of timer word or sign bit
-22	Digital Ground	Digital Ground
-23	Not used	Not used
-24	Digital Ground	Digital Ground
-25	Not used	Not used
-26	Digital Ground	Digital Ground
-27	FRYX-I	FRYX-I Device address tag line
-28	Digital Ground	Digital Ground
-29	DRYX-I	DRYX-I Gates timer word into buffer register
-30	Digital Ground	Digital Ground

BACKPLANE WIRING (Cont.)

Pin No.	Name	Name Function
P1-31	SERX-I	SERX-I Sense input to computer
-32	Digital Ground	Digital Ground
-33	Not used	Not used
-34	Digital Ground	Digital Ground
-35	Not used	Not used
-36	Digital Ground	Digital Ground
-37	Not used	Not used
-38	Digital Ground	Digital Ground
-39	Not used	Not used
-40	Digital Ground	Digital Ground
-41	Not used	Not used
-42	Not used	Not used
-43	SYRT-I	SYRT-I Resets system logic
-44	IUAX-I	IUAX-I Interrupt acknowledge from computer
-45	Not used	Not used
-46	Not used	Not used
-47	Not used	Not used
-48	Digital Ground	Digital Ground
-49	TRQX-B	TRQX-B Transfer request from ADCM to BIC
-50	Not used	Not used
-51	Digital Ground	Digital Ground
-52	Not used	Not used
-53	Digital Ground	Digital Ground
-54	CDCX-B	CDCX-B Notifies BIC that ADCM is connected
-55	Digital Ground	Digital Ground
-56	DCEX-B	DCEX-B Connect signal from BIC
-57	Digital Ground	Digital Ground
-58	TAKX-B	TAKX-B Transfer request acknowledge from BIC
-59	Digital Ground	Digital Ground
-60	DESX-B	DESX-B Disconnect from BIC
-61	Not used	Not used
-62	Not used	Not used
-63	Not used	Not used
-64	EB00 +	EB00 + Jumper connection for wiring device address
-65	EB00-	EB00 - Jumper connection for wiring device address
-66	EB0I +	EB0I + Jumper connection for wiring device address
-67	EB01 +	EB01 + Jumper connection for wiring device address
-68	EB01-	EB01 - Jumper connection for wiring device address
-69	EB1I +	EB1I + Jumper connection for wiring device address
-70	EB02 +	EB02 + Jumper connection for wiring device address

BACKPLANE WIRING (Cont.)

Pin No.	Name	Name Function
P1-71	EB02	EB02 Jumper connection for wiring device address
-72	EB2I +	EB2I + Jumper connection for wiring device address
-73	TIMER OUT	TIMER OUT For external use of timer
-74	ENABLE	ENABLE Not normally used
-75	BUSY	BUSY Notifies multiplexer that ADC is converting
-76	Not used	Not used
-77	Not used	Not used
-78	Not used	Not used
-79	Not used	Not used
-80	Not used	Not used
-81	Not used	Not used
-82	Not used	Not used
-83	OUTPUT ENABLE	OUTPUT ENABLE Gates data onto E-bus
-84	STORE	STORE Indicates that conversion is complete
-85	DTOS	DTOS Timer word transfer request to computer
-86	Not used	Not used
-87	CLK	CLK For external use of CLK pulses
-88	Not used	Not used
-89	DTIS	DTIS Request to transfer data to computer
-90	Not used	Not used
-91	Not used	Not used
-92	Not used	Not used
-93	Not used	Not used
-94	Not used	Not used
-95	Not used	Not used
-96	Not used	Not used
-97	Not used	Not used
-98	Not used	Not used
-99	Not used	Not used
-100	Digital Ground	Digital Ground
-101	ERR	ERR Sets Data Sense condition
-102	Not used	Not used
-103	Not used	Not used
-104	Not used	Not used
-105	Not used	Not used
-106	Not used	Not used
-107	Not used	Not used
-108	Not used	Not used
-109	-20 Vdc	-20 Vdc
-110	Not used	Not used

Pin No.	Name	Name Function
P1-111	+15 Vdc	+15 Vdc
-112	Not used	Not used
-113	-15 Vdc	-15 Vdc
-114	Not used	Not used
-115	Analog Ground	Analog Ground
-116	Not used	Not used
-117	Not used	Not used
-118	+5 Vdc	+5 Vdc
-119	Not used	Not used
-120	Not used	Not used
-121	+5 Vdc	+5 Vdc
-122	Digital Ground	Digital Ground

TERMINAL EDGE CONNECTOR WIRING

Pin No.	Name	Name Function
J1-1	Not used	Not used
-2	Digital Ground	Digital Ground
-3	Not used	Not used
-4	Digital Ground	Digital Ground
-5	Not used	Not used
-6	Digital Ground	Digital Ground
-7	Not used	Not used
-8	Digital Ground	Digital Ground
-9	Not used	Not used
-10	Digital Ground	Digital Ground
-11	Not used	Not used
-12	Digital Ground	Digital Ground
-13	Not used	Not used
-14	Digital Ground	Digital Ground
-15	Not used	Not used
-16	Digital Ground	Digital Ground
-17	Not used	Not used
-18	Digital Ground	Digital Ground
-19	Not used	Not used
-20	Digital Ground	Digital Ground
-21	Not used	Not used
-22	Digital Ground	Digital Ground
-23	Not used	Not used
-24	Digital Ground	Digital Ground
-25	Not used	Not used

TERMINAL EDGE CONNECTOR WIRING (Cont.)

Pin No.	Name	Name Function
J1-26	Digital Ground	Digital Ground
-27	2°	2°
-28	Digital Ground	Digital Ground
-29	Not used	Not used
-30	Digital Ground	Digital Ground
-31	Not used	Not used
-32	Digital Ground	Digital Ground
-33	Not used	Not used
-34	Digital Ground	Digital Ground
-35	EXT SEN	EXT SEN Input connection for EXT SEN line
-36	Digital Ground	Digital Ground
-37	EXT START	EXT START Input connection for EXT START line
-38	Digital Ground	Digital Ground
-39	Timer Out	Timer Out Output connection for timer pulses
-40	Digital Ground	Digital Ground
-41	EXT TMR CNTL	EXT TMR CNTL Input connection for EXT TMR CNTL line
-42	Digital Ground	Digital Ground
-43	Not used	Not used
-44	Digital Ground	Digital Ground
J2-1	Not used	Not used
-2	Analog Ground	Analog Ground
-3	Not used	Not used
-4	Analog Ground	Analog Ground
-5	Not used	Not used
-6	Analog Ground	Analog Ground
-7	Not used	Not used
-8	Analog Ground	Analog Ground
-9	Not used	Not used
-10	Analog Ground	Analog Ground
-11	Not used	Not used
-12	Analog Ground	Analog Ground
-13	Not used	Not used
-14	Analog Ground	Analog Ground
-15	Not used	Not used
-16	Analog Ground	Analog Ground
-17	Not used	Not used
-18	Analog Ground	Analog Ground
-19	Not used	Not used
-20	Analog Ground	Analog Ground
-21	Not used	Not used
-22	Analog Ground	Analog Ground

TERMINAL EDGE CONNECTOR WIRING (Cont.)

Pin No.	Name	Name Function
J2-23	Not used	Not used
-24	Analog Ground	Analog Ground
-25	Not used	Not used
-26	Analog Ground	Analog Ground
-27	Not used	Not used
-28	Analog Ground	Analog Ground
-29	Not used	Not used
-30	Analog Ground	Analog Ground
-31	Not used	Not used
-32	Analog Ground	Analog Ground
-33	Not used	Not used
-34	Analog Ground	Analog Ground
-35	Not used	Not used
-36	Analog Ground	Analog Ground
-37	SIG +	SIG + Input connection for + analog signal
-38	Analog Ground	Analog Ground
-39	Not used	Not used
-40	Analog Ground	Analog Ground
-41	Not used	Not used
-42	Analog Ground	Analog Ground
-43	SIG -	SIG - Input connection for - analog signal
-44	Analog Ground	Analog Ground

APPENDIX C: SPECIFICATIONS

ANALOG-TO-DIGITAL CONVERTER

Resolution	13 binary bits 10 binary bits
Output Format	Two's complement
Conversion Accuracy	± 0.012% of full scale, ± 1/2 LSB (13-bit) ± 0.05% of full scale, ± 1/2 LSB (10-bit)
Conversion Time	10 μsec, maximum (13-bit) 5 μsec, maximum (10-bit)
Temperature Coefficient	± 50 mV/°C, maximum
Warm-Up Time	Essentially zero
Full Scale Range	± 10 V
Digital Outputs	
BUSY	High (true) during Analog-to-Digital conversion. Available fanout: 8 logic loads. Maximum capacitive load: 100 pF.
STORE	Low (true) during last 1 μsec of the BUSY signal. Available fanout: 10 logic loads. Maximum capacitive load: 1000 pF.
Output Enable	High (true) during the time ADC data is on the E-Bus (1.90 μ sec). Available fanout: 20 logic loads. Maximum capacitive load: 100 pF.
Digital Inputs	
EXT START	1 kΩ to +5 V; low true sense input. Computer may test the status of this input with a SEN 2YY instruction.
EXT SENSE	5.6 kΩ to + 5 V; low true sense input. Computer may test the status of this input with a SEN 2YY instruction.

PROGRAMMABLE TIMER

Clock Frequency	1.0 MHz ± 0.01% (13-bit) 2.0 MHz ± 0.01% (10-bit)

Clock Drift	± 1 PPM/°C
Clock Stability	± 0.01 PPM/day
Resolution	16 binary bits (computer E-Bus $2^0 - 2^{15}$)
Programmed PRF	1 MHz to 15.26 Hz (13-bit) 2 MHz to 30.52 Hz (10-bit) 1 μsec to 65.535 milliseconds (13-bit) 0.5 μsec to 32.767 milliseconds (10-bit)
Timer Output	100 nanosecond pulse to ground. 1 kΩ to + 5 V sinks 100 mA. Maximum capacity load 1000 pF.
CLK Output	100 nanosecond pulse from low to high. TTL output. Available fanout: 6 logic loads. PRF = 1.0 MHz ± 0.01% (13-bit) 2.0 MHz ± 0.01% (10-bit)
Timer Clock Input	1 TTL load. Maximum PRF = 10 MHz. Increments counter on low to high position.

SAMPLE AND HOLD

Gain and Accuracy	
Voltage Gain	+1
Accuracy	± 0.01% of FS
Gain Temperature Coefficient	± 10 PPM/°C
Track Mode, Single Ended	
Full Power Sine Wave	65 kHz
Slew Rate	4 V/μsec
Settling Time to	± 1 mV, 4 μsec
Track Mode, Differential	
Full Power Sine Wave	15 kHz
Slew Rate	1/μsec
Settling Time to	± 1 mV, 30 μsec
Input Characteristics, Single Ended	
Single Range	± 10 V
Maximum Rating (without damage)	± 15 V

Input Impedance	50 kΩ in parallel with 5000 pF.
Offset Voltage	± 2 mV maximum
VS Temperature	± 50 mV/°C
Input Characteristics, Differential	
Signal Range	± 10 V
Maximum Rating (without damage)	± 30 V
Input Impedance	50 kΩ
Common Mode Rejection	80 dB, 0 to 60 Hz
Offset Voltage	± 2 mV, maximum
VS Temperature	± 100 mV/°C
Output Characteristics	
Signal Range	± 10 V
Noise, RMS Wideband (hold mode)	± 1 mV peak-to-peak
Decay Rate in, hold mode	± 10 mV/sec
Feedthrough 20 V Step (hold mode)	- 80 dB
Switching Characteristics	
Aperture Time, Maximum	100 nanoseconds
Offset Pedestal, Maximum	± 2 mV
Acquisition Time, Maximum	6 μsec

POWER

+15 Vdc ± 0.1%; 150 mA
-15 Vdc ± 1% ; 150 mA
-22 Vdc ± 2%; 2 mA
+5 Vdc ± 5%; 1275 mA

TEMPERATURE RANGE

Specification	0° to 50°C
Operating	-10° to 70°C
Storage	-55° to 85°C

PHYSICAL CHARACTERISTICS

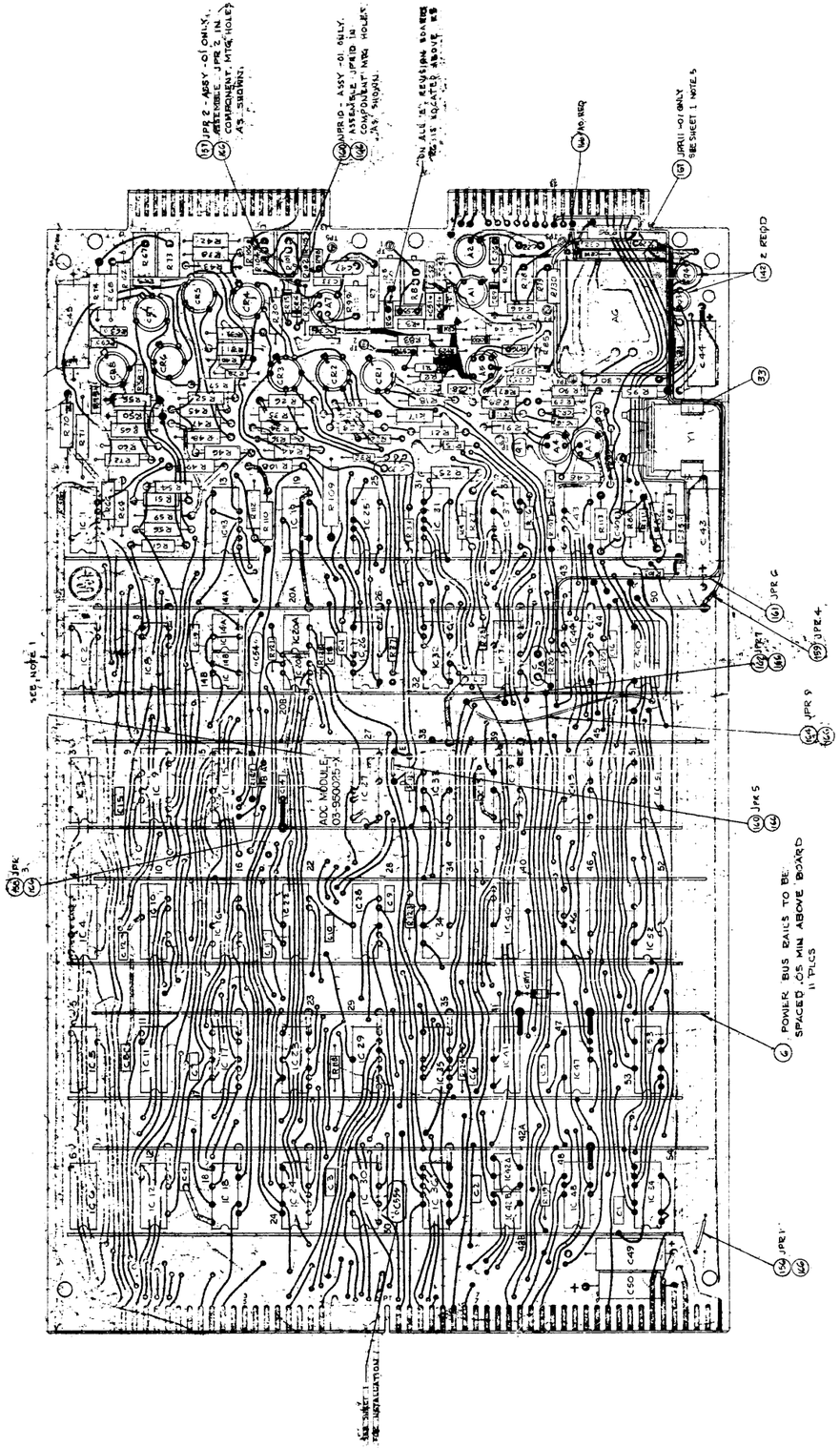
Dimensions	One printed circuit board 7-3/4 x 12 x 1/2 inches
Connectors	Two 44-terminal card edge connectors One 122-terminal card edge connector

MODULE PERFORMANCE SUMMARY

Accuracy	± 0.025% of FS
Accuracy (with Multiplexer)	± 0.040% of FS
Throughput Rate	55 kHz, maximum (13-bit) 105 kHz, maximum (10-bit)
Throughput Rate (with Multiplexer)	50 kHz, maximum (13-bit) 100 kHz, maximum (10-bit)

APPENDIX D

SCHEMATICS, ASSEMBLIES AND PARTS LISTS


ADC MODULE
03-950095-X
SEE NOTE 1
SEE SHEET 1 FOR INSTALLATION
POWER BUS RAILS TO BE SPACED .05 MIN ABOVE BOARD
11 PLCS
MARK ALL BLACK DASHED CURRENT ASSY REV LETTER
NOTES:

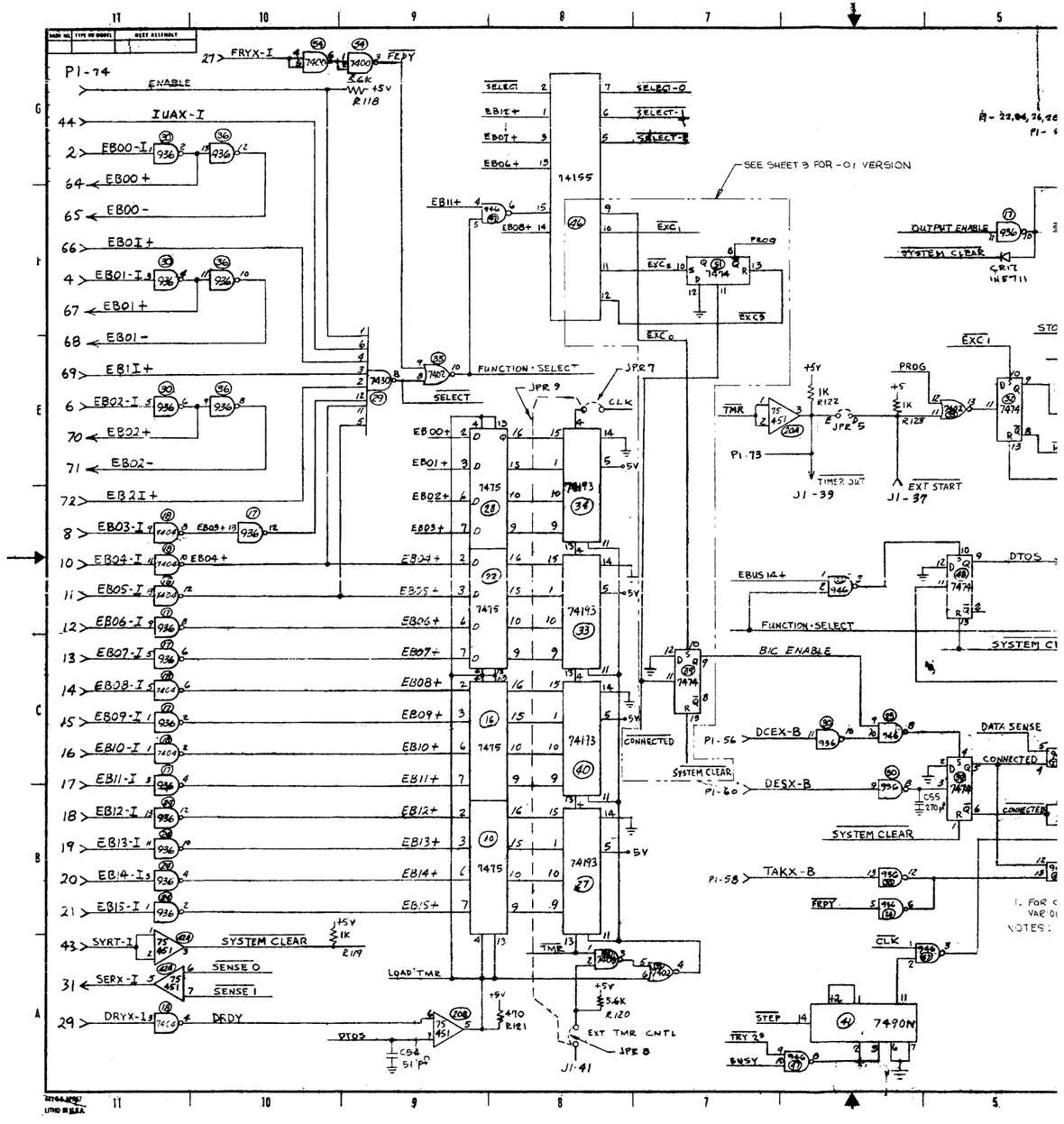

P1-74
ENABLE
IUAX-I
EB00-I
EB00+
EB00-
EB01+
EB01-I
EB01-
EB11+
EB02-I
EB02+
EB02-
EB12I+
EB03-I
EB04-I
EB05-I
EB06-I
EB07-I
EB08-I
EB09-I
EB10-I
EB11-I
EB12-I
EB13-I
EB14-I
EB15-I
SYRT-I
SERX-I
DRYX-I
FRYX-I
FEPY
+5V
1K R118
SEE SHEET B FOR -01 VERSION
FUNCTION SELECT
SELECT
JPR 9
JPR 7
CLK
74155
74193
74175
74173
74190N
EXC1
EXC0
PROG
OUTPUT ENABLE
SYSTEM CLEAR
TMR
TIMER OUT
J1-39
EXT START
J1-37
EBUS 14+
BIC ENABLE
CONNECTED
DATA SENSE
P1-56
DCEX-B
P1-60
DESX-B
P1-58
TAKX-B
FEPY
SYSTEM CLEAR
SENSE 0
SENSE 1
LOAD TMR
DTOS
DRDY
EXT TMR CNTL
JPR 8
J1-41
STEP
TRY 20
BUSY
5.6K R120
470 R121
CS4 51pF
CS5 270pF
CS6 .1μF
CR12 1N5711
CR13 1N5711
NOTES:

Figure D-1, Sht 1

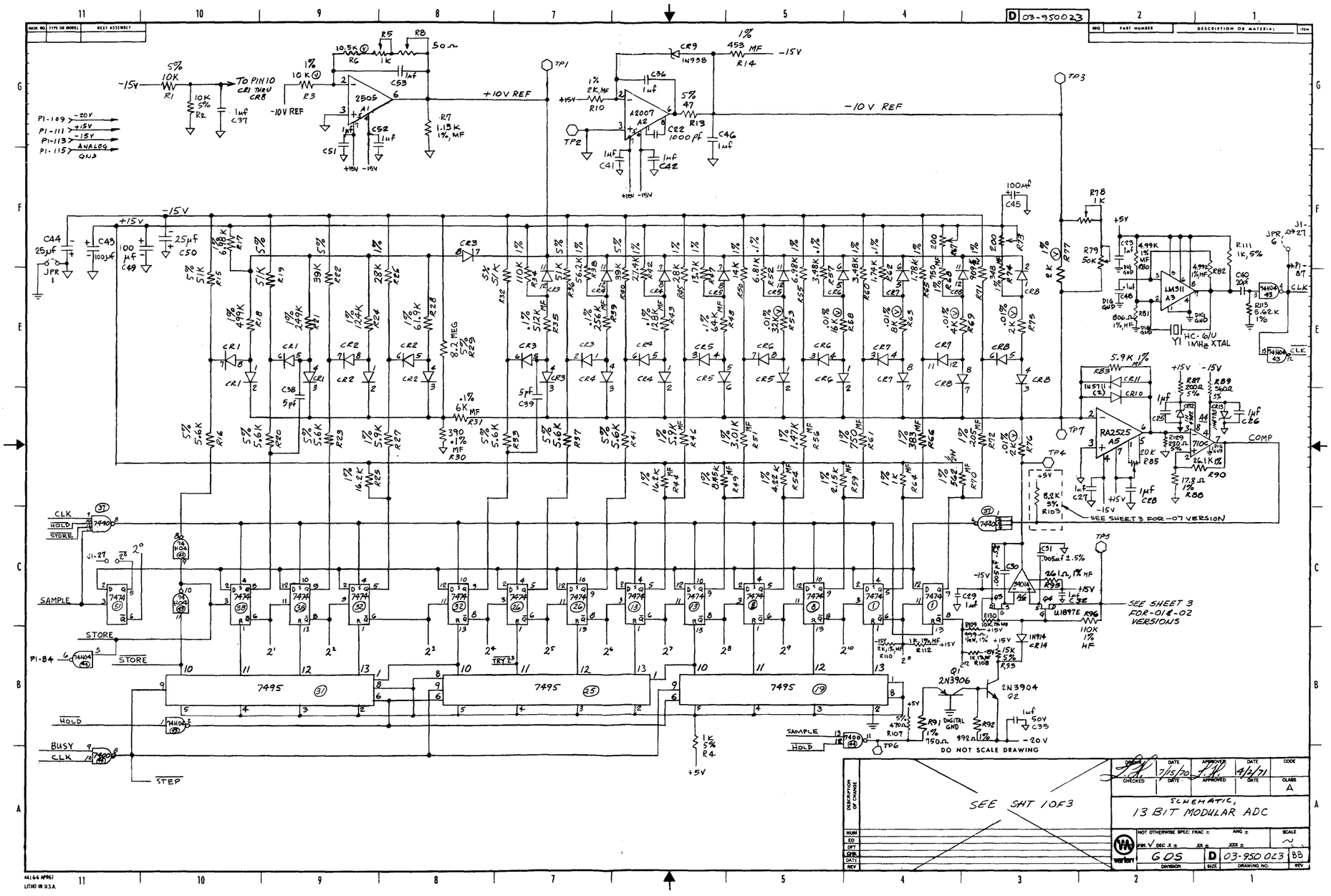


Figure D-1, Sht 2

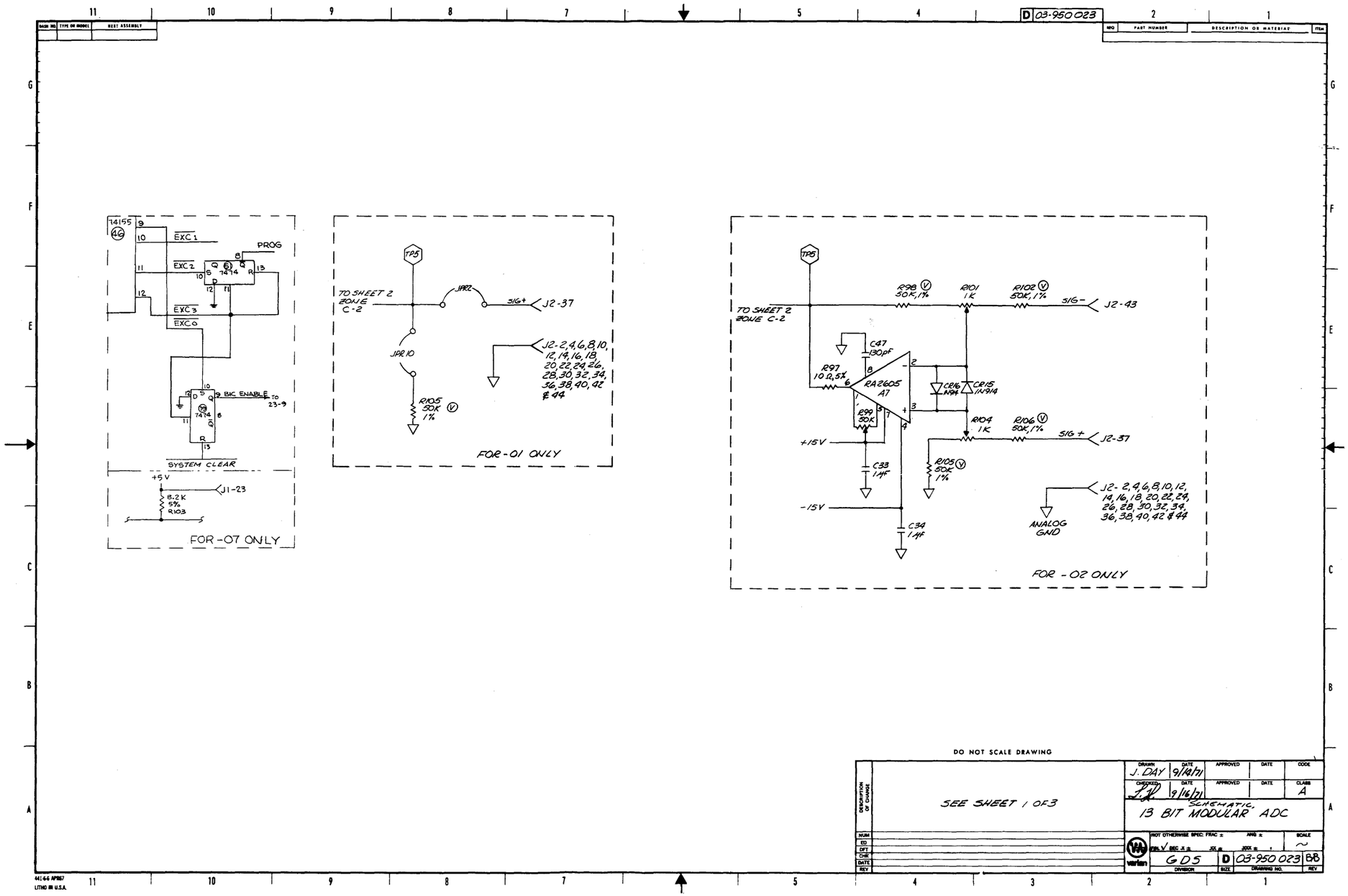


Figure D-1, Sht 3

ADC MODULE, 03-950025

Schematic Reference	Description	Varian Part No.
IC1, 18, 13, 26 32, 38, 39, 45, 48, 51, 52	IC Element - 7474	62-600 365
IC39, 45, 48, 51, 52		
IC2, 3, 5, 6, 11, 12	IC Element - 944	62-600 306
IC4, 9, 10, 15, 16 22, 28, IC10, 16		
22, 28	IC Element - 7475	62-600 351
IC17, 24, 30, 36	IC Element - 936	62-600 309
IC19, 25, 31	IC Element - 7495	62-600 406
IC20A, 14A&B, 42A&B, 20B, 42A&B	IC Element - 75451	62-600 260
IC23, 47	IC Element - 946	62-600 303
IC27, 33, 34, 40	IC Element - 74193	62-600 367
IC29	IC Element - 7430	62-600 359
IC35	IC Element - 7402	62-600 356
IC37	IC Element - 7440	62-600 310
IC41	IC Element - 7490 N	62-600 350
IC43	IC Element - 74H04	62-600 012
IC44, 54	IC Element - 7400	62-600 355
IC46	IC Element - 74155	62-600 271
IC50	IC Element - 7473	62-600 362
IC 53	IC Element - 962	62-600 300
IC18	IC Element - 7404 N	62-600 013
Y1	Crystal	66-479 984
A1	Amplifier, 2505	62-600 219
A2	Amplifier, 42007	62-600 235
A3	Amplifier, LM311	62-600 208
A4	Amplifier, μA710 C	62-600 190
A5	Amplifier, 2525	62-600 204
A6	Amplifier, 3401 A	78-199 966
A7	Amplifier, 2605	62-600 203
CR1-CR8	Diode Array, CA3039	62-600 091
CR9	Diode, 1N938	66-300 938
CR10, 11, 17	Diode, 1N5711	66-981 101
CR12	Diode, 1N4742	66-304 742
CR13	Diode, 1N4735	66-304 735
CR14	Diode, 1N914	66-304 148
CR15, 16		
R1, 2	Res, F.C. 10 K, 1/4 W, 5%	32-301 510
R4, 111, 119, 122, 123, 127, 128	Res, F.C. 1 K, 1/4 W, 5%	32-301 410
R13	Res, F.C. 47 Ω, 1/4 W, 5%	32-301 247
R15, 19, 32, 36	Res, F.C. 51 K, 1/4 W, 5%	32-301 551

ADC MODULE, 30-950025 (Cont'd)

Schematic Reference	Description	Varian Part No.
R16, 20, 23, 33 37, 41, 118, 120 124	Res, F.C. 5.6 K, 1/4 W, 5%	32-301 456
R29	Res, F.C. 8.2 MEG, 1/4 W, 5%	32-301 782
R93	Res, F.C., 15 K, 1/4 W, 5%	32-301 515
R97	Res, F.C. 10 Ω, 1/4 W, 5%	32-301 210
R103	Res, F.C. 8.2 K, 1/4 W, 5%	32-301 482
R107, R121	Res, F.C. 470 Ω, 1/4 W, 5%	32-301 347
R87	Res, F.C. 200 Ω, 1/4 W, 5%	32-301 320
R89	Res, F.C. 560 Ω, 1/4 W, 5%	32-301 356
R129	Res, F.C. 220 Ω, 1/4 W, 5%	32-301 322
R22, R40	Res, F.C. 39 K, 1/4 W, 5%	32-301 539
R7	Res, MF, 1.13 K, 1/4 W, 1%	31-224 113
R10, 110	Res, MF, 2 K, 1/4 W, 1%	31-224 200
R14	Res, MF, 453 Ω, 1/4 W, 1%	31-223 453
R17, 55	Res, MF, 6.98 K, 1/4 W, 1%	31-224 698
R18	Res, MF, 499 K, 1/4 W, 1%	31-226 499
R21	Res, MF, 249 K, 1/4 W, 1%	31-226 249
R24	Res, MF, 124 K, 1/4 W, 1%	31-226 124
R25, 44	Res, MF, 16.2 K, 1/4 W, 1%	31-225 162
R26, 45	Res, MF, 28 K, 1/4 W, 1%	31-225 280
R27, 46, 83	Res, MF, 5.9 K, 1/4 W, 1%	31-224 590
R28	Res, MF, 61.9 K, 1/4 W, 1%	31-225 619
R34, R96	Res, MF, 110 K, 1/4 W, 1%	31-226 110
R38	Res, MF, 56.2 K, 1/4 W, 1%	31-225 562
R42	Res, MF, 27.4 K, 1/4 W, 1%	31-225 274
R47	Res, MF, 13.7 K, 1/4 W, 1%	31-225 137
R49	Res, MF, 8.45 K, 1/4 W, 1%	31-224 845
R50	Res, MF, 14 K, 1/4 W, 1%	31-225 140
R51	Res, MF, 3.01 K, 1/4 W, 1%	31-224 301
R54	Res, MF, 4.22 K, 1/4 W, 1%	31-224 422
R56	Res, MF, 1.47 K, 1/4 W, 1%	31-224 147
R59	Res, MF, 2.15 K, 1/4 W, 1%	31-224 215
R60	Res, MF, 3.48 K, 1/4 W, 1%	31-224 348
R61, 68, 91	Res, MF, 750 Ω, 1/4 W, 1%	31-223 750
R64, 108, 112	Res, MF, 1 K, 1/4 W, 1%	31-224 100
R65	Res, MF, 1.78 K, 1/4 W, 1%	31-224 178
R66	Res, MF, 383 Ω, 1/4 W, 1%	31-223 383
R72	Res, MF, 205 Ω, 1/4 W, 1%	31-223 205
R74	Res, MF, 348 Ω, 1/4 W, 1%	31-223 348
R80, 82	Res, MF, 4.99 K, 1/4 W, 1%	31-224 499
R90	Res, MF, 26.1 K, 1/4 W, 1%	31-225 261
R92	Res, MF, 392 Ω, 1/4 W, 1%	31-223 392
R95	Res, MF, 261 Ω, 1/4 W, 1%	31-223 261
R130	Res, MF, 10 K, 1/4 W, 1%	31-225 100
R113	Res, MF, 5.62 K, 1/4 W, 1%	31-224 562
R88	Res, MF, 17.8 Ω, 1/4 W, 1%	31-222 178
R81	Res, MF, 806 Ω, 1/4 W, 1%	31-223 806
R70	Res, MF, 562 Ω, 1/2 W, 1%	31-614 654

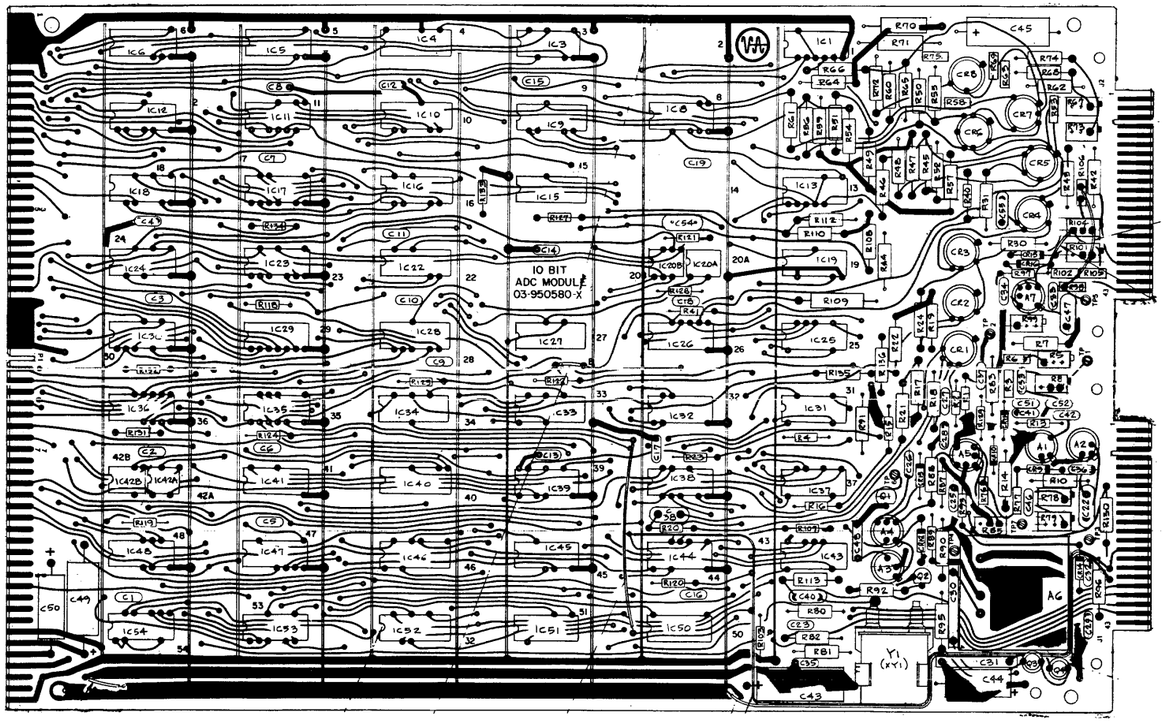
Schematic Reference
R71
R109
R53
R58
R63
R69
R75, R76
R98, 102, 105, 106
R6
R77
R3
R30
R31
R35
R39
R43
R48
R52
R57
R62
R5, R78, 101, 104
R8
R67, R73
R79, 99
R85
Q1
Q2
Q3, Q4
C1-19, 23, 25-29, 32-37, 41, 42, 46, 51-5
C2, 4, 5, 8, 9, 12, 13, 14, 16, 19, 23
C22
C30, C31
C38, C39
C40, C43, 45, 49
C44, 50
C47
C48
C55
C54

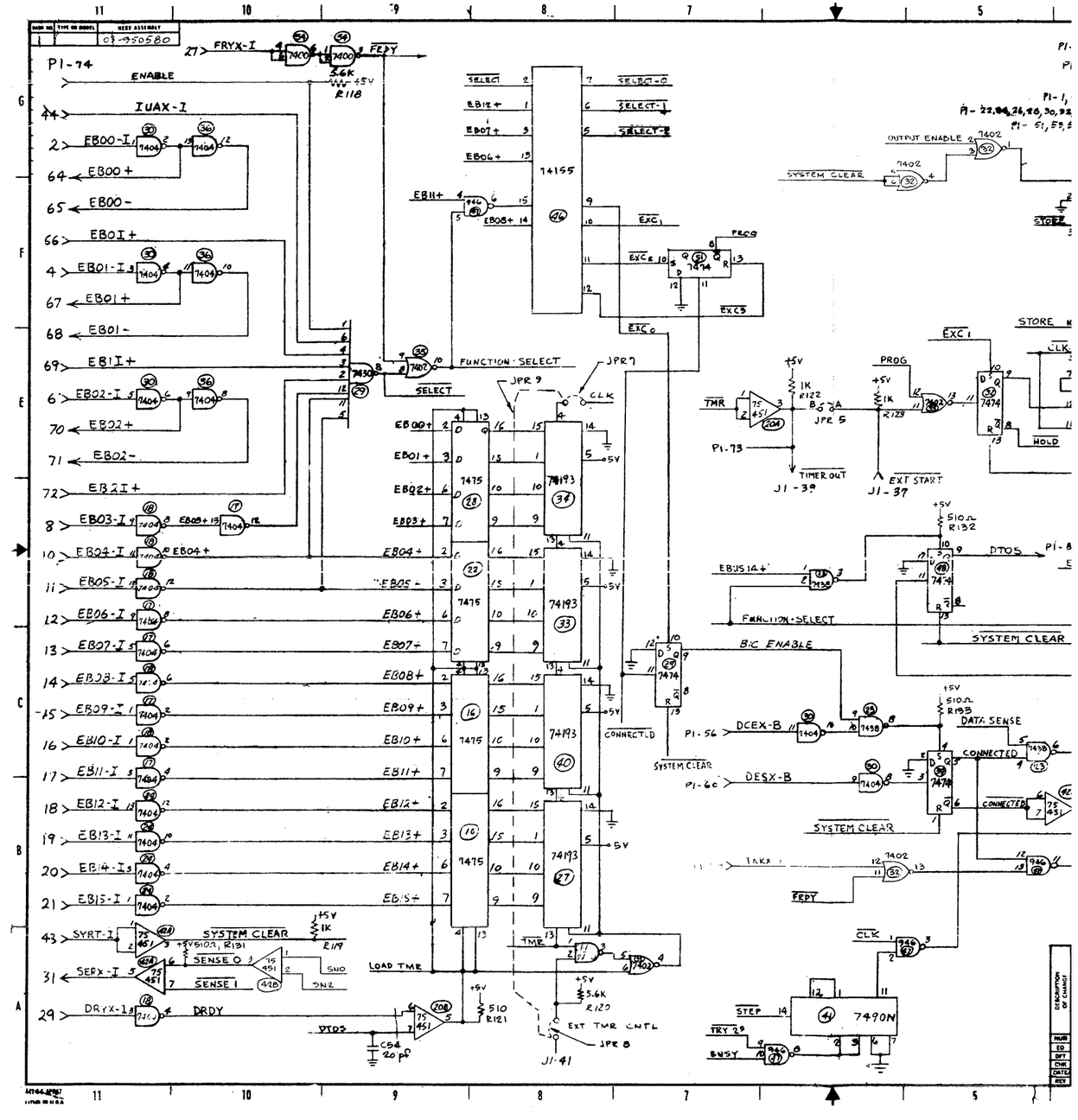
ADC MODULE, 30-950025 (Cont'd)

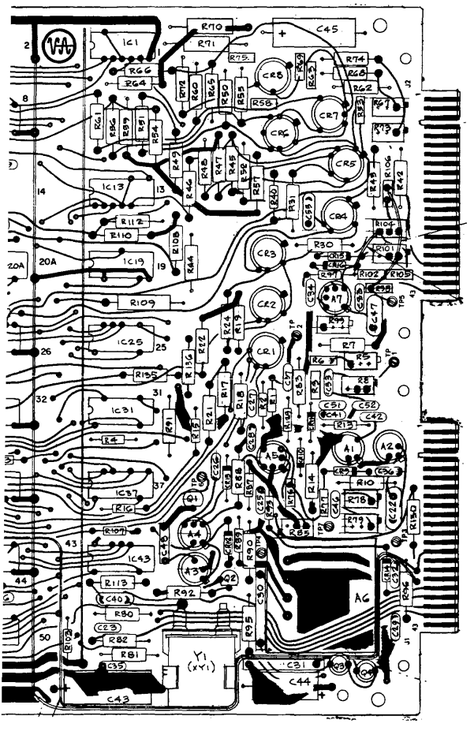
Varian Part No.	Schematic Reference	Description	Varian Part No.
	R16,20,23,33 37,41,118,120		
62-600 365	124	Res, F.C. 5.6 K, 1/4 W, 5%	32-301 456
	R29	Res, F.C. 8.2 MEG, 1/4 W, 5%	32-301 782
62-600 306	R93	Res, F.C., 15 K, 1/4 W, 5%	32-301 515
	R97	Res, F.C. 10Ω, 1/4 W, 5%	32-301 210
	R103	Res, F.C. 8.2 K, 1/4 W, 5%	32-301 482
62-600 351	R107,R121	Res, F.C. 470 Ω, 1/4 W, 5%	32-301 347
62-600 309	R87	Res, F.C. 200 Ω, 1/4 W, 5%	32-301 320
62-600 406	R89	Res, F.C. 560 Ω, 1/4 W, 5%	32-301 356
	R129	Res, F.C. 220 Ω, 1/4 W, 5%	32-301 322
	R22,R40	Res, F.C. 39 K, 1/4 W, 5%	32-301 539
62-600 260	R7	Res, MF, 1.13 K, 1/4 W, 1%	31-224 113
62-600 303	R10,110	Res, MF, 2 K, 1/4 W, 1%	31-224 200
62-600 367	R14	Res, MF, 453 Ω, 1/4 W, 1%	31-223 453
62-600 359	R17,55	Res, MF, 6.98 K, 1/4 W, 1%	31-224 698
62-600 356	R18	Res, MF, 499 K, 1/4 W, 1%	31-226 499
62-600 310	R21	Res, MF, 249 K, 1/4 W, 1%	31-226 249
62-600 350	R24	Res, MF, 124 K, 1/4 W, 1%	31-226 124
62-600 012	R25,44	Res, MF, 16.2 K, 1/4 W, 1%	31-225 162
62-600 355	R26,45	Res, MF, 28 K, 1/4 W, 1%	31-225 280
62-600 271	R27,46,83	Res, MF, 5.9 K, 1/4 W, 1%	31-224 590
62-600 362	R28	Res, MF, 61.9 K, 1/4 W, 1%	31-225 619
62-600 300	R34,R96	Res, MF, 110 K, 1/4 W, 1%	31-226 110
62-600 013	R38	Res, MF, 56.2 K, 1/4 W, 1%	31-225 562
66-479 984	R42	Res, MF, 27.4 K, 1/4 W, 1%	31-225 274
62-600 219	R47	Res, MF, 13.7 K, 1/4 W, 1%	31-225 137
62-600 235	R49	Res, MF, 8.45 K, 1/4 W, 1%	31-224 845
62-600 208	R50	Res, MF, 14 K, 1/4 W, 1%	31-225 140
62-600 190	R51	Res, MF, 3.01 K, 1/4 W, 1%	31-224 301
62-600 204	R54	Res, MF, 4.22 K, 1/4 W, 1%	31-224 422
78-199 966	R56	Res, MF, 1.47 K, 1/4 W, 1%	31-224 147
62-600 203	R59	Res, MF, 2.15 K, 1/4 W, 1%	31-224 215
62-600 091	R60	Res, MF, 3.48 K, 1/4 W, 1%	31-224 348
66-300 938	R61,68,91	Res, MF, 750 Ω, 1/4 W, 1%	31-223 750
66-981 101	R64,108,112	Res, MF, 1 K, 1/4 W, 1%	31-224 100
66-304 742	R65	Res, MF, 1.78 K, 1/4 W, 1%	31-224 178
66-304 735	R66	Res, MF, 383 Ω, 1/4 W, 1%	31-223 383
66-304 148	R72	Res, MF, 205 Ω, 1/4 W, 1%	31-223 205
	R74	Res, MF, 348 Ω, 1/4 W, 1%	31-223 348
32-301 510	R80,82	Res, MF, 4.99 K, 1/4 W, 1%	31-224 499
	R90	Res, MF, 26.1 K, 1/4 W, 1%	31-225 261
32-301 410	R92	Res, MF, 392 Ω, 1/4 W, 1%	31-223 392
32-301 247	R95	Res, MF, 261 Ω, 1/4 W, 1%	31-223 261
32-301 551	R130	Res, MF, 10 K, 1/4 W, 1%	31-225 100
	R113	Res, MF, 5.62 K, 1/4 W, 1%	31-224 562
	R88	Res, MF, 17.8 Ω, 1/4 W, 1%	31-222 178
	R81	Res, MF, 806 Ω, 1/4 W, 1%	31-223 806
	R70	Res, MF, 562 Ω, 1/2 W, 1%	31-614 654

ADC MODULE, 30-950025 (Cont'd)

Schematic Reference	Description	Varian Part No.
R71	Res, MF, 909 Ω, 1/2 W, 1%	31-614 653
R109	Res, MF, 499 Ω, 1/2 W, 1%	31-614 655
R53	Res, MF, 32 K, .01%	31-239 053
R58	Res, MF, 16 K, .01%	31-239 052
R63	Res, MF, 8 K, .01%	31-239 051
R69	Res, MF, 4 K, .01%	31-239 050
R75,R76	Res, MF, 2 K, .01%	31-239 059
R98,102,105, 106	Res, MF, 50 K, 1%	31-239 058
R6	Res, MF, 10.5 K, 1%	31-239 057
R77	Res, MF, 2 K, 1%	31-239 031
R3	Res, MF, 10 K, 1%	31-239 033
R30	Res, MF, 390 Ω, .1%	31-613 347
R31	Res, MF, 6 K,	31-613 281
R35	Res, MF, 512 K	31-613 339
R39	Res, MF, 256 K	31-613 340
R43	Res, MF, 128 K	31-613 344
R48	Res, MF, 64 K	31-613 343
R52	Res, MF, 6.81 K	31-613 342
R57	Res, MF, 3.48 K	31-613 345
R62	Res, MF, 1.74 K, .1%	31-613 346
R5,R78,101,104	Res, VAR, W.W. 1 K	37-577 311
R8	Res, VAR, W.W. 50 Ω	37-577 308
R67,R73	Res, VAR, W.W. 200 Ω	37-577 310
R79,99	Res, VAR, W.W. 50 K	37-577 315
R85	Res, VAR, W.W. 20 K	37-577 314
Q1	Transistor, 2N3906	62-903 906
Q2	Transistor, 2N3904	62-903 904
Q3,Q4	Transistor, FET, U1897E	62-798 125
C1-19,23,25-29, 32-37,41,42,46,51-53, C2,4,5,8,9,12,13, 14,16,19,23	Cap, CER, 1 μf, 200 V, 10%	41-228 009
C22	Cap, CER, 1000 pf, 100 V, 5%	41-159 599
C30,C31	Cap, Mylar, .005 μf, 100 V, 1/2%	41-718 754
C38,C39	Cap, CER, 5 pf, 500 V, 10%	41-159 505
C40,	Cap, CER, 20 pf, 500 V, 5%	41-159 573
C43,45,49	Cap, Elect, 100 μf, 25 V	41-506 258
C44,50	Cap, Elect, 25 μf, 25 V	41-506 255
C47	Cap, CER, 130 pf, 500 V, 5%	41-159 566
C48	Cap, CER, .1 μf, 25 V, 20%	41-206 993
C55	Cap, 270 pf, 500V	41-159 601
C54	Cap, MICA, 51 pf, 500V, 5%	41-159 584


10 BIT
ADC MODULE
03-950580-X


03-950580
P1-74
ENABLE
IUAX-I
EB00-I
EB00+
EB00-
EB01+
EB01-I
EB01-
EB1I+
EB02-I
EB02+
EB02-
EB2I+
EB03-I
EB03+
EB04-I
EB04+
EB05-I
EB05+
EB06-I
EB06+
EB07-I
EB07+
EB08-I
EB08+
EB09-I
EB09+
EB10-I
EB10+
EB11-I
EB11+
EB12-I
EB12+
EB13-I
EB13+
EB14-I
EB14+
EB15-I
EB15+
SYRT-I
SERX-I
DRYX-I
FRYX-I
FERY
36K
R118
74155
SELECT-0
SELECT-1
SELECT-2
EXC1
EXC0
FUNCTION SELECT
SELECT
74175
74193
JPR 7
JPR 9
CLK
+5V
TMR
1K
R122
JPR 5
PROG
R123
TIMER OUT
J1-39
EXT START
J1-37
STORE
HOLD
SYSTEM CLEAR
SENSE 0
SENSE 1
SNO
SN2
DRDY
DTOS
LOAD TME
TME
5.6K
R120
EXT TMR CNTL
JPR 8
J1-41
510Ω
R121
C64
20 pf
OUTPUT ENABLE
STORE
EBUS14+
FUNCTION-SELECT
B/C ENABLE
DCEX-B
DESX-B
P1-56
P1-66
DATA SENSE
CONNECTED
TAKX
FERY
CLK
STEP
TRY 29
BUSY
7490N
R132
R133
P1-73
P1-8



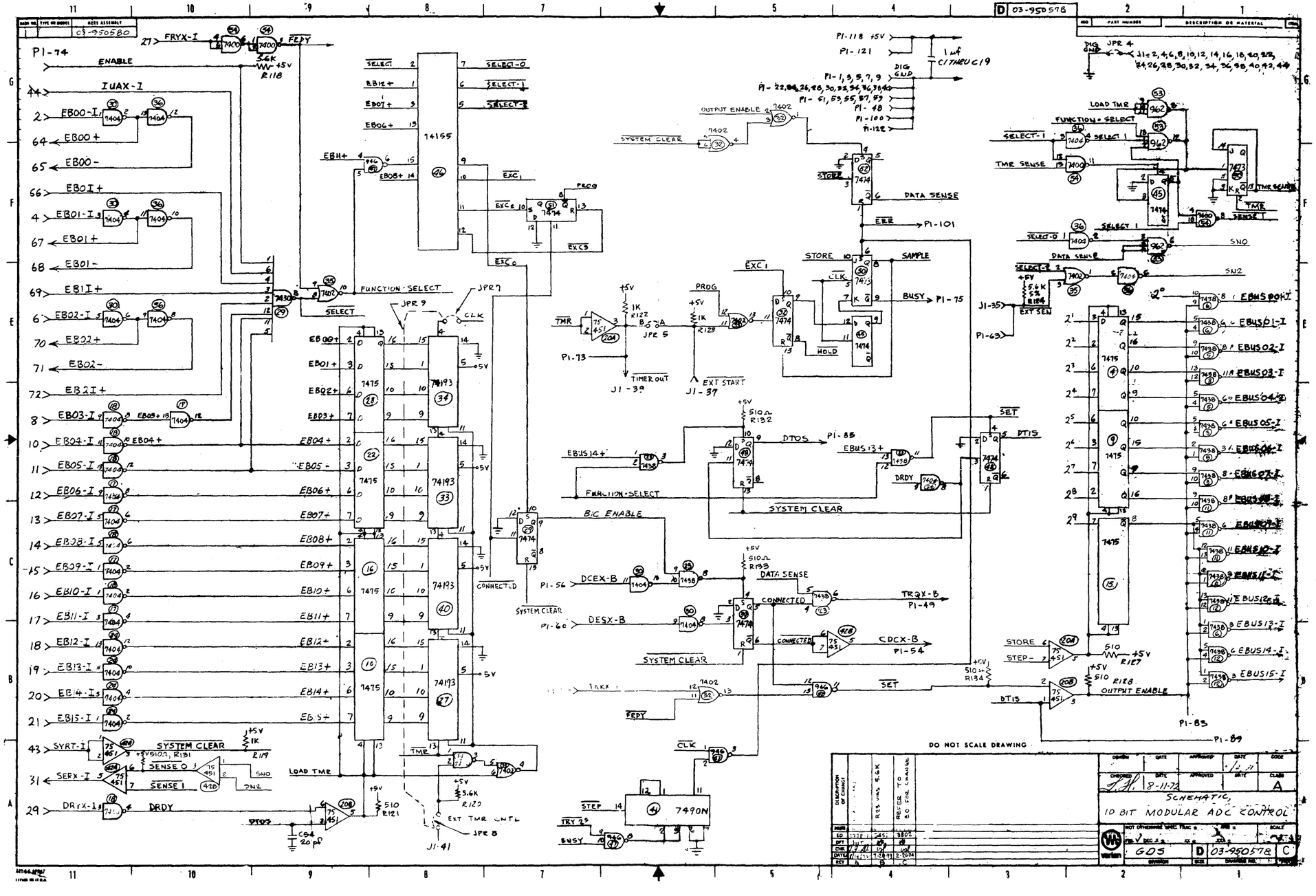


Figure D-2, Sht 1

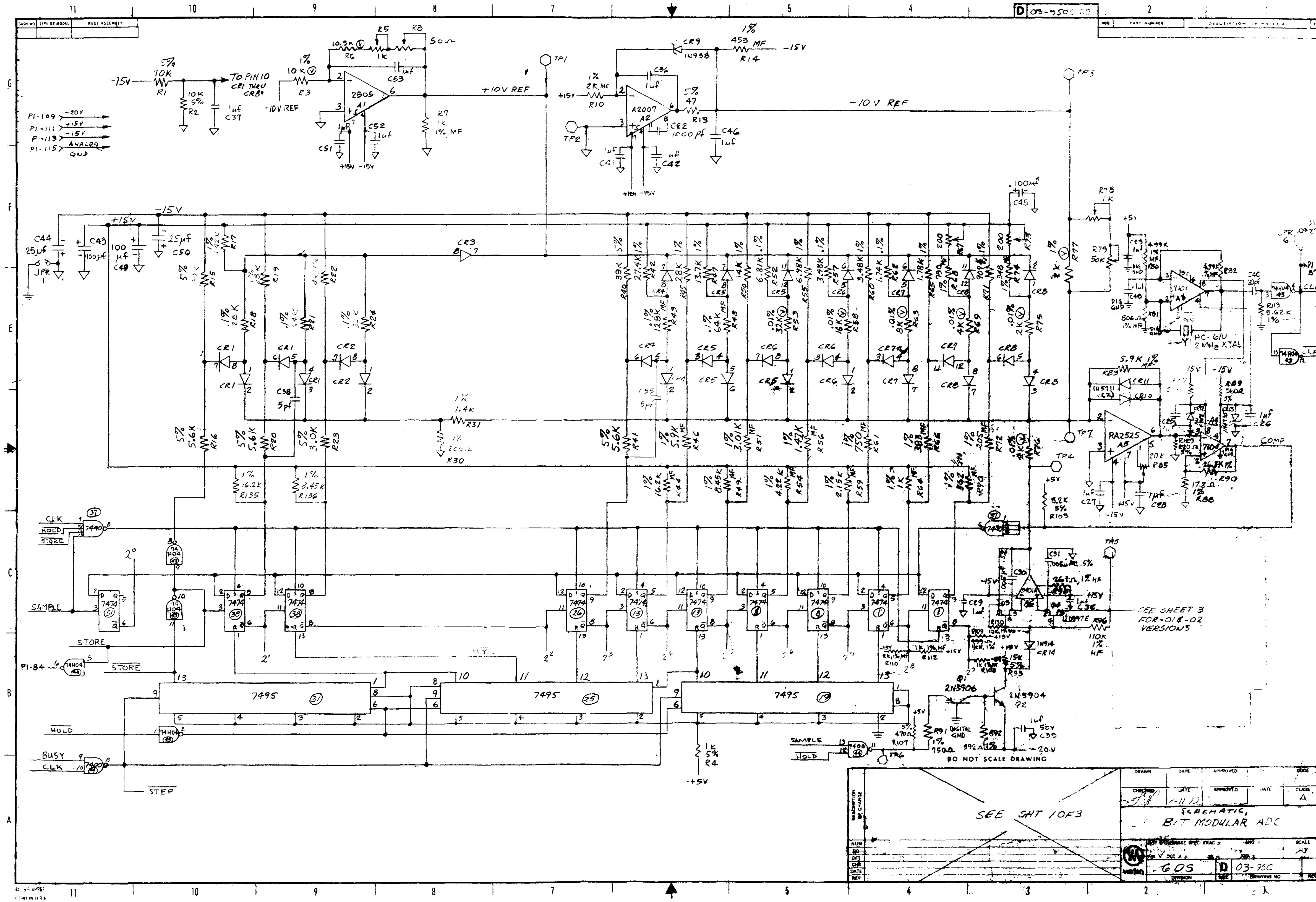


Figure D-2, Sht 2

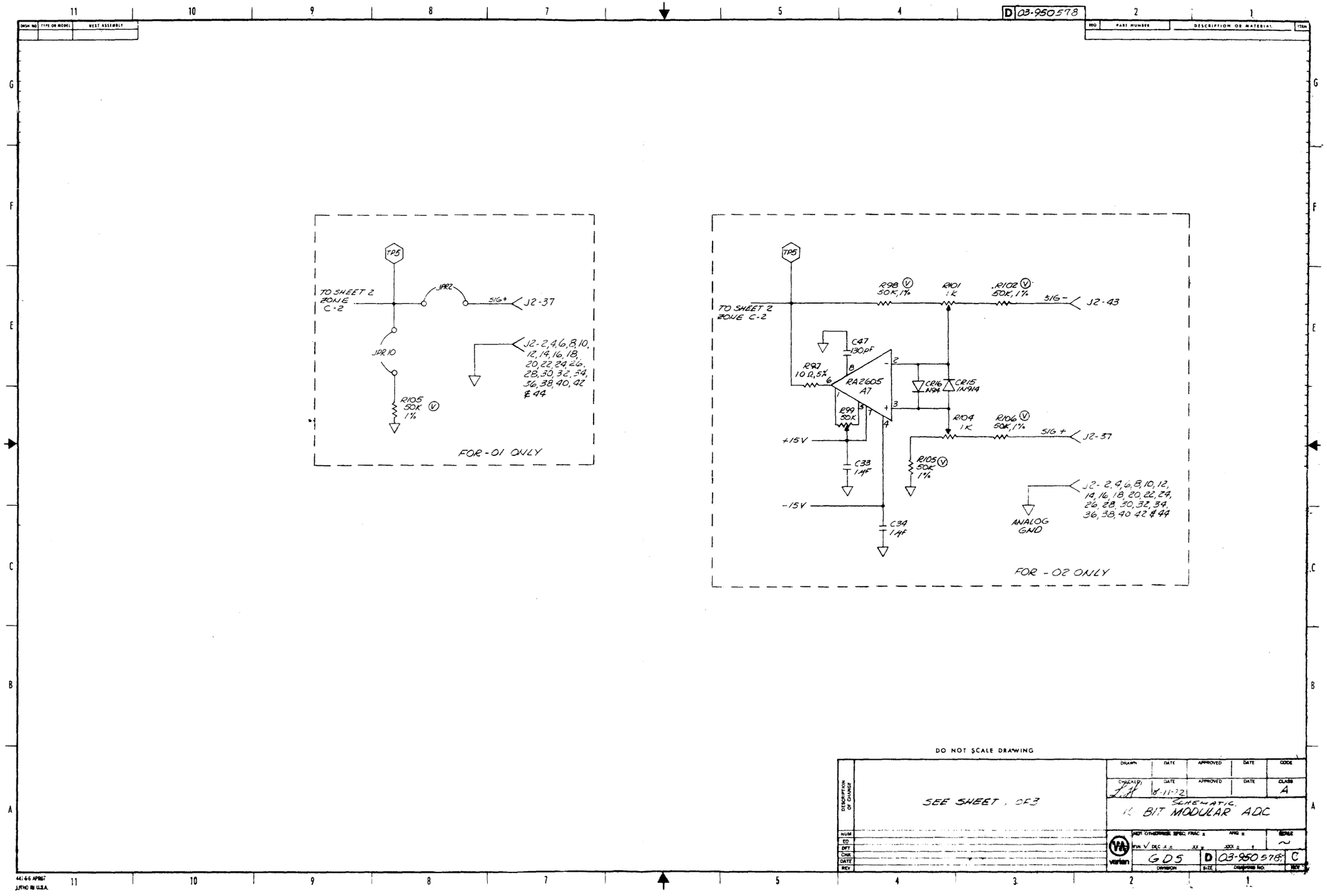


Figure D-2, Sht 3

10 BIT ADC MODULE, 03-950580

Schematic Reference	Description	Varian Part No.
TP1-TP7	Terminal, Swage	16-229 857
IC1, 8, 15, 26, 38, 39, 45, 48, 51, 52	IC Element - 7474	62-600 365
IC4, 9, 10, 15, 16, 22, 28	IC Element - 7475	62-600 351
IC3, 5, 6, 11, 12, 23	IC Element - 7438	62-600 373
IC19, 25, 31	IC Element - 7495	62-600 406
IC20A, 20B42A, 42B	IC Element - 75451	62-600 260
IC 47	IC Element - 946	62-600 303
IC 27, 33, 34, 40	IC Element - 74193	62-600 367
IC29	IC Element - 7430	62-600 359
IC32, 35	IC Element - 7402	62-600 356
IC37	IC Element - 7440	62-600 310
IC41	IC Element - 7490N	62-600 350
IC43	IC Element - 74H04	62-600 012
IC44, 54	IC Element - 7400	62-600 355
IC46	IC Element - 74155	62-600 271
IC50	IC Element - 7473	62-600 362
IC53	IC Element - 962	62-600 300
IC17, 18, 24, 30, 36	IC Element - 7404N	62-600 013
Y1	Crystal	66-481 592
A1	Amplifier, 2505	62-600 219
A2	Amplifier, A2007	62-600 235
A3, A4	Amplifier, μA710C	62-600 190
A5	Amplifier, 2525	62-600 204
A6	Amplifier, 3401A	78-199 966
A7	Amplifier, 2605	62-600 203
CR1-CR8	Diode Array, CA3039	62-600 091
CR9	Diode, 1N938	66-300 938
CR10, 11, 17	Diode, 1N5711	66-981 101
CR12	Diode, 1N4742	66-304 742
CR13	Diode, 1N4735	66-304 735
CR14, 15, 16	Diode, 1N914	66-304 148
R1R2	Res. F.C. 10 K, 1/4 W, 5%	32-301 510
R4, 119, 122, 123	Res. F.C. 1 K, 1/4, 5%	32-301 410
R13	Res. F.C., 47 Ω, 1/4 W, 5%	32-301 247
R19	Res. F.C., 51 K, 1/4 W, 5%	32-301 551
R16, 20, 23, 41, 118, 120, 124	Res, F.C., 5.6 K, 1/4 W, 5%	32-301 456
R127, 128, R131, 134	Res., F.C., 510 Ω, 1/4 W, 5%	32-301 351
R93	Res., F.C., 15 K, 1/4 W, 5%	32-301 515
R97	Res., F.C., 10 Ω, 1/4, 5%	32-301 210

10 BIT ADC MODULE, 03-950580 (Cont'd)

Schematic Reference	Description	Varian Part No.
R103	Res., F.C., 8.2 K, 1/4 W, 5%	32-301 482
R107, R121	Res., F.C., 470 Ω, 1/4 W, 5%	32-301 347
R87	Res, F.C., 200 Ω, 1/4 W, 5%	32-301 320
R89	Res. F.C., 560 Ω, 1/4 W, 5%	32-301 356
R129	Res. F.C., 220 Ω, 1/4 W, 5%	32-301 322
R15, R40	Res. F.C., 39 K, 1/4 W, 5%	32-301 539
R10, 110	Res. MF, 2 K, 1/4 W, 1%	31-224 200
R14	Res. MF, 453 Ω, 1/4 W, 1%	31-223 453
R55	Res. MF, 6.98 K, 1/4 W, 1%	31-224 698
R17	Res. MF, 4.42 K, 1/4 W, 1%	31-224 442
R30	Res. MC, 200 Ω, 1/4 W, 1%	31-223 200
R44, 135	Res. MC, 16.2 K, 1/4 W, 1%	31-225 162
R45	Res. MC, 28 K, 1/4 W, 1%	31-225 230
R46, 83	Res. MC, 5.9 K, 1/4 W, 1%	31-224 590
R96	Res. MC, 110 K, 1/4 W, 1%	31-226 110
R31	Res. MC, 1.4 K, 1/4 W, 1%	31-224 140
R42	Res. MC, 27.4 K, 1/4 W, 1%	31-225 274
R47	Res. MC, 13.7 K, 1/4 W, 1%	31-225 137
R49, R136	Res. MC, 8.45 K, 1/4 W, 1%	31-224 845
R22, 50	Res. MC, 14 K, 1/4 W, 1%	31-225 140
R51	Res. MC, 3.01 K, 1/4 W, 1%	31-224 301
R54	Res. MC, 4.22 K, 1/4 W, 1%	31-224 422
R56	Res. MC, 1.47 K, 1/4 W, 1%	31-224 147
R59	Res. MC, 2.15 K, 1/4 W, 1%	31-224 215
R60	Res. MC, 3.48 K, 1/4 W, 1%	31-224 348
R61, 68, 91	Res. MC, 750 Ω, 1/4 W, 1%	31-223 750
R7, 64, 108, 112	Res. MC, 1 K, 1/4 W, 1%	31-224 100
R65	Res. MC, 1.78 K, 1/4 W, 1%	31-224 178
R66	Res. MC, 383 Ω, 1/4 W, 1%	31-223 383
R72	Res. MC, 205 Ω, 1/4 W, 1%	31-223 205
R74	Res. MC, 348 Ω, 1/4 W, 1%	31-223 348
R80, 82	Res. MC, 4.99 K, 1/4 W, 1%	31-224 499
R90	Res. MC, 26.1 K, 1/4 W, 1%	31-225 261
R92	Res. MC, 39.2 Ω, 1/4 W, 1%	31-223 392
R95	Res. MC, 261 Ω, 1/4 W, 1%	31-223 261
R130	Res. MC, 10 K, 1/4 W, 1%	31-225 100
R113	Res. MC, 5.62 K, 1/4 W, 1%	31-224 562
R88	Res. MC, 17.8 Ω, 1/4 W, 1%	31-222 178
R81	Res. MF, 506 Ω, 1/4 W, 1%	31-223 806
R70	Res. MF, 562 Ω, 1/2 W, 1%	31-614 654
R71	Res. MF, 909 Ω, 1/2 W, 1%	31-614 653
R109	Res. MF, 499 Ω, 1/2 W, 1%	31-614 655
R53	Res. MF, 32 K, .10%	31-239 053
R58	Res. MF, 16 K, .10%	31-239 052
R63	Res. MF, 8 K, .01%	31-239 051
R69	Res. MF, 4 K, .10%	31-239 050
R75, R76	Res. MF, 2 K, .10%	31-239 059

Schematic Reference
R98, 102, 105
106
R105
R6
R77
R3
R18, 43
R21, 48
R52
R57
R62
R24
R5, R78, 25, 78
101, 104
R8
R67, R73
R79, R99
R85
Q1
Q2
Q3, Q4
C1-19, 23, 25-29, 32-37, 41, 42, 46, 51-53
C22
C30, C31
C38, C55
C40, C54
C43, 45, 49
C44, 50
C47
C48
JPR
JPR2
JPR4
JPR5(A-B)
JPR6
JPR9
JPR10

10 BIT ADC MODULE, 03-950580 (Cont'd)

Varian Part No.	Schematic Reference	Description	Varian Part No.
16-229 857	R103	Res., F.C., 8.2 K, 1/4 W, 5%	32-301 482
	R107, R121	Res., F.C., 470 Ω, 1/4 W, 5%	32-301 347
	R87	Res, F.C., 200 Ω, 1/4 W, 5%	32-301 320
62-600 365	R89	Res. F.C., 560 Ω, 1/4 W, 5%	32-301 356
	R129	Res. F.C., 220 Ω, 1/4 W, 5%	32-301 322
62-600 351	R15, R40	Res. F.C., 39 K, 1/4 W, 5%	32-301 539
	R10, 110	Res. MF, 2 K, 1/4 W, 1%	31-224 200
62-600 373	R14	Res. MF, 453 Ω, 1/4 W, 1%	31-223 453
62-600 406	R55	Res. MF, 6.98 K, 1/4 W, 1%	31-224 698
	R17	Res. MF, 4.42 K, 1/4 W, 1%	31-224 442
62-600 260	R30	Res. MC, 200 Ω, 1/4 W, 1%	31-223 200
62-600 303	R44, 135	Res. MC, 16.2 K, 1/4 W, 1%	31-225 162
62-600 367	R45	Res. MC, 28 K, 1/4 W, 1%	31-225 230
62-600 359	R46, 83	Res. MC, 5.9 K, 1/4 W, 1%	31-224 590
62-600 356	R96	Res. MC, 110 K, 1/4 W, 1%	31-226 110
62-600 310	R31	Res. MC, 1.4 K, 1/4 W, 1%	31-224 140
62-600 350	R42	Res. MC, 27.4 K, 1/4 W, 1%	31-225 274
62-600 012	R47	Res. MC, 13.7 K, 1/4 W, 1%	31-225 137
62-600 355	R49, R136	Res. MC, 8.45 K, 1/4 W, 1%	31-224 845
62-600 271	R22, 50	Res. MC, 14 K, 1/4 W, 1%	31-225 140
62-600 362	R51	Res. MC, 3.01 K, 1/4 W, 1%	31-224 301
62-600 300	R54	Res. MC, 4.22 K, 1/4 W, 1%	31-224 422
	R56	Res. MC, 1.47 K, 1/4 W, 1%	31-224 147
62-600 013	R59	Res. MC, 2.15 K, 1/4 W, 1%	31-224 215
66-481 592	R60	Res. MC, 3.48 K, 1/4 W, 1%	31-224 348
62-600 219	R61, 68, 91	Res. MC, 750 Ω, 1/4 W, 1%	31-223 750
62-600 235	R7, 64, 108, 112	Res. MC, 1 K, 1/4 W, 1%	31-224 100
62-600 190	R65	Res. MC, 1.78 K, 1/4 W, 1%	31-224 178
62-600 204	R66	Res. MC, 383 Ω, 1/4 W, 1%	31-223 383
78-199 966	R72	Res. MC, 205 Ω, 1/4 W, 1%	31-223 205
62-600 203	R74	Res. MC, 348 Ω, 1/4 W, 1%	31-223 348
62-600 091	R80, 82	Res. MC, 4.99 K, 1/4 W, 1%	31-224 499
66-300 938	R90	Res. MC, 26.1 K, 1/4 W, 1%	31-225 261
66-981 101	R92	Res. MC, 39.2 Ω, 1/4 W, 1%	31-223 392
66-304 742	R95	Res. MC, 261 Ω, 1/4 W, 1%	31-223 261
66-304 735	R130	Res. MC, 10 K, 1/4 W, 1%	31-225 100
66-304 148	R113	Res. MC, 5.62 K, 1/4 W, 1%	31-224 562
32-301 510	R88	Res. MC, 17.8 Ω, 1/4 W, 1%	31-222 178
32-301 410	R81	Res. MF, 506 Ω, 1/4 W, 1%	31-223 806
32-301 247	R70	Res. MF, 562 Ω, 1/2 W, 1%	31-614 654
32-301 551	R71	Res. MF, 909 Ω, 1/2 W, 1%	31-614 653
	R109	Res. MF, 499 Ω, 1/2 W, 1%	31-614 655
32-301 456	R53	Res. MF, 32 K, .10%	31-239 053
	R58	Res. MF, 16 K, .10%	31-239 052
32-301 351	R63	Res. MF, 8 K, .01%	31-239 051
32-301 515	R69	Res. MF, 4 K, .10%	31-239 050
32-301 210	R75, R76	Res. MF, 2 K, .10%	31-239 059

10 BIT ADC MODULE, 03-950580 (Cont'd)

Schematic Reference	Description	Varian Part No.
R98, 102, 105		
106	Res. MF, 50 K, 1%	31-239 058
R105	Res. MF, 50 K, 1%	31-239 058
R6	Res. MF, 10.5 K, 1%	31-239 057
R77	Res. MF, 2 K, 1%	31-239 031
R3	Res. MF, 10 K, 1%	31-239 033
R18, 43	Res. MF, 128 K, .1%	31-613 344
R21, 48	Res. MF, 64 K, .1%	31-613 343
R52	Res. MF, 6.81 K, .1%	31-613 342
R57	Res. MF, 3.48 K, .1%	31-613 345
R62	Res. MF, 1.74 K, .1%	31-613 346
R24	Res. MF, 32 K, .1%	31-613 348
R5, R78, 25, 78		
101, 104	Res. VAR, W.W, 1 K	37-577 311
R8	Res. VAR. W.W., 50 Ω	37-577 308
R67, R73	Res. VAR. W.W., 200 Ω	37-577 310
R79, R99	Res. VAR. W.W., 50 K	37-577 315
R85	Res, VAR. W.W., 20 K	37-577 314
Q1	Transistor, 2N3906	62-903 906
Q2	Transistor, 2N3904	62-903 904
Q3, Q4	Transistor, Fet, U1897E	62-798 125
C1-19, 23, 25-29, 32-37, 41, 42, 46, 51-53	Cap. Cer, 1 μf, 200 V, 10%	41-228 009
C22	Cap. Cer, 1000 pf, 100 V, 5%	41-159 599
C30, C31	Cap. Mylar, .005 μf, 100 V, 1/2%	41-718 754
C38, C55	Cap. Cer, 5 pf, 500 V, 10%	41-159 505
C40, C54	Cap. Cer, 20 pf, 500 V, 5%	41-159 573
C43, 45, 49	Cap. Elect, 100 μf, 25 V	41-506 258
C44, 50	Cap. Elect, 25 μf, 25 V	41-506 255
C47	Cap. Cer, 130 pf, 500 V, 5%	41-159 566
C48	Cap. Cer, .1 μf, 25 V, 20%	41-206 993
JPR	Wire, Bus, Bare #24 AWG	81-099 924
JPR2	Wire, Bus, Bare #24 AWG	81-099 924
JPR4	Wire, Insul. Blk #24 AWG	81-293 700
JPR5(A-B)	Wire, Bus, Bare #24 AWG	81-099 924
JPR6	Wire, Insul, Red #24 AWG	81-293 702
JPR9	Wire, Bus, Bare #24 AwG	81-099 924
JPR10	Wire, Bus, Bare #24 AWG	81-099 924

USER'S GUIDE
DIGITAL-TO-ANALOG CONVERTER MODULE

for use with

Varian 620 or V73 Series Computers

Publication No. 03-996 805A

June 1973

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TABLES

FIGURES

1. INTRODUCTION

1.1 GENERAL

The Digital-to-Analog Converter (DAC) Module is a hardware option that interfaces Varian 620 and V73 series computers with external devices which require analog voltage as their inputs. DAC models are available to provide 10-bit, 12-bit, or 14-bit digital-to-analog resolution. A DAC module includes three functional features:

- One or two Digital-to-Analog (D/A) Converters, which convert digital data from the computer into equivalent analog voltage output signals.
- External Control (EXC) Interface Logic, which allows a computer program to control external devices via logic-signal output lines.
- Sense (SEN) Interface Logic, which allows a computer program to test the status of external devices by sampling logic levels present on Sense input lines.

The DAC's output capability may be expanded through the addition of Digital-to-Analog Converter Expansion (DACE) modules. Each DACE module provides two digital-to-analog converters. Up to three DACEs can be attached to each DAC. As many as eight DACs with 24 DACE modules can be attached to a single computer to provide the following I/O capability:

64 Analog Outputs	Each module (DAC and DACE) contains two digital-to-analog converters.
64 External Control Outputs	Each DAC contains eight External Control output lines.
64 Sense Inputs	Each DAC contains eight Sense input lines.

Simple installation procedures allow the DAC to be installed either at the factory or on-site at the user's facility. A comprehensive software test package is provided with the DAC for post-installation checkout of its operational status. In addition, the module is fully supported by standard Varian software and input/output options.

1.2 FUNCTIONAL DESCRIPTION

All elements needed to perform the module's three basic functions are packaged on a single plug-in printed circuit board. Figure 1-1 illustrates the functional elements included in a DAC module. A DACE contains only those elements shown in the shaded portion of Figure 1-1. Although the figure shows a DAC module which includes two digital-to-analog converters, some models of the DAC contain only one converter.

Device Address

The computer program must select a DAC by its device address before the module can perform any operation. There are eight device addresses (50_8 to 57_8) reserved for use by DACs. One DAC and three DACEs can be located at a device address; the DAC serves as the master module and contains the device address decode logic for the DACEs, which function as slaves to the DAC but provide the same basic conversion capability.

DAC Select

An individual D/A converter is selected by the computer program, using an Extended EXC (EXC2) instruction. There are eight DAC select lines at each device address; each line is enabled by the corresponding EXC2 instruction.

The master DAC module contains the DAC select logic for DACEs located at that device address. Once selected, a DAC remains selected until a different DAC at the same address is selected, until SYSTEM CLEAR occurs, or until power is interrupted.

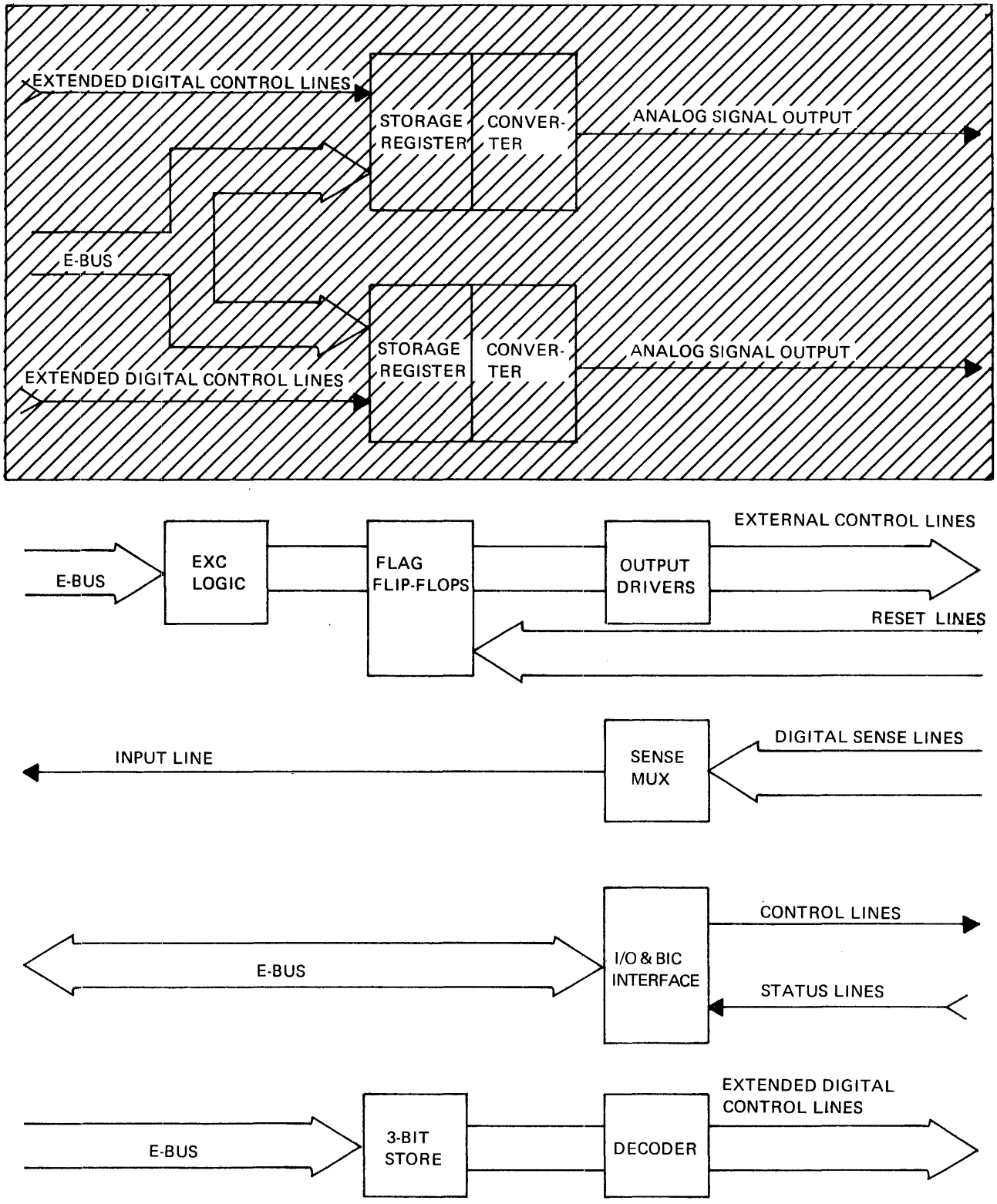


Figure 1-1. DAC Block Diagram

Buffer Enable Logic

The buffer enable logic is responsible for coordinating the transfer of data into the DAC buffer registers. If data transfer is under direct program control, the buffer enable logic exchanges data transfer control signals with the computer. When data transfer is under control of the Buffer Interlace Controller (BIC), special logic interfaces with the BIC.

Conversion

Digital data transmitted by the computer is gated into the addressed DAC's buffer register; the buffer data is immediately converted into a voltage signal by the D/A converter.

The converter output consists of a sequence of voltage levels which correspond to numbers transmitted by the computer. If the voltage changes are small enough, the converter output appears to the external device as an analog voltage curve rather than step value changes, as illustrated in Figure 1-2.

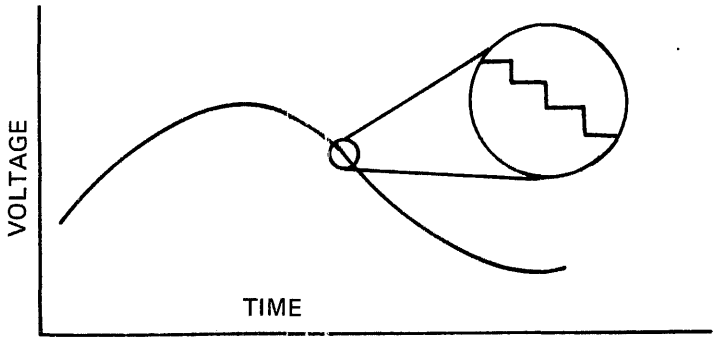


Figure 1-2. Analog Simulation by DAC Output

External Control (EXC) Interface

External Control Signals, which are generated by the computer to control operations in external devices, are distributed to the external devices via eight EXC output lines.

The DAC module's EXC interface logic selects one of the eight output lines according to the contents of the function code received from the computer. The master DAC contains all EXC interface logic for that device address.

Sense Interface

The DAC's Sense interface logic selects one of eight sense input lines according to the contents of the function code received from the computer. The logic level present on the selected line is gated to the computer. The master DAC contains all Sense interface logic for that device address.

2. PROGRAMMING

2.1 INTRODUCTION

This section describes Assembly Language programming techniques for operating the DAC module and presents instructions for using the DAC software test package for module checkout. In addition, this section describes the usage of two special driver programs which are supplied with the DAC. More detailed programming information may be found in the 620 series or V73 system handbooks.

A program directs DAC operation in three ways:

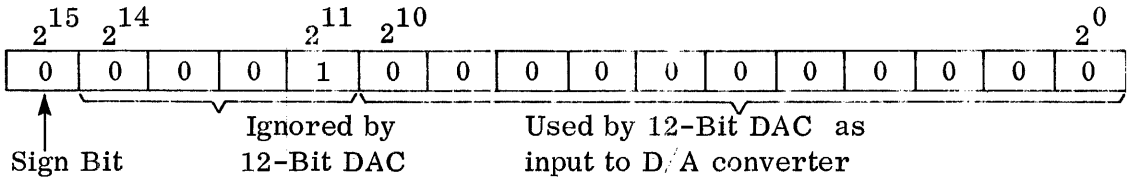
- Transfers data to the digital-to-analog converters.
- Distributes signals to External Control lines.
- Checks Sense input lines.

There are three basic factors to consider when writing a computer program to drive a DAC: data, timing, and hardware. Section 2.2 defines the restrictions placed on the numerical data which is generated by the computer program as input to the DAC. Section 2.3 discusses timing, which must be controlled by the program as it provides digital inputs for the DAC to generate real-time voltage output. Section 4 discusses the hardware capabilities of External Control and Sense lines, which should be evaluated by the programmer before setting up a permanent system.

2.2 INPUT DATA

The programmer may find it a useful precaution to check all DAC input data for numerical limits before it is transferred to the module. Table 2-1 provides the scale factor (F) which relates digital input (M) to the DAC with voltage output (V) from the DAC. M_+ to M_- are the maximum positive and negative numbers that will be converted properly.

If an attempt is made to convert numbers outside the range M_+ to M_- given in Table 2-1, the output voltage will be in error since the DAC assumes right-adjusted numbers with a high-order sign bit. For example, consider an attempt to convert +2048 to a voltage with a 12-bit DAC. In 2's complement binary +2048 is represented by:



Since a 12-bit DAC determines the output voltage magnitude from the 11 rightmost bits (2^0 to 2^{10}), 2048 would be read as 0.

Table 2-1. Numerical Properties of 10, 12, and 14 Bit DAC's

Number of DAC Bits	Scale Factor (F)	V_+ Volts	M_+ Decimal	M_+ Octal	V_- Volts	M_- Decimal	M_- Octal
10	1/512	9.980	511	777	-10.000	-512	177000
12	1/2048	9.995	2047	3777	-10.000	-2048	174000
14	1/8192	9.999	8191	17777	-10.000	-8192	160000

$V = FM$

Where
- V = Voltage Signal at DAC
- M = Digital Input to DAC
- F = Scale Factor
- V_+ = Maximum Positive Voltage
- V_- = Maximum Negative Voltage
- M_+ = Maximum Positive Digital Number
- M_- = Maximum Negative Digital Number

2.3 DATA TRANSFER UNDER PROGRAM CONTROL

The essential programming instructions for transferring data to a DAC are shown in Table 2-2. The instructions are given in the form of a block of code from a typical program.

An individual D/A converter is selected for a data transfer operation by means of an EXC2 instruction. For example, an instruction with the format EXC2 XYY selects converter number X at device address YY. Table 2-3 shows the converter number assignments for a device address. After a converter is selected, data is transferred to it by means of an OAR, OBR, or OME instruction.

Table 2-2. Instructions To Output Data Under Program Control

Program Step	Function
ONE LDA J	Load value of variable J into the computer A register. (LDB may be used instead of LDA.)
TWO EXC2 XYY	Select converter number X (0 to 7) at device address YY (50 to 57).
THRE OAR 0YY	Output data from A register to module at address YY (50 to 57). (OBR would be used if LDB had been used. OME could also be used to output data.)
(Time Delay Code)	(Timing data transfer to the DAC must allow for DAC settling time as discussed in Section 2.3.)
(Code To Generate Next Output Number)	
JMP ONE	

Table 2-3. D/A Converter Number Assignments

Module	D/A Converter Number
DAC (master)	0, 1
DACE (first slave)	2, 3
DACE (second slave)	4, 5
DACE (third slave)	6, 7

When an individual converter is selected at a particular device address, it remains selected until another EXC2 instruction selects a different converter at the same device address. For example, assume the following sequence of coding:

EXC2	053	Select First Converter on First Module at Device Address 53.
•		
•		
•		
EXC2	253	Select First Converter on Second Module at Device Address 53. This changes the selection specified by the previous EXC2 since both DACs are located at the same device address.
•		
•		
•		
EXC2	252	Select First Converter on Second Module at Device Address 52. This has no effect on the previous EXC2 instructions since the DACs are located at different device addresses.

Thus it is possible to select one D/A converter at each device address. The following example illustrates the selection and usage of converters at three different device addresses:

EXC2	050	Select First Converter on First Module at Device Address 50.
EXC2	351	Select Second Converter on Second Module at Device Address 51.
EXC2	453	Select First Converter on Third Module at Device Address 53.
LDA	V1	Load Variable V1 into Computer Register A.
LDB	V2	Load Variable V2 into Computer Register B.
OAR	050	Output V1 to selected DAC at Device Address 50.
OBR	051	Output V2 to selected DAC at Device Address 51.

```
        LDA     V3              Load Variable V3 into Computer Register A.

        OAR     053             Output Variable V3 to Selected DAC at Device
                                Address 53.
```

Timing is an essential part of programming data transfers to a DAC. There are two types of timing to be considered:

1. Settling-time delay, which is determined by the maximum rate at which a DAC can receive and accurately convert data, and
2. Real-time delay, which is a function of the required real-time DAC output voltage signal.

The maximum settling time for a DAC (when switching from minus full scale to plus full scale) is 20 microseconds.

Under program control, one data transfer is possible in every four cycles (for example, every 3.0 microseconds on the 620/f-100 computer). If the DAC is to provide an accurate analog representation of the digital data, settling-time delay should be provided so that the interval between successive data transmissions to the DAC is greater than 20 microseconds.

Some examples of steps to provide time delay include:

1. A number of NOP instructions for short delays.
2. An indexed loop for longer delays.
3. Use of a real time clock.
4. Use of an external clock and sense lines.

The following example illustrates the use of an indexed loop to provide a time delay:

```
        LDX     IND             Load Index Value into X Register.

ONE     DXR                     Decrement the Index.
```

```
JXZ     TWO     Jump Out to TWO when Index Equals Zero.
JMP     ONE     Jump Back to ONE.
```

Note that settling-time delay may not be the same as the real-time delay required to generate a real-time voltage signal. The following considerations affect real-time delay:

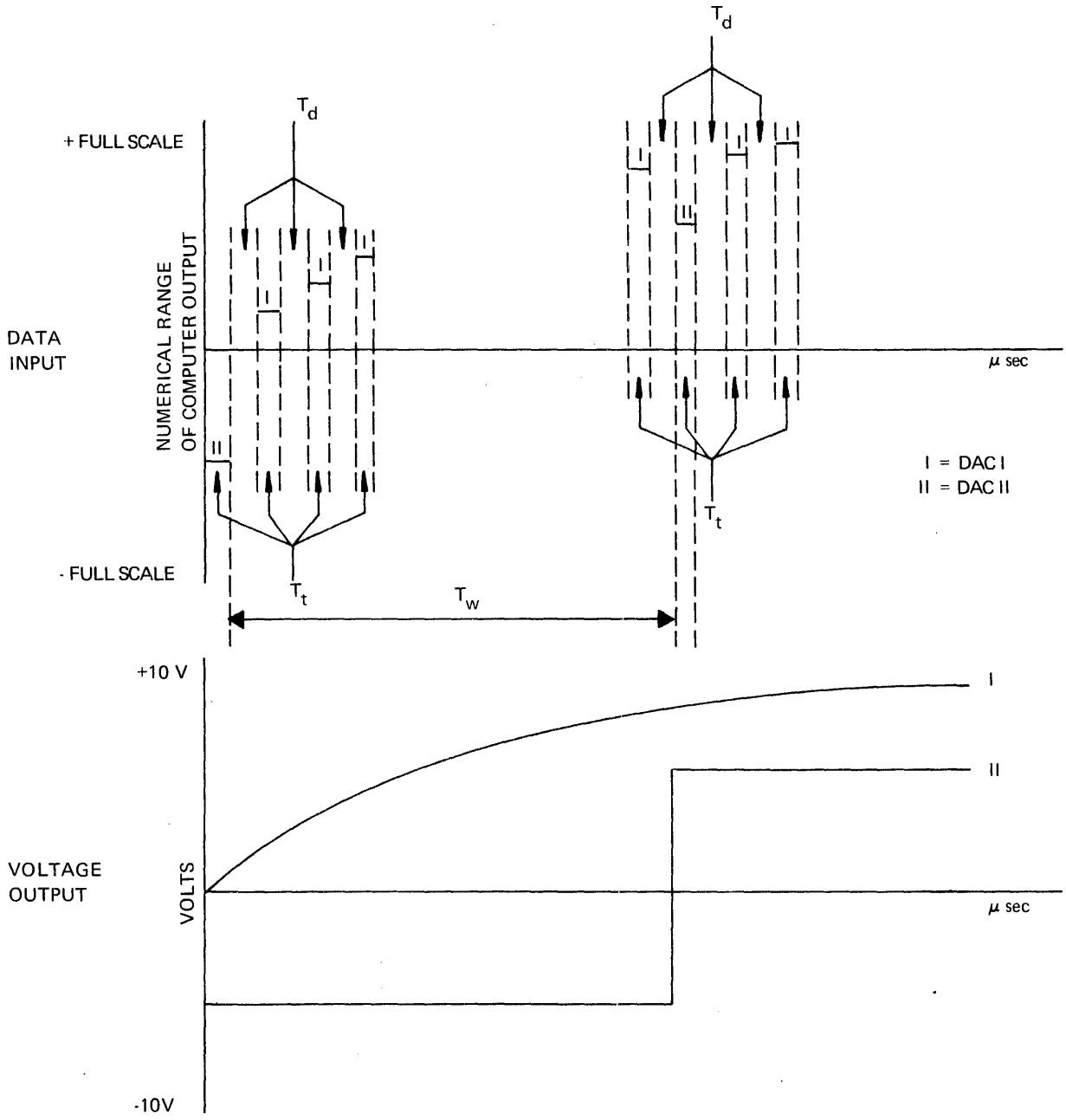
1. If data is being transferred to more than one DAC, then provision must be made for the time required to execute instructions that transfer data to other DAC's in the cycle.
2. Real-time delay should usually be greater than or equal to settling time delay.

Figure 2-1 illustrates settling-time delay and real-time delay for two voltage signals being generated simultaneously. Signal I is continuous, and requires the maximum data transmission rate; only settling-time separates these successive digital data inputs to DAC I. Signal II is a step function; it requires an initial signal at time zero and a reset signal after some real-time delay. The real-time delay in this example is computed using the cycle times of the program steps necessary for each data transfer. Lengthy real-time delays are more frequently controlled by an external clock, using a Sense line to initiate data transfers.

2.4 PROGRAMMING EXAMPLE

The following short program creates ramps via the A and B registers, and uses the X register to develop a time step during which the current contents of the A and B registers are output to two D/A converters.

```
ONE     LDBI    01777       Load A and B Registers.
        LDAI    0177000
```



T_t = TIME TO TRANSMIT ONE NUMBER TO DAC (μ sec.)
T_d = DESIRED MINIMUM DELAY BEFORE TRANSMITTING ANOTHER NUMBER TO THE SAME DAC.
T_w = DESIRED TIME DELAY BETWEEN TRANSMITTING TWO NUMBERS TO GENERATE SIGNAL (II).

Figure 2-1. Time Delays Required - 2 Voltage Signals/1 Program

```
TWO     EXC2    050     Load Contents of A Register into D/A
        OAR     050     Converters 0 and 1 Device
        EXC2    150     Address 50.
        OAR     050
        LDXI    0100    Inititalize X Register.
TRE     DXR             Decrement X Register.
        JXZ     GO      Branch Out if X Register is Zero.
        JMP     TRE     Return to X Register Decrement.
GO      IAR             Increment A Register.
        DBR             Decrement B Register.
        JBZ     ONE     Return to ONE If B Register
        JMP     TWO     is Zero; otherwise Return to TWO
```

2.5 DATA TRANSFER WITH BUFFER INTERLACE CONTROLLER

The Buffer Interlace Controller (BIC) is a hardware option which allows the user to transfer a block of data to or from a peripheral device using only one set of instructions. The user loads the first and last memory address location for a data block into special registers in the BIC; the BIC then transfers the specified data block to (or from) the peripheral device. Since data is transferred to a DAC, only this direction of data flow is considered in this section.

Once a program initiates the BIC data transfer, the BIC operates in parallel to the computer program, stealing cycles to read data from memory via direct memory access. The program can, therefore, proceed independently with other processing.

Typically, the program instructions for initializing a BIC are coded as a separate subroutine. The applications program then calls this subroutine when BIC usage is required. Table 2-4 illustrates the coding of a BIC initialization subroutine and demonstrates the usage of the subroutine within an applications program. This example assumes the BIC is assigned device address 20, 21 octal; the sequence of operations is as follows:

BIC Subroutine -

1. Sense that BIC is not busy, using a standard SEN 020 instruction. The BIC cannot be initialized while it is busy. If busy, loop until BIC completes its operation.

2. Initialize the BIC, using a standard EXC 021 instruction.

3. Store data block's initial and final addresses in the appropriate BIC address registers.

4. Enable the BIC for connection to device which will initiate the data transfer.

Applications Program -

1. Call BIC subroutine.

2. Check readiness of peripheral device that is to receive analog data from the DAC. Sense line M (0 to 7) at device address NN (50 to 57) is used to declare the device's status. Loop if device is busy.

3. Connect BIC to DAC, using an EXC instruction to initiate data transfer. An EXC 0YY instruction, where YY is the DAC device address, is used to output data. An EXC 1YY instruction is used to read gated input data.

4. The data block transfer will be complete when the BIC is, again, "not busy." The applications program may perform other processing and subsequently use SEN 020 and SEN 021 instructions to check for BIC-not-busy and BIC-abnormal-halt conditions.

Note that the BIC initial and final register addresses may be any pair of octal numbers in the range 20 through 27. Ordinarily, in systems employing more than one BIC, addresses 20 and 21 are assigned to the first BIC's registers; 22 and 23, 24 and 25, and 26 and 27 are assigned to the second, third, and fourth pairs of registers, respectively.

Table 2-4. Example of Instructions To Output Data Under BIC Control

Program Step			Function
BIC Subroutine -			
BICS	ENTR	0	
WAIT	SEN	020, GO	Go when BIC not busy.
	NOP		
	NOP		
	JMP	WAIT	
GO	EXC	021	Initialize BIC.
	OME	020, FIRST	Set start address of memory block.
	OME	021, LAST	Set end address of memory block.
	EXC	020	Enable BIC.
	RETU*	BICS	
Applications Program -			
	CALL	BICS	Set up BIC.
BUSY	NOP		
	NOP		
	SEN	MNN, BUSY	Loop if device busy.
	EXC	050	Connect BIC to DAC
	•		
	•		
	•		

2.6 EXTERNAL CONTROL

External Control signals may be generated by a computer program to provide a variety of logic controls for external devices.

The user has eight External Control lines available at each master DAC module. The instruction that causes an External Control Signal is:

EXC XYY

where X (0 to 7) defines one of eight External Control lines at DAC device address YY (50 to 57).

The signals are also made available to the backplane connectors so that they may be used to control certain portions of DAC logic when required by the use of an option such as the BIC. This use of External Control signals will depend on specific applications of the DAC module.

A program can set, but cannot reset, an External Control signal; reset is a function of external hardware. As determined by external interconnections, one External Control signal can reset another, other external electronic components can control reset, or the External Control signal can reset itself (pulse operation). Several methods for resetting External Control output signals are discussed in this section. These methods illustrate how the program can use the EXC command to trigger sequences of operations that have been predetermined by system hardware interconnection. The wiring configurations for these methods are illustrated in Figures 2-2 through 2-7. In all cases, some external wiring is required; the external modifications for each method are shown to the right of the vertical dashed line in each figure. Section 4.3 discusses the circuit logic for these reset types.

Command Sequence Reset

By connecting the EXC-N output of one latch to the REX-M of another latch, selecting the first will reset the second. This requires that the function codes in a series of EXC commands always follow the sequence prescribed by the latch interconnections. Figure 2-2 illustrates one configuration. In this example, the command sequence would progress from EXC-0 to EXC-7.

For example, in the following sequence of instructions used with this configuration, one External Control line resets one other line.

EXC	050	EXC 750 is automatically reset, EXC 050 is set.
EXC	150	EXC 150 is automatically reset, EXC 150 is set.
EXC	250	EXC 150 is automatically reset, EXC 250 is set.

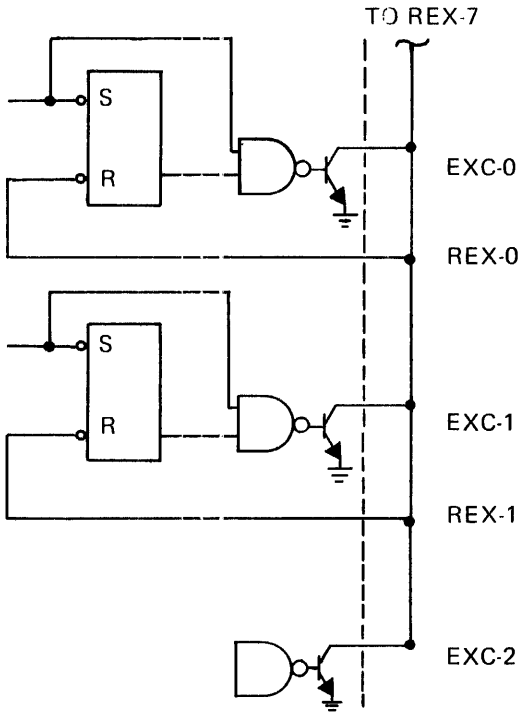


Figure 2-2. Command Sequence Reset Wiring

Special Assignment Reset

One latch can be assigned as the reset latch. An EXC command selecting that latch will then reset all other EXC latches. Figure 2-3 illustrates this configuration. The following sequence of program instructions used with this configuration functions as follows:

EXC	050	Set EXC 050.

EXC	150	Set EXC 150.
EXC	250	Set EXC 250.
EXC	750	EXC 050, EXC 150, and EXC 250 are automatically reset.

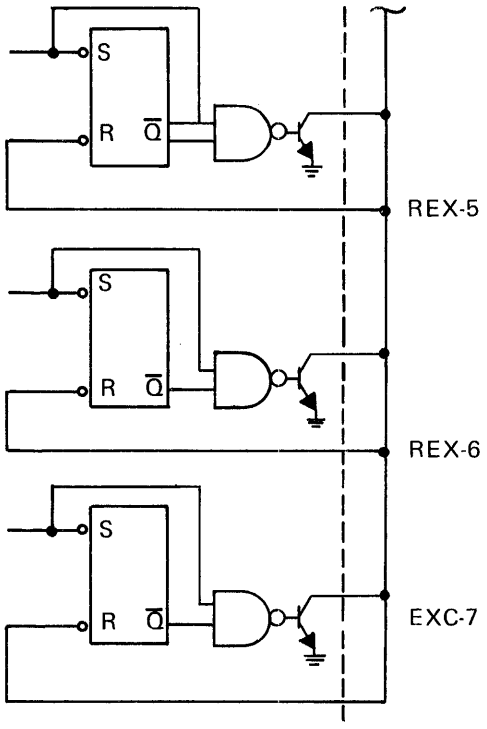


Figure 2-3. Special Assignment Reset Wiring

Fixed Delay Reset

An EXC latch can reset itself, following a suitable delay provided by an RC, transmission line, or other delay circuit. Figure 2-4 illustrates a typical latch circuit with an RC delay. An example of an instruction which can be used with such a configuration is as follows:

EXC	050	EXC is set for nn microseconds, then resets itself. (nn is determined by delay hardware added to the EXC output.)

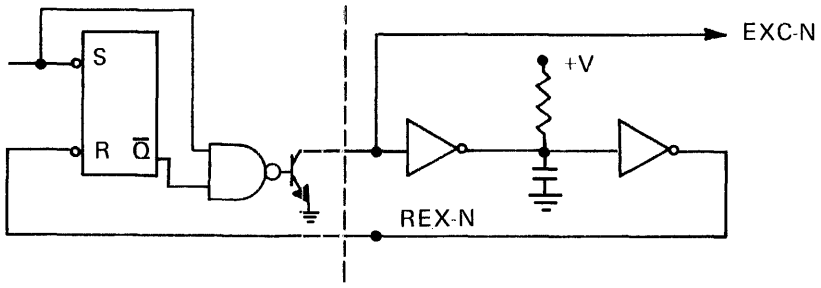


Figure 2-4. Fixed Delay Reset Wiring

Reset Returned By Receiving Device

The reset signal can be returned by the receiving device as shown in Figure 2-5. In this case, the pulse width is determined by the cable length. This insures that the pulse width is great enough for proper reception, regardless of cable capacitance.

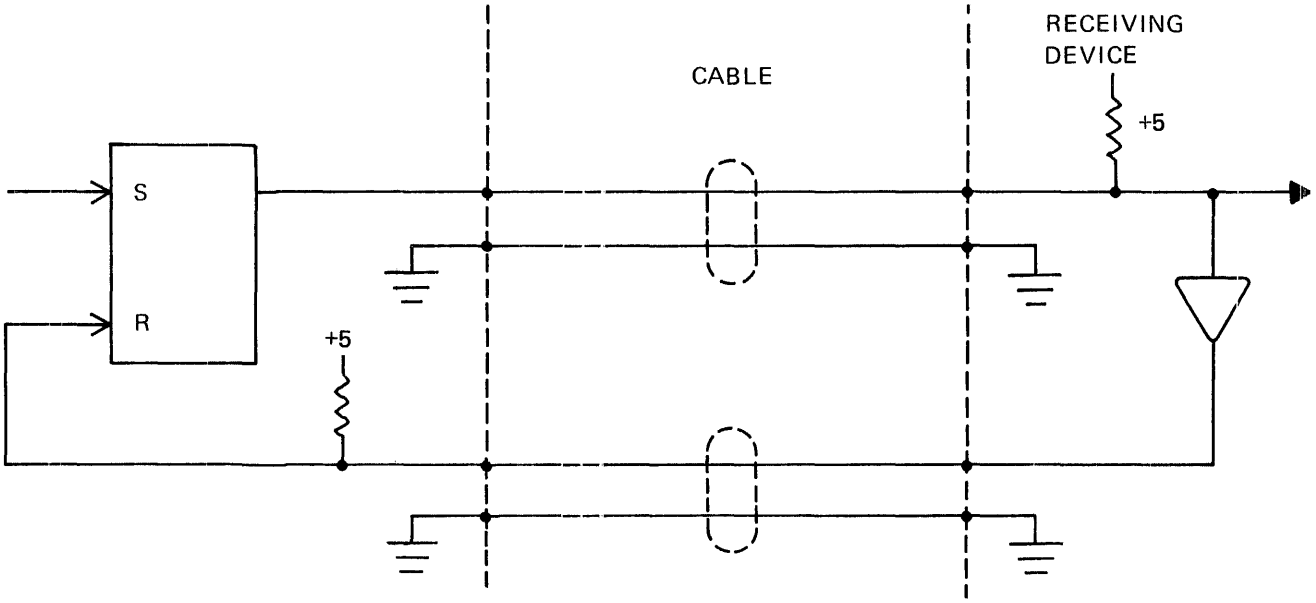


Figure 2-5. Reset Returned By Receiving Device

Automatic Reset

Connecting a REX-N output to ground will cause the EXC-N output to reset as soon as the EXC input to the latch goes false. In the 620/L-100 computer, this produces a 200 nanosecond pulse. (The pulse duration will differ slightly for other computers.) Figure 2-6 illustrates such a configuration. In this configuration, an EXC is set, and then reset after 200 nanoseconds. This is accomplished by making the EXC latch output follow the latch input, which is a 200 nanosecond pulse. Normally, the input pulse causes the EXC to be set "on", but the input pulse in no way influences resetting the EXC to "off".

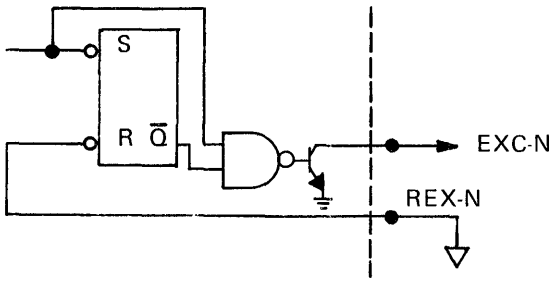


Figure 2-6. Automatic Reset Wiring

External Logic Reset

In this case, the flip-flop is set by the program and reset by the external device. This is especially useful in passing data or control commands; the program sets the EXC flag to indicate that data is ready, and the external device resets it to acknowledge that it has received the data or that it is ready to accept additional data. The EXC output is connected to a Sense input as well as to the external device, so the program can

determine that the acknowledgement has been received. (See Figure 2-7.) The same scheme can, of course, be used for receipt of data by the computer.

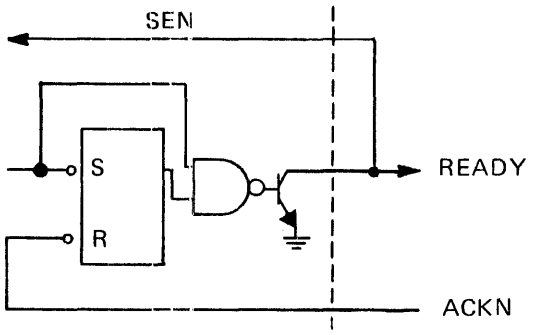


Figure 2-7. External Logic Reset Wiring

External Control Usage With BIC

Table 2-5 illustrates a program utilizing External Control Line 253 to connect the BIC to the DAC module located at device address 53. (Note that this would also require a jumper from EXC 253 to signal EPO-N, as discussed in Section 5.2). Statement FIVE connects the DAC at device address 53 to the BIC (assuming External Control line 2 at device address 53 has been connected to EPO-N of the BIC enable logic). Statement SIX resets EXC 253, then resets itself after a short delay. Figure 2-8 shows the logic that would be needed by the program in Table 2-5.

2.7 SENSE LINES

Sense lines allow the program to sense a signal from an external device, and branch depending on whether a Sense line is true or false.

There are eight external sense lines associated with each DAC device address. The command which selects a Sense line is:

SEN XYY

X (0 to 7) defines a specific line at device address YY (50 to 57).

Table 2-5 illustrates three uses of the SEN statement. Statement TWO inhibits data transfer via the BIC until Sense line 4 at device address 50 is sensed "false". The other two SEN statements are BIC system commands. (See 620 series or V73 system handbooks.)

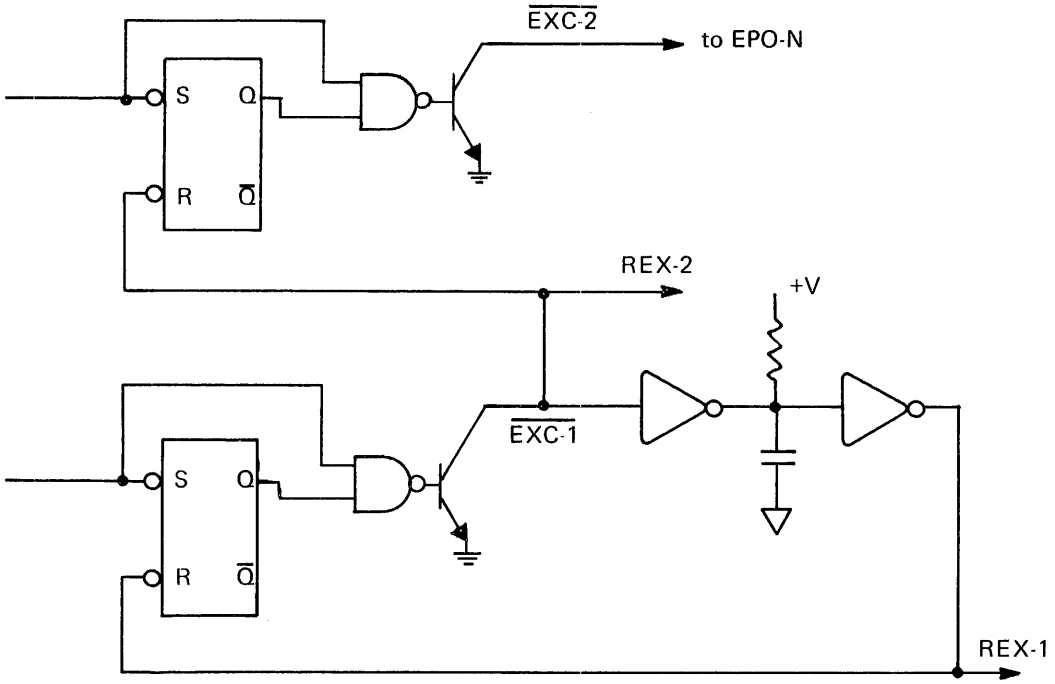


Figure 2-8. External Control To Connect and Disconnect BIC

Table 2-5. Use of External Sense Logic

Program Step			Function
WAIT	SEN	020, ONE	Sense BIC not busy.
	NOP		
	NOP		
	JMP	WAIT	
ONE	EXC	021	Initialize BIC.
	OAR	020	Output start address to BIC register.
	OBR	021	Output end address to BIC register.
	EXC	020	Enable BIC
NOP	NOP		
	NOP		
TWO	SEN	450, NOP	Start data transfer when Sense line 4 at device address 50 is "false". Branch back if "true."
FIVE	EXC	253	Connect BIC to DAC.
	SEN	021, TEN	Check for abnormal stop.
SIX	EXC	153	Reset EXC 253.

2.8 DAC SOFTWARE DRIVERS

Two driver programs are supplied to provide convenient access to digital-to-analog converters without detailed knowledge of hardware. These drivers may be used by themselves or embedded in an operating system.

The drivers and their functions are:

PDAC	Provides programmed data transfers.
DDAC	Provides direct memory transfers.

These drivers assume standard device address assignments (50_8 to 57_8) for the DAC modules. If other device addresses are used for DAC's, the drivers must be reassembled.

The drivers assume the following device address assignments for BICs:

Address (Octal)	Device
020 - 021	BIC, No. 1
022 - 023	BIC, No. 2
024 - 025	BIC, No. 3
026 - 027	BIC, No. 4

Programmed Data Transfer

The PDAC driver provides programmed data transfers to a selected DAC. A variable number of 16-bit words are transferred each time the driver is called. The time interval between data transfers is approximately 20 microseconds.

PDAC is called with the following assembly language sequence:

```
CALL PDAC, DACNR, NUM, SOURCE, EXIT
```

All entries in the calling sequence are either direct or indirect addresses which point to the actual arguments. Multiple levels of indirect addresses are permitted. The arguments are defined as follows:

DACNR - An integer value which specifies the D/A converter to which data is to be transferred. The range of DACNR must be between 1 and 64, inclusive; otherwise control passes to EXIT. The DACNR arguments correspond to the actual device address codes as follows:

DACNR	Device Address
1	050
2	150
3	250
•	•
•	•
•	•
9	051
•	•
•	•
•	•
64	757

NUM - An integer value which specifies the total number of 16-bit words to be transferred to the selected DAC.

SOURCE - The values in the SOURCE vector represent the data which is to be transferred to the selected DAC. Care should be taken to insure that integer data does not exceed the limits of the DAC size.

EXIT - The start address of the user's error routine. Control is transferred to EXIT when illegal input arguments are detected.

Programmed Data Transfer Example

The following example illustrates the use of PDAC. In this example, one word is transferred to DAC number 63 (device address 657 octal).

```
        CALL PDAC, = 63, = 1, WORD, ERROR
          •
          •
          •
ERROR   HLT         Error Exit
          •
          •
          •
WORD    DATA 10     Data Word to be Transferred
          •
          •
          •
```

Direct Memory Data Transfer

Two programs, DDAC and SDAC, are provided to utilize the BIC to transfer data directly from memory to a selected DAC without programmed intervention. DDAC and SDAC offer two advantages over PDAC:

- Data transfer rates are not limited by software overhead.
- The applications program is freed to work on other processes while the BIC supervises and controls the data transfer.

Unlike other peripherals, DACs do not have built-in logic to determine when the next data item should be transferred to them. Therefore, external hardware must be provided to indicate when data from memory is to be transferred to the DAC. This is accomplished by providing a Data Ready line at P1-73 on the computer backplane. The data transfer timing is completely under the control of this external control line.

In addition to this external signal, one of the eight EXC outputs on the master DAC module must be dedicated, and a jumper must be placed between P1-101 and P1-79. This provides a BIC connect function for the selected DAC. The DDAC driver uses the following EXC's for this function:

DACNR	EXC Used For BIC Connect
1-8	EXC 050
9-16	EXC 051
17-24	EXC 052
25-32	EXC 053
33-40	EXC 054
41-48	EXC 055
49-56	EXC 056
57-64	EXC 057

J1-9 also must be grounded so that the flip-flop associated with EXC 0XX is automatically reset.

Direct memory data transfer to a DAC is accomplished by a two-step process. First DDAC is called to initiate the transfer and return control immediately. Then, SDAC is called at the user's convenience to determine when the transfer is complete.

DDAC Driver

The DDAC driver is called with the following assembly language sequence:

CALL DDAC, BICNR, DACNR, NUM, SOURCE, EXIT

All entries in the calling sequence are either direct or indirect addresses of the arguments. Multiple levels of indirect address are permitted. The arguments are defined as follows:

BICNR - An integer value which specifies the BIC to be used for data transfer. The range of BICNR is from 1 to 4 corresponding to BIC device addresses $20\text{-}21_8$ through $26\text{-}27_8$. A value outside the legal range causes control to pass to EXIT.

DACNR - An integer value which specifies the individual D/A converter to be selected. The range of DACNR must be between 1 and 64 inclusive; otherwise control passes to EXIT. (See PDAC driver for a description of DACNR and actual device address relationship.)

NUM - An integer value which specifies the total number of 16-bit words to be transferred to the selected DAC.

SOURCE - The values in the SOURCE vector represent the data which is to be transferred to the selected DAC. Care should be taken to insure that integer data does not exceed the limits of the DAC size.

EXIT - The start address of the user's error routine. Control is transferred to EXIT when illegal input arguments are detected.

SDAC Routine

The SDAC routine checks the status of a previously-initiated direct memory data transfer. SDAC is called with the following assembly language sequence:

```
CALL SDAC, STATUS
```

The single entry in the calling sequence can be either a direct address or an indirect address which points to the actual argument. The argument is defined as follows:

STATUS - This argument receives a value of 0, 1 or 2 to indicate the status of the transfer operation:

Value	Meaning
0	Operation not complete
1	Operation complete; no errors
2	Operation aborted

Direct Memory Transfer Example

The following example illustrates the use of DDAC and SDAC. In this example, a sequence of numbers (0, 1, 2, . . . 100) is transferred to D/A converter number 10 (which is located at device address 0151). The transfer rate is determined by external hardware, and the transfer is performed by the BIC at device address 24_8 - 25_8. The program steps are as follows:

```
CALL DDAC,  = 3, = 10, = 101, RAMP, ERR
   •
   •
   •                    (Concurrent Processing)
```

```
WAIT    CALL SDAC, STATE        Check Status.
        LDA STATE               Test Status Word.
        JAZ WAIT                If Not Complete, Continue Wait.
        DAR                     If Complete, Check for Normal Completion.
        JAZ ...                 Normal Completion, Jump to Other Processing.
        JMP ERR                 Error.
ERR     HLT
RAMP    DATA 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10
        DATA 11, 12, 13, 14, 15, 16, 17, 18, 19, 20
           •
           •
           •
        DATA 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100
```

2.9 TEST PROGRAMS

A set of test programs is provided for DAC checkout. The set consists of three programs which may be selected through the Maintain II Test Executive. The programs, numbered 0 through 3, are as follows:

Test No.	Description
0	Returns control to the Test Executive Program.
1	Tests External Control and Sense lines.
2	Tests digital-to-analog converters.
3	Tests BIC interface.

These programs may be selected in any order and may be run as often as desired. This allows DACs with different device codes to be tested.

The minimum computer configuration on which the tests may be run is a 620 or V73 series computer with 4 K of memory, a teletype terminal, and a DAC card. In addition, a DAC test shoe (Part No. 03-950225) is required for running the tests.

Supervisor Program

A simple supervisor or test program selector is provided as part of the test package to allow the user to select individual tests and return control to the Test Executive

Program. The Test Executive Program is a standard Varian software option which must be loaded and run prior to the initiation of the DAC test package. Instructions for operating this program are given in the Test Program Manual (Publication No. 98A 9952-061). The DAC test package is loaded through the Test Executive.

When the Test Executive Program is running, the "L" command may be used to load the test package and transfer control to its supervisor. If the test package is already loaded, the "G500" command may be used to transfer control to the supervisor.

When the supervisor is activated, it responds by issuing a carriage return/line feed and by starting to print a series of prompting messages. The user must enter a valid response to each message as it is printed. An invalid response causes the message to be repeated. The first message is:

```
EXC, SENSE AND DAC TEST SUPERVISOR
ENTER DAC DEVICE ADDRESS?
```

The user must enter the DAC device address, which is an octal number between 050 and 057, followed by a period. The supervisor will then print:

```
ENTER BIC DEVICE ADDRESS?
```

The user must enter any of the following assigned octal numbers: 020, 022, 024, or 026 followed by a period.

The DAC and BIC device addresses entered at this time will be used throughout the three tests, where applicable. To change device address selections, the supervisor must be reactivated from the Test Executive Program or run from location 500. After the device addresses have been entered, the supervisor will print:

```
ENTER TEST NO. ?
```

The user should enter any number between 0 and 3 followed by a period. The supervisor will then transfer control to the selected test program, which will identify itself and perform its specified functions.

Test 1 should be used for each master DAC module to test the EXC and SENSE logic.

Test 2 should be used for each D/A converter in the system.

Test 3 should be used to check the BIC interface to the DAC's and should be exercised on each DAC that will be driven under BIC control.

Sense Switches

During all DAC tests, the sense switches may be used to control the mode of operation. The normal mode is followed when all switches are OFF; one or more switches may be set to control operation as follows:

SS1 — Sense switch 1 suppresses teletype printouts of test results and error messages. This function is useful to speed up the continuous execution of a test so that an oscilloscope may be used to monitor signals.

SS2 — Sense switch 2 causes a test to repeat indefinitely without user intervention.

SS3 — Sense switch 3 terminates execution of a test and returns control to the supervisor. If sense switch 3 is set when the supervisor requests a new test number, the following message will be printed:

RESET SENSE SWITCH 3

A new test may be selected after SS3 is reset.

Test 1 - External Control and Sense Test

This test uses a special test shoe which must be plugged into J1 and J2 of the DAC card. The test checks all EXC and Sense lines on a given device address. The test shoe is designed to connect each EXC output to a Sense input and to reset another EXC according to the following table.

EXC Output	Sense Line	EXC Reset
00XX	07XX	05XX
03XX	04XX	00XX
04XX	03XX	03XX
01XX	06XX	04XX
02XX	05XX	01XX
06XX	02XX	02XX
07XX	01XX	06XX
05XX	00XX	07XX

Therefore, at each step in the table only one of the Sense lines should be true at a time. All Sense lines are polled after each step and errors are reported if detected and if sense switch 1 is reset.

When the test program is activated, it will print:

EXTERNAL CONTROL AND SENSE TEST

If no errors occur during the execution of the test, the program returns control to the supervisor after printing the following message:

TEST PASSED

If errors occur during the test, one or more of the following messages will be printed:

EXC 00XX OR SEN 07XX ERROR
EXC 03XX OR SEN 04XX ERROR
EXC 04XX OR SEN 03XX ERROR

EXC 01XX OR SEN 06XX ERROR

EXC 02XX OR SEN 05XX ERROR

EXC 06XX OR SEN 02XX ERROR

EXC 07XX OR SEN 01XX ERROR

EXC 05XX OR SEN 00XX ERROR

If the first error occurs, the problem may be in the address decoder logic on the master DAC card.

Test 2 - DAC Test

Each DAC card has two digital-to-analog converters. For purposes of these tests the converters at a particular device are numbered as shown in Table 2-3.

The DAC test program provides for the checking of any of 64 DACs, one at a time. The test provides a full scale negative to full scale positive ramp in one count increments.

Ten, twelve, and fourteen-bit DAC's may be tested with this program. The following table shows the plus full scale and minus full scale values for each DAC size.

No. of Bits	+Full Scale	-Full Scale	Signal Rep Rate (Hz)
10	511	-512	139.3
12	2047	-2048	34.7
14	8191	-8192	8.7

When the program is activated, it will print:

DAC RAMP TEST

ENTER DAC NO. ?

The user must enter any number from 0 to 7 followed by a period. The test program then requests the DAC size:

ENTER NO. OF BITS?

The user must enter the appropriate DAC size, either 10, 12, or 14 followed by a period.

The ramp will be continuously generated until sense switch 3 is set. No errors are generated by the test program. An oscilloscope may be used to monitor the voltage and check that the DAC functions properly. The DAC outputs are on J2-1 for even numbered DACs and J2-43 for odd numbered DACs. All other terminals on the J2 connector are at analog ground.

Test 3 - BIC Interface Test

This test exercises the BIC interface by outputting data to the DAC under BIC control. A monotonically decreasing bipolar waveform consisting of eighteen data points is output to the DAC through the BIC. The waveform starts at full scale and decreases to zero.

EXC 0 on the DAC is used to connect the DAC controller to the BIC. To provide for this, P1-101 must be wired to P1-79.

The BIC transfers a word of data to the DAC controller whenever the DEVICE READY line (P1-73) goes low. To keep more than one word from being transferred, this signal may go low for only one machine cycle. EXC 5 is used to control this function in conjunction with EXC 0. EXC 5 (P1-87) is wired to DEVICE READY (P1-73). EXC 0 resets EXC 5 and causes the trap out. EXC 5 is given directly thereafter to inhibit further trap outs.

EXC 5 is used in this fashion for test purposes only and the jumper from P1-87 to P1-73 should be removed after the testing is completed.

When the test program is activated, it will print:

```
DAC - BIC TEST
ENTER DAC NO. ?
```

The user must enter the appropriate DAC number from 0 to 7 followed by a period. The test program then requests the DAC size:

ENTER NO. OF BITS

The user must enter the appropriate DAC size, either 10, 12, or 14 followed by a period.

The waveform will be continuously generated until sense switch 3 is set. No errors are generated by this program.

3. THEORY OF OPERATION

3.1 DATA CONVERSION NETWORK

The DAC output voltage is provided by an operational amplifier whose input is the sum of a set of scaled currents (see Figure 3-1).

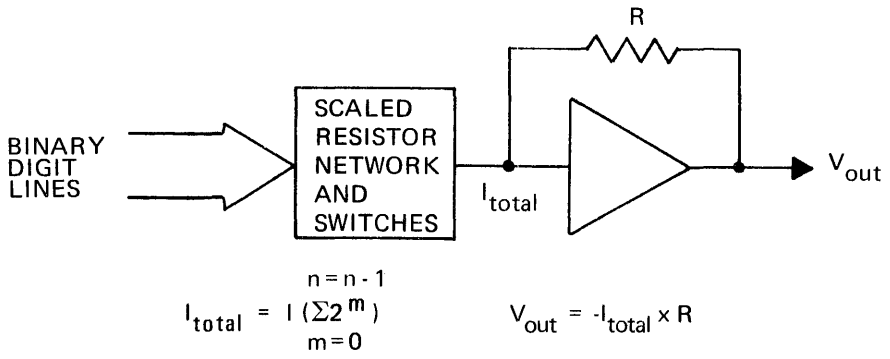


Figure 3-1. Basic DAC Simplified Diagram

The individual scaled currents are provided by current switches arranged in a ladder network.

Each switch is controlled by a different bit of the data word received from the computer. A relative-high output from the data buffer register in a bit position turns the corresponding switch on, adding its weighted current to the total current. A relative-low output turns the switch off so that it contributes no current to the sum.

3.2 DAC SWITCHES

Figure 3-2 represents a single DAC switch; the reference designators are arbitrary and do not apply to any actual assemblies. Refer to Appendix C for detailed schematics of the DAC switches.

When a data bit out of the buffer register is relative-high (approximately +4 Vdc), current steering diode CR1 is reverse biased. This directs current flowing through precision resistor R1 to the virtual ground summing junction. When a data bit out of the buffer register is a relative-low (approximately +0.5 Vdc), CR1 is forward biased and current from R1 flows through CR1 to the -15 Vdc sink; no current flows to the summing junction. The voltage levels present at the cathode of CR1 are approximately +1 Vdc when the data bit is high and approximately -1 Vdc when the data bit is low.

The value of precision resistor R1 determines the current through the switch and, consequently, the amount of current that switch adds to the summing junction. The precision resistor for each switch is scaled to provide an amount of current corresponding to the weighted value of the bit position controlling that switch.

CR2 and CR3 are matched diodes that, together, cancel the effect of temperature variations on the voltage drop across the switch.

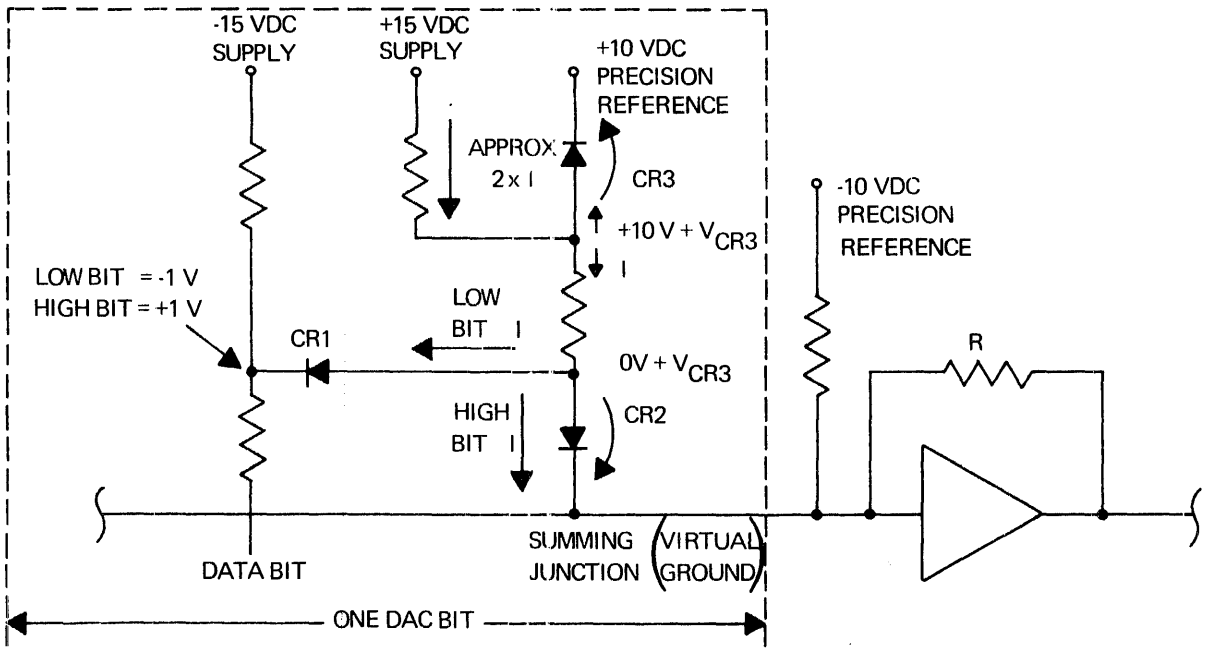


Figure 3-2. Current Steering Switch

3.3 SWITCH LADDER

A DAC may have any one of three resolutions: 10, 12, or 14 bits. The switch ladder schematic shown in Appendix C represents a DAC with 14-bit resolution. The current switches are arranged in a ladder network.

The amount of current added to the summing junction by a switch is directly proportional to the relative significance of the bit controlling that switch. The least significant bit controls the switch that supplies the least amount of current. The most significant data bit controls the second-most significant switch, with the sign bit controlling the most significant switch.

For DACs of 12- or 10-bit resolution, the two or four most significant switches are deleted. Since the sign bit must be preserved, a jumper connection at the buffer register input directs that bit to the most significant switch regardless of the DAC's resolution.

The three most significant switches on 14-bit DACs include calibration resistors. The values of these resistors are set during final assembly according to the results of a computer calibration program. Although field calibration is not normally required, these resistors may be adjusted to assure specified accuracy for these switches.

An attenuating resistor network, in series with the six least significant switches, allows the use of smaller values than would otherwise be required for these positions.

3.4 POWER SUPPLIES AND REFERENCE VOLTAGES

Two regulated power supplies, +15 Vdc and -15 Vdc, are provided by circuits located on a power supply module.

The +10 Vdc and -10 Vdc precision references are provided by voltage supplies contained on the DAC module. If two converters occupy the same module, they share the same reference voltages.

Output of the minus reference, as measured at its test point, is within the range +8.5 Vdc to +9.5 Vdc. This output is stable to within $\pm$0.1 mV. Coarse and fine adjustments set the amount of constant offset current provided to the summing junction from the minus reference. With all switches open, this offset current is provided entirely by the output amplifier feedback loop, and the amplifier output voltage is at + full scale.

Output of the plus reference source is +10 Vdc $\pm$0.1 mV. The feedback resistance of this circuit may be calibrated with both coarse and fine adjustment.

3.5 OUTPUT AMPLIFIER

The output amplifier converts the switch current sum to an inverted voltage output with a gain of one. Resistance values of the amplifier's feedback loop, the minus reference load and the sign bit switch are nominally equal.

When all current switches are open, output of the amplifier is plus full scale (approximately +10 Vdc) and full current flows from the amplifier output through the feedback loop to the minus reference. When all current switches are closed, amplifier output is at minus full scale (-10 Vdc) and full current flows from the summing junction through the feedback loop to the amplifier output. The crossover point (0 Vdc) is produced when the sign bit switch is open and all others are closed. All currents leaving the bit switches sum together and flow into the minus reference; no current flows through the output amplifier and feedback loop.

Tables 3-1 through 3-3 compare switch settings with the corresponding amplifier output voltage levels for various digital numbers received from the computer. Output voltage levels for other numerical values in the allowed range can be derived by application of one of the following equations:

14-bit DAC

$$V_{out} \approx N\ (1.2\ mV)$$

12-bit DAC

$$V_{out} \approx N\ (4.88\ mV)$$

10-bit DAC

$$V_{out} \approx N\ (19.52\ mV)$$

where N is the decimal value of the number received from the computer.

For example, the decimal number -5250 would result in a voltage output from a 14-bit DAC of:

$$V_{out} \approx -5250\ (1.2\ mV) \approx -7.3\ V$$

Table 3-1. 14-Bit DAC Output Scale

ANALOG VALUE				COMPUTER OUTPUT AND SWITCH SETTINGS													
				EB 15 SW	EB 12 SW	EB 11 SW	EB 10 SW	EB 09 SW	EB 08 SW	EB 07 SW	EB 06 SW	EB 05 SW	EB 04 SW	EB 03 SW	EB 02 SW	EB 01 SW	EB 00 SW
RANGE	DECIMAL	OCTAL	Vout	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+Full Scale-1	+8191	017777	+9.999	0	1	1	1	1	1	1	1	1	1	1	1	1	1
				0	0	0	0	0	0	0	0	0	0	0	0	0	0
+Half Scale	+4096	010000	+5.000	0	1	0	0	0	0	0	0	0	0	0	0	0	0
				0	0	1	1	1	1	1	1	1	1	1	1	1	1
+1 LSB	+1	01	+0.0012	0	0	0	0	0	0	0	0	0	0	0	0	0	1
				0	1	1	1	1	1	1	1	1	1	1	1	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
				0	1	1	1	1	1	1	1	1	1	1	1	1	1
- LSB	- 1	17777.7	-0.0012	1	1	1	1	1	1	1	1	1	1	1	1	1	1
				1	0	0	0	0	0	0	0	0	0	0	0	0	0
-Half Scale	-4096	170000	-5.000	1	1	0	0	0	0	0	0	0	0	0	0	0	0
				1	0	1	1	1	1	1	1	1	1	1	1	1	1
-Full Scale+1	-8191	160001	-9.999	1	0	0	0	0	0	0	0	0	0	0	0	0	1
				1	1	1	1	1	1	1	1	1	1	1	1	1	0
-Full Scale	-8192	160000	-10.000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
				1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTE

The data contents of all the E bus lines are inverted once, except for the sign bit, which is inverted twice. This means a true level on an E bus data line (0 vdc) opens its switch, which tends to make the amplifier output more positive.

Table 3-2. 12-Bit DAC Output Scale

ANALOG VALUE				COMPUTER OUTPUT AND SWITCH SETTINGS											
				EB 15 SW 11	EB 10 SW 10	EB 09 SW 9	EB 08 SW 8	EB 07 SW 7	EB 06 SW 6	EB 05 SW 5	EB 04 SW 4	EB 03 SW 3	EB 02 SW 2	EB 01 SW 1	EB 00 SW 0
RANGE	DECIMAL	OCTAL	Vout												
+Full Scale -1	+2047	3777	+ 9.995	0	1	1	1	1	1	1	1	1	1	1	1
				0	0	0	0	0	0	0	0	0	0	0	0
-Half Scale	+1024	2000	+ 5.000	0	1	0	0	0	0	0	0	0	0	0	0
				1	1	1	1	1	1	1	1	1	1	1	1
+1 LSB	+ 1	1	+ 0.005	0	0	0	0	0	0	0	0	0	0	0	1
				0	1	1	1	1	1	1	1	1	1	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
				0	1	1	1	1	1	1	1	1	1	1	1
-1 LSB	- 1	177777	- 0.005	1	1	1	1	1	1	1	1	1	1	1	1
				1	0	0	0	0	0	0	0	0	0	0	0
-Half Scale	-1024	176000	- 5.000	1	1	0	0	0	0	0	0	0	0	0	0
				1	1	1	1	1	1	1	1	1	1	1	1
+Full Scale +1	-2047	174001	- 9.995	1	0	0	0	0	0	0	0	0	0	0	1
				1	1	1	1	1	1	1	1	1	1	1	0
-Full Scale	-2048	174000	-10.000	1	0	0	0	0	0	0	0	0	0	0	0
				1	1	1	1	1	1	1	1	1	1	1	1

Table 3-3. 10-Bit DAC Output Scale

ANALOG VALUE				COMPUTER OUTPUT AND SWITCH SETTINGS										
RANGE	DECIMAL	OCTAL	Vout	EB 12 SW 9	EB 08 SW 8	EB 07 SW 7	EB 06 SW 6	EB 05 SW 5	EB 04 SW 4	EB 03 SW 3	EB 02 SW 2	EB 01 SW 1	EB 00 SW 0
+Full Scale -1	+511	777	+ 9.980	0	1	1	1	1	1	1	1	1	1
				0	0	0	0	0	0	0	0	0	0
+Half Scale	+256	400	+ 5.000	0	1	0	0	0	0	0	0	0	0
				0	1	1	1	1	1	1	1	1	1
+1 LSB	+ 1	1	+ 0.020	0	0	0	0	0	0	0	0	0	1
				0	1	1	1	1	1	1	1	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0
				0	1	1	1	1	1	1	1	1	1
-1 LSB	- 1	177777	- 0.020	1	1	1	1	1	1	1	1	1	1
				1	0	0	0	0	0	0	0	0	0
-Half Scale	-256	177400	- 5.000	1	1	0	0	0	0	0	0	0	0
				1	1	1	1	1	1	1	1	1	1
-Full Scale +1	-511	177001	- 9.980	1	0	0	0	0	0	0	0	0	1
				1	1	1	1	1	1	1	1	1	0
-Full Scale	-512	177000	-10.000	1	0	0	0	0	0	0	0	0	0
				1	1	1	1	1	1	1	1	1	1

4. I/O INTERFACE THEORY OF OPERATION

The DAC Modules coordinate three types of communication between the computer and peripheral device: digital-to-analog data out, External Control signals out, and Sense signals in. The DAC logic responsible for providing these three interfaces is discussed in this section.

All communication between the DAC and the computer is conducted on the computer I/O bus. In the following discussion, mnemonics used to identify E-bus signals include the suffix "I". Signals transferred between the DAC and the BIC are carried on the B-bus; mnemonics for these signals include the suffix "B". Refer to Varian 620 and V73 system handbooks and Buffer Interlace Controller Manual for details regarding communication conducted via the computer I/O bus.

The following discussions are keyed by letter designations to schematics and logic diagrams presented in Appendix C.

4.1 PROGRAM-CONTROLLED DATA TRANSFER

A data transfer operation, resulting in a digital-to-analog conversion, occurs in two stages. First, the individual DAC is selected; then a data word is sent to the DAC buffer register inputs and strobed into the selected register.

DAC Selection Stage

The selection stage begins when the computer enters the desired device address and function code on E bus lines EB00-I through EB05-I and EB06-I through EB08-I. An NAND gate on the addressed master DAC decodes the device address and generates a Device Select signal. This is combined with the control line pulse FRYX-I (Function Ready). The resulting signal Function Select combines with a true level on EB15-I to clock the contents of the function code into the EXC2 storage register.

The EXC2 Decode Logic selects one of eight output lines, EXC2-0 through EXC2-7, according to the contents of the function code. Each EXC2 line is connected via a wire wrap jumper in the backplane to the clock input gate of a different DAC buffer register. An active EXC2 line enables one of three inputs to the clock input gate in preparation for the data transfer stage of the operation.

Data Transfer Stage

The device address is again placed on the E bus. A true level on EB14-I identifies the operation as a data transfer out and, together with Function-Select, sets the data transfer out (DTOS) latch. Output of the DTOS latch enables the second input to the clock input gate.

After the control pulse FRYX-I goes false, the computer removes the device address from the E bus and places a data word on lines EB00-I through EB14-I, with a sign bit on EB15-I. This is followed by the control pulse DRYX-I. DRYX-I enables the clock input gate of the selected DAC buffer register, clocking the data into the register. DRYX-I also resets the DTOS latch.

After DRYX-I goes false, the only true input to the clock input gate of the register is provided by the selected EXC2 line. This input remains true until a different EXC2 line at that device address is selected. Until that time, subsequent data transfer operations for that device address will be routed to the same DAC, without requiring another EXC2 instruction.

4.2 BIC-CONTROLLER DATA TRANSFER

When a data transfer is under BIC control, a different set of DAC logic is involved.

DAC Selection Stage

The DAC selection stage is the same for a BIC-controlled data transfer as for a program-controlled data transfer; the data transfer stage, however, is not.

Data Transfer Stage

The DAC module is selected by a special signal, EPO-N, which is made available through custom hardwire connections. One method for providing this signal is to jumper an EXC output to the EPO-N pin (P1-79) and execute an EXC instruction selecting that line. All eight EXC signals are made available to the backplane by the DAC for this reason.

The EPO-N pulse is combined with the BIC-generated signal DCEX-B. Together they set the DAC's Connected latch. When the BIC receives the output of the Connected latch, CDCX-B, indicating that the DAC has been connected, it resets DCEX-B. The Connected latch remains set, however, until the end of the data transfer.

Output from the Connected latch is also returned to the BIC as TROX-B and TRQX-B. TROX-B identifies the direction of the data transfer (from the computer to the DAC) and TRQX-B is a request for data.

TRQX-B will be true while the Connected latch is set if the signal Device Ready is true. Device Ready is a pulse that indicates that the DAC has had sufficient time to convert the last data word or that the external device can accept a new voltage signal from the DAC.

Since Device Ready determines the rate at which data words are supplied to the DAC, the maximum frequency with which that signal occurs must be determined by the speed of the DAC or the external device. Settling times for DACs of different resolutions are given in the table of specifications. Device Ready may be provided in a number of ways, using external hardware. The choice of method will depend on the specific application. Suggested implementation is the application of the pulse output from the programmable timer contained on the ADC module or the use of a standard laboratory pulse generator.

With Device Ready true and Transfer Enable false (data word has not yet been placed on the E-bus), TRQX-B is true. When the BIC receives TRQX-B, it causes the computer

to place the data on the E-bus and responds to the DAC with TAKX-B. TAKX-B produces Transfer Enable, which resets TRQX-B and enables the second input to the clock input gate of the selected DAC. Transfer Enable is the BIC equivalent to DTOS.

After the computer places the data word on the E-bus, it generates DRYX-I. This control pulse enables the clock input gate of the DAC buffer register, clocking the data into the register. When Deivce Ready goes true again, TRQX-B will go true and another data word will be transferred. This sequence is repeated until the last word in the block has been transferred. At that time, DESX-B from the BIC resets the connected latch, disconnecting the DAC.

4.3 EXTERNAL CONTROL DECODE

Each master DAC module makes available eight EXC outputs. An output goes true (ground) when its flip-flop is set by the EXC decode logic. A function code, provided by the computer as a result of an EXC program instruction, specifies which EXC output flip-flop is set.

EXC output flip-flops are not reset by program instructions alone; they may be reset through a variety of hardware or hardware/software techniques. Some examples of methods for resetting EXC output flip-flops are discussed in Section 2.6.

The EXC output driver is capable of providing signals at levels up to +30 volts, with current sinking of up to 300 mA (see Appendix B).

4.4 SENSE DECODE

Every master DAC is capable of sampling, one at a time, up to eight Sense input lines and forwarding the logic level present on the selected line to the computer. A function code, provided by the computer as a result of a SEN program instruction, specifies which sense input is to be sampled.

Sense input signals are considered logically true when they are at 0 Vdc and logically false at +4 Vdc. When sampled, a logically true input will cause a jump condition in the program. The DAC provides a 5.6 K pullup resistor to +5 volts on each Sense input. It is, therefore, not necessary to drive the Sense inputs high. The Sense inputs are normally connected to external logic (0 to +5 volts) or switch closures to ground.

Note: Sensed signals should not be allowed to go negative with respect to DAC logic ground and should not be allowed to go more positive than the DAC +5 volts.

5. INSTALLATION

5.1 PREREQUISITES

Each DAC or DACE requires one card slot in either the mainframe or Memory Expansion/ Peripheral Controller frame. No special slots are reserved for use by DACs; their location in the frame is determined solely by considerations of convenience in backplane wiring.

An Analog Power Supply Module (Part No. 620-88) must be installed when using one or more DAC or DACE moudles. If a Power Supply Module has been previously installed and sufficient current is available to support the DAC modules, an additional power supply need not be installed.

5.2 INSTALLATION AND INTERCONNECTION

A DAC or DACE is installed vertically, with its component side to the installer's left in 620/i and 620/L computers, and horizontally in the 620/f computer. Figure 5-1 illustrates a typical installation.

CAUTION

Do not install DAC modules in slots that have been previously wired to provide power to other modules; if the intended slot is already wired, remove any connections to power before installing the DAC module to protect its components. Refer to Table 5-1 for proper power connection.

The card is installed with the double pin edge pointing toward the installer. Proper orientation of the module is important since the cards are not keyed.

Connection to the computer I/O-bus and the BIC option B-bus is provided through backplane wiring. All pin assignments for the I/O-bus and B-bus are listed in Appendix A.

For each DAC, connections to external instruments include one or two DAC outputs and may include up to eight External Control outputs and up to eight Sense inputs. Connections between DAC and DACE modules may also be required (for example, EXC2 and DAC Enable outputs from a master DAC to digital-to-analog converters located on slave DACEs). Pin assignments for these connections are also listed in Appendix A. Recommended connector types for J1 and J2 are identified in the summary of key specifications in Appendix B.

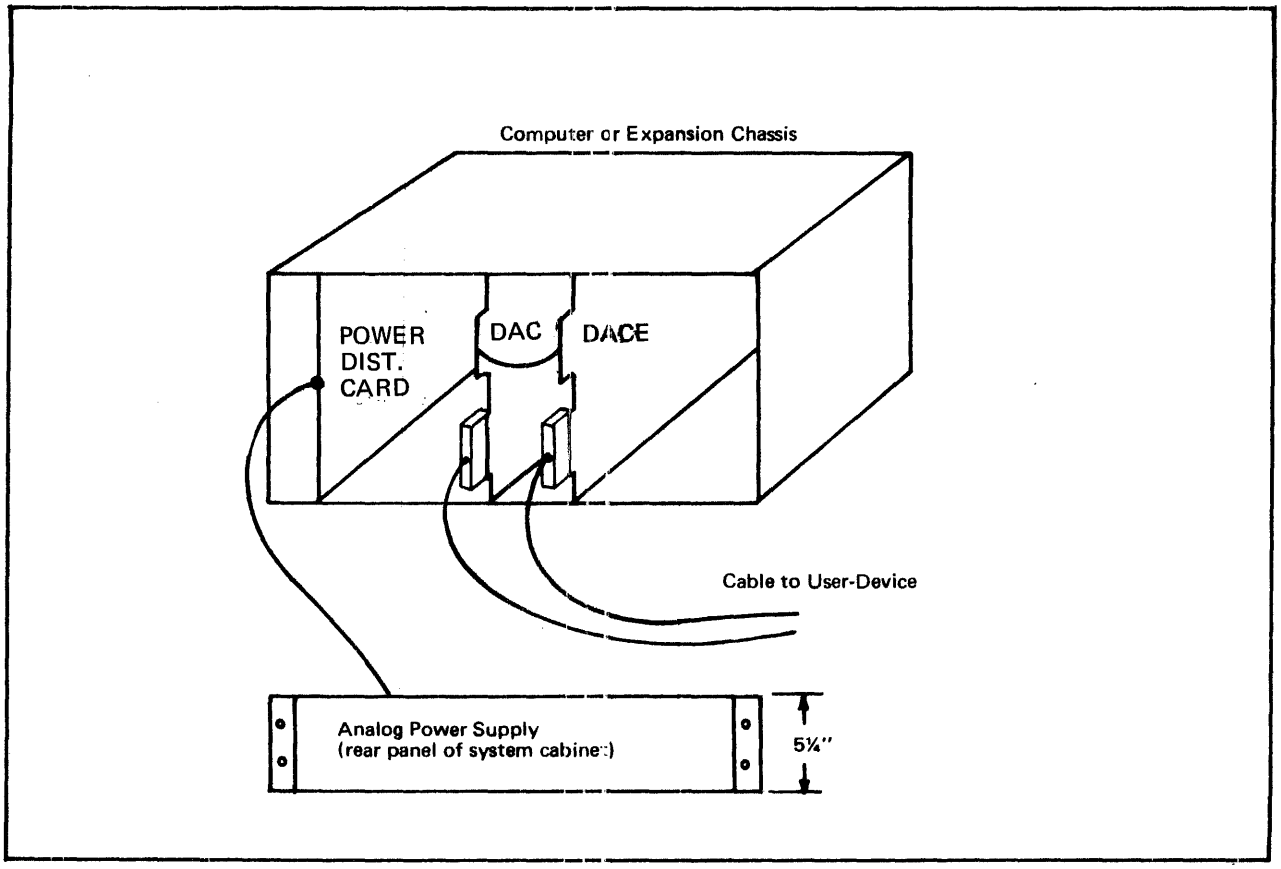


Figure 5-1. Typical Module Installation

Power Supply Wiring

Connections to the DAC must be made for three power supply voltages and senses, an analog ground, digital ground, and digital ground sense. Table 5-1 lists the pin assignments on the DAC wirewrap backplane for these connections. When the DAC is used with other modules (ADCMs, DACEs, MUXs, etc.), similar voltages should be tied together, and the voltage sense line should be brought from the mid-point of the voltage tie-line to a voltage sense line on the power supply wirewrap backplane.

The voltages and sense points for the power supply backplane are given in the Power Supply Manual (Publication No. 03-996-812).

Table 5-1. DAC Wirewrap Backplane Pin Connections for Power Supply

Power Supply Voltage	DAC Pins
Digital Ground	P1-1, 48, 100, 122
+5 Vdc	P1-118, 121
+15 Vdc	P1-111
-15 Vdc	P1-113
Analog Ground	P1-115

Device Address Wiring

Table 5-2 lists the jumper connections required to wire a device address for a master DAC. Note that P1-76 (Enable) is not normally used. It is available, however, and may be used as an additional addressing condition. For example, if multiple master DAC modules have the same device address, the Enable input can be used to permit only one module to respond to that address at a given time.

Table 5-2. Device Address Wiring

Address	Wirewrap Jumpers		
050	P1-72 to P1-71	P1-69 to P1-68	P1-66 to P1-65
051	P1-72 to P1-71	P1-69 to P1-68	P1-66 to P1-64
052	P1-72 to P1-71	P1-69 to P1-67	P1-66 to P1-65
053	P1-72 to P1-71	P1-69 to P1-67	P1-66 to P1-64
054	P1-72 to P1-70	P1-69 to P1-68	P1-66 to P1-65
055	P1-72 to P1-70	P1-69 to P1-68	P1-66 to P1-64
056	P1-72 to P1-70	P1-69 to P1-67	P1-66 to P1-65
057	P1-72 to P1-70	P1-69 to P1-67	P1-66 to P1-64

EXC2 Output Wiring (DAC Select)

Table 5-3 lists the jumper connections required to wire the eight EXC2 outputs to select individual converters on the DAC and DACEs.

Table 5-3. DAC Select Connections

EXC2 Output	Master (DAC 1) Pin		Pin		DAC Card
0	P1-110	to	P1-77	of	1
1	P1-112	to	P1-78	of	1
2	P1-114	to	P1-77	of	2
3	P1-103	to	P1-78	of	2
4	P1-104	to	P1-77	of	3
5	P1-105	to	P1-78	of	3
6	P1-106	to	P1-77	of	4
7	P1-107	to	P1-78	of	4

External Control Reset Wiring

Provision must be made for resetting External Control outputs. Basic information on techniques for resetting the outputs is presented in Section 2.6. One possible configuration is illustrated in Table 5-4; this configuration converts the eight EXC flags to four RS flip-flops with both set and reset driven by the program.

Table 5-4. External Control Reset Wiring

Signals	Master DAC	Master DAC
EXC1/REX0	J1-6	J1-5
EXC3/REX2	J1-12	J1-11
EXC5/REX4	J1-18	J1-17
EXC7/REX6	J1-24	J1-23

Device Ready and EPO-N Wiring

DACs used in conjunction with the BIC option require that two special signals be provided to the master DAC. One, called Device Ready, synchronizes data transfer with the DAC or external device operation; it is applied to P1-73 of the master DAC. The other, called EPO-N, selects the DAC for connection to the BIC; it is applied to P1-79 of the master DAC. If a BIC is not used P1-79 should be grounded. Further discussion of this wiring can be found in Section 4.2 of this manual.

5.3 INSTALLATION EXAMPLE

A typical single DAC module could be installed with the following wiring:

Device Address 050

P1-71 wired to P1-72
P1-68 wired to P1-69
P1-65 wired to P1-66

DAC Select Connections

P1-110 wired to P1-77
P1-112 wired to P1-78

BIC Control

P1-79 wired to P1-101
P1-73 wired to P1-87

Note: If a BIC is not used, P1-79 should be grounded.

Note that appropriate EXC Reset wiring would also be configured. See Sections 2.6 and 5.2 for further details. In addition, analog power supply wiring would be required, as described in Section 5.2.

APPENDIX A: DAC PIN ASSIGNMENTS

BACKPLANE WIRING

PIN NO.	NAME	FUNCTION
P1-1	Digital ground	
-2	EB00	One bit of Device Address or data word
-3	Digital ground	
-4	EB01	One bit of Device Address or data word
-5	Digital ground	
-6	EB02	One bit of Device Address or data word
-7	Digital ground	
-8	EB03	One bit of Device Address or data word
-9	Digital ground	
-10	EB04	One bit of Device Address or data word
-11	EB05	One bit of Device Address or data word
-12	EB06	One bit of EXC, EXC2 or SEN code or data word
-13	EB07	One bit of EXC, EXC2 or SEN code or data word
-14	EB08	One bit of EXC, EXC2 or SEN code or data word
-15	EB09	One bit of data word
-16	EB10	One bit of data word
-17	EB11	EXC tag line or one bit of data word
-18	EB12	Sense tag line or one bit of data word
-19	EB13	One bit of data word
-20	EB14	Data tag line or one bit of data word
-21	EB15	EXC2 tag line or one bit of data word
-22	Digital ground	
-23	Not used	
-24	Digital ground	
-25	Not used	
-26	Digital ground	
-27	FRYX	Device Address tag line
-28	Digital line	
-29	DRYX	Gates data into buffer register
-30	Digital ground	
-31	SERX	Sense input to computer
-32	Digital ground	
-33	Not used	

PIN NO.	NAME	FUNCTION
P1-34	Digital ground	
-35	Not used	
-36	Digital ground	
-37	Not Used	
-38	Digital ground	
-39	Not used	
-40	Digital ground	
-41	Not used	
-42	Not used	
-43	SYRT	Resets system logic
-44	IUAX	Interrupt acknowledge from computer
-45	Not used	
-46	Not used	
-47	Not used	
-48	Digital ground	
-49	TRQZ	Transfer Request from AOM to BIC
-50	TROX	Identifies direction of BIC-controlled data transfer
-51	Digital ground	
-52	Not used	
-53	Digital ground	
-54	CDCX	Notifies BIC that AOM is connected
-55	Digital ground	
-56	DCEX	Connect signal from BIC
-57	Digital ground	
-58	TAKX	Transfer Request acknowledge from BIC
-59	Digital ground	
-60	DESX	Disconnect from BIC
-61	Not used	
-62	Not used	
-63	Not used	
-64	EB00+	Jumper connection for wiring Device Address
-65	EB00-	Jumper connection for wiring Device Address
-66	EB0I	Jumper connection for wiring Device Address
-67	EB01+	Jumper connection for wiring Device Address
-68	EB01-	Jumper connection for wiring Device Address
-69	EBlI	Jumper connection for wiring Device Address

PIN NO.	NAME	FUNCTION
P1-70	EB02+	Jumper connection for wiring Device Address
-71	EB02-	Jumper connection for wiring Device Address
-72	EB2I	Jumper connection for wiring Device Address
-73	Device Ready	Externally supplied timing for BIC-connected operations
-74	Not used	
-75	Not used	
-76	Enable	Not used
-77	EXC2-N	Jumper connection for EXC2 signal assigned to DAC 1
-78	EXC2-M	Jumper connection for EXC2 signal assigned to DAC 2
-79	EPO-N	DAC Select signal for BIC-connected operations
-80	Not used	
-81	Not used	
-82	Not used	
-83	Not used	
-84	Not used	
-85	DTOS	Data transfer request to computer
-86	EXC7	Jumper connection for internal use of EXC7
-87	EXC5	Jumper connection for internal use of EXC5
-88	Not used	
-89	Not used	
-90	EXC6	Jumper connection for internal use of EXC6
-91	EXC2	Jumper connection for internal use of EXC2
-92	Not used	
-93	EXC3	Jumper connection for internal use of EXC3
-94	EXC4	Jumper connection for internal use of EXC4
-95	Not used	
-96	Not used	
-97	Not used	
-98	EXC1	Jumper connection for internal use of EXC1

PIN NO.	NAME	FUNCTION
P1-99	Not used	
-100	Digital ground	
-101	EXC0	Jumper connection for internal use of EXC0
-102	Enable	Jumper connection for Enable signal to slave DACs
-103	EXC2-3	Jumper connection for DAC Select line 3
-104	EXC2-4	Jumper connection for DAC Select line 4
-105	EXC2-5	Jumper connection for DAC Select line 5
-106	EXC2-6	Jumper connection for DAC Select line 6
-107	Not used	
-108	EXC2-7	Jumper connection for DAC Select line 7
-109	Not used	
-110	EXC2-0	Jumper connection for DAC Select line 0
-111		Jumper connection for +15 Vdc source
-112	EXC2-1	Jumper connection for DAC Select line 1
-113		Jumper connection for -15 Vdc source
-114	EXC2-2	Jumper connection for DAC Select line 2
-115		Jumper connection for -15 Vdc ground
-116	Not used	
-117	Not used	
-118	+5 Vdc	+5 Vdc
-119	Not used	
-120	Not used	
-121	+5 Vdc	+5 Vdc
-122	Digital ground	

TERMINAL EDGE CONNECTOR WIRING

PIN NO.	NAME	FUNCTION
J1-1	Not used	
-2		Jumper connection to +5 Vdc supply
-3	REX5	Jumper connection for EXC5 reset
-4	Not used	
-5	REX4	Jumper connection for EXC4 reset
-6	Not used	
-7	REX1	Jumper connection for EXC1 reset
-8	Not used	
-9	REX0	Jumper connection for EXC0 reset
-10	Not used	
-11	REX7	Jumper connection for EXC7 reset

PIN NO.	NAME	FUNCTION
J1-12	Not used	
-13	REX6	Jumper connection for EXC6 reset
-14	EXC-7	Output connection for EXC7
-15	REX2	Jumper connection for EXC2 reset
-16	EXC6	Output connection for EXC6
-17	REX3	Jumper connection for EXC3 reset
-18	EXC5	Output connection for EXC5
-19		Jumper connection for DAC1 buffer clock
-20	EXC4	Output connection for EXC4
-21		Jumper connection for DAC2 buffer clock
-22	EXC3	Output connection for EXC3
-23	Device Ready	Externally supplied timing for BIC-connected operations
-24	EXC2	Output connection for EXC2
-25	Not used	
-26	EXC1	Output connection for EXC1
-27	Not used	
-28	EXC0	Output connection for EXC0
-29	Sense 7	Input connection for Sense 7 line
-30		Jumper connection to digital ground
-31	Sense 6	Input connection for Sense 6 line
-32		Jumper connection to digital ground
-33	Sense 5	Input connection for Sense 5 line
-34		Jumper connection to digital ground
-35	Sense 4	Input connection for Sense 4 line
-36		Jumper connection to digital ground
-37	Sense 3	Input connection for Sense 3 line
-38		Jumper connection to digital ground
-39	Sense 2	Input connection for Sense 2 line
-40		Jumper connection to digital ground
-41	Sense 1	Input connection for Sense 1 line
-42		Jumper connection to digital ground
-43	Sense 0	Input connection for Sense 0 line
-44		Jumper connection to digital ground
J2-1		DAC1 analog output signal
-43		DAC2 analog output signal

APPENDIX B: SPECIFICATIONS

Accuracy

± 0.003% of 20 V full scale (14-bit option)

± 0.012% of 20 V full scale (12-bit option)

± 0.05% of 20 V full scale (10-bit option)

Temperature Coefficient

±0.1 LSB/°C (0 °C to 50 °C)

Warm Up Time

Essentially 0; however allow 15 minutes for best results.

Slew Rate

4 volts/microsecond

Settling Time

20 microseconds to stated accuracy

Adjustments

Full scale and zero (10-bit option)

Full scale, zero, and MSB (12-bit option)

Full scale, zero, and 3 MSB (14-bit option)

Output Voltage Range

± 10 V full scale

Output Current Range

10 ma

(40 ma option available)

Switching Transient

200 mV peak, maximum duration less than 5 microseconds.

Capacitive Load

200 pF at specified settling time.

Short Circuit Protection

DAC outputs may be shorted to ground indefinitely without damage.

Output Noise

Less than $\pm$ 1/2 LSB maximum due to activity on computer E-bus or other DACs.

Digital Control Outputs

Number: Eight.

Type: Open Collector Transistor. TI SN75451P Dual Peripheral Driver sinks current when true. Each output will sink 300 mA when and standoff +30 volts. Outputs are controlled by flip-flops which are set by computer instructions and are reset externally. (See manufacturer's specifications for further details.)

Digital Sense Inputs

Number: Eight

Type: TTL logic levels. Ground true, open circuit inputs are held to +5 volt supply through 5.6 K ohm resistors.

Power

+15 Vdc ±0.1%, 90 mA

-15 Vdc ±3%, 90 mA

+5 Vdc ±1%, 850 mA

Temperature Range

Specification: 0°C to 50°C

Operating: -10°C to 70°C

Storage: -55°C to 85°C

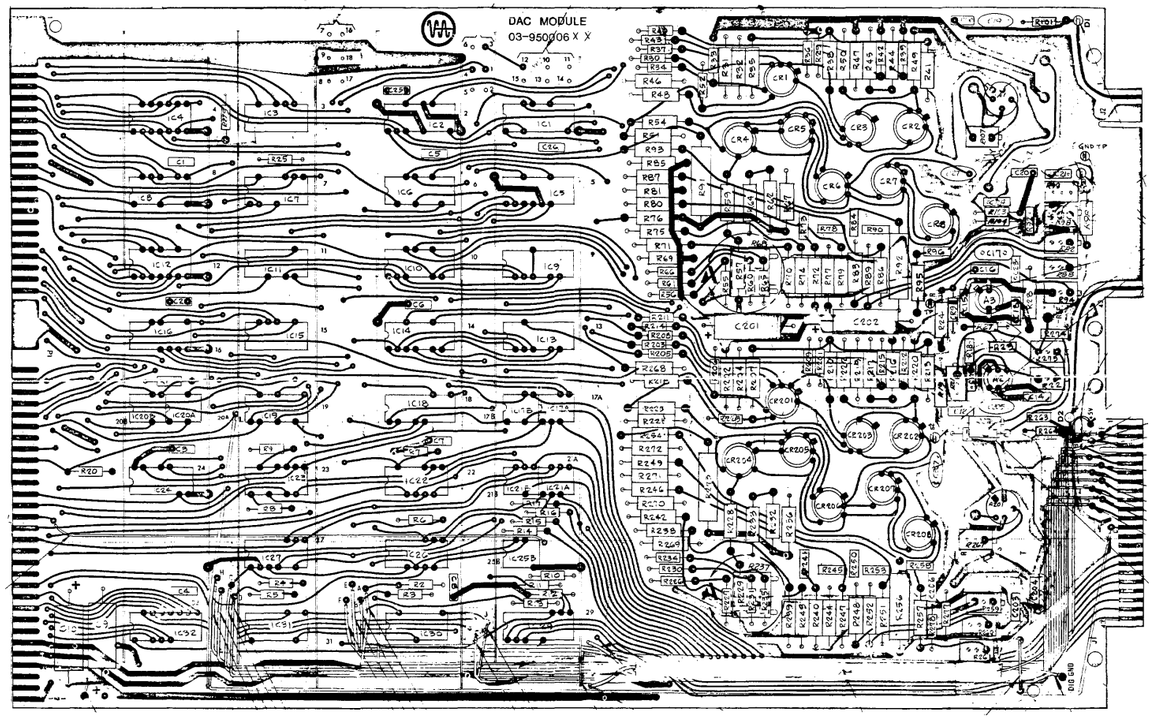
Physical Characteristics

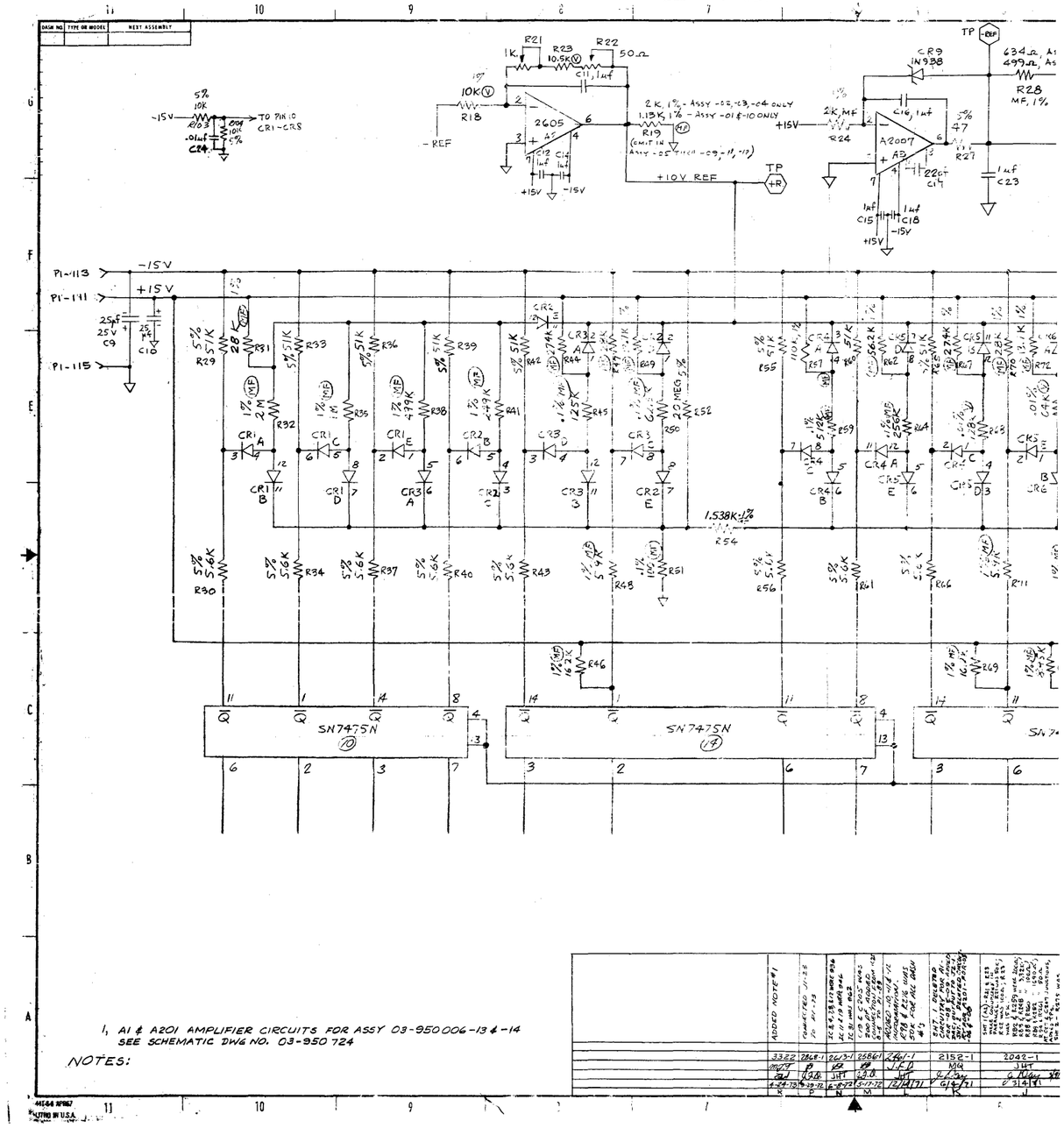
Dimensions: One printed circuit board 7-3/4 x 12 x 1/2 inches.

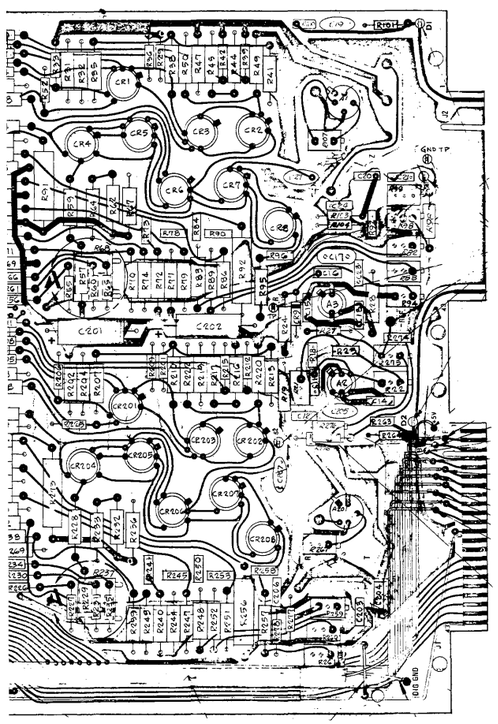
Connectors: One 122-terminal card edge connector. Two 44-terminal card edge connectors.

APPENDIX C:
SCHEMATIC, ASSEMBLIES, AND PARTS LIST

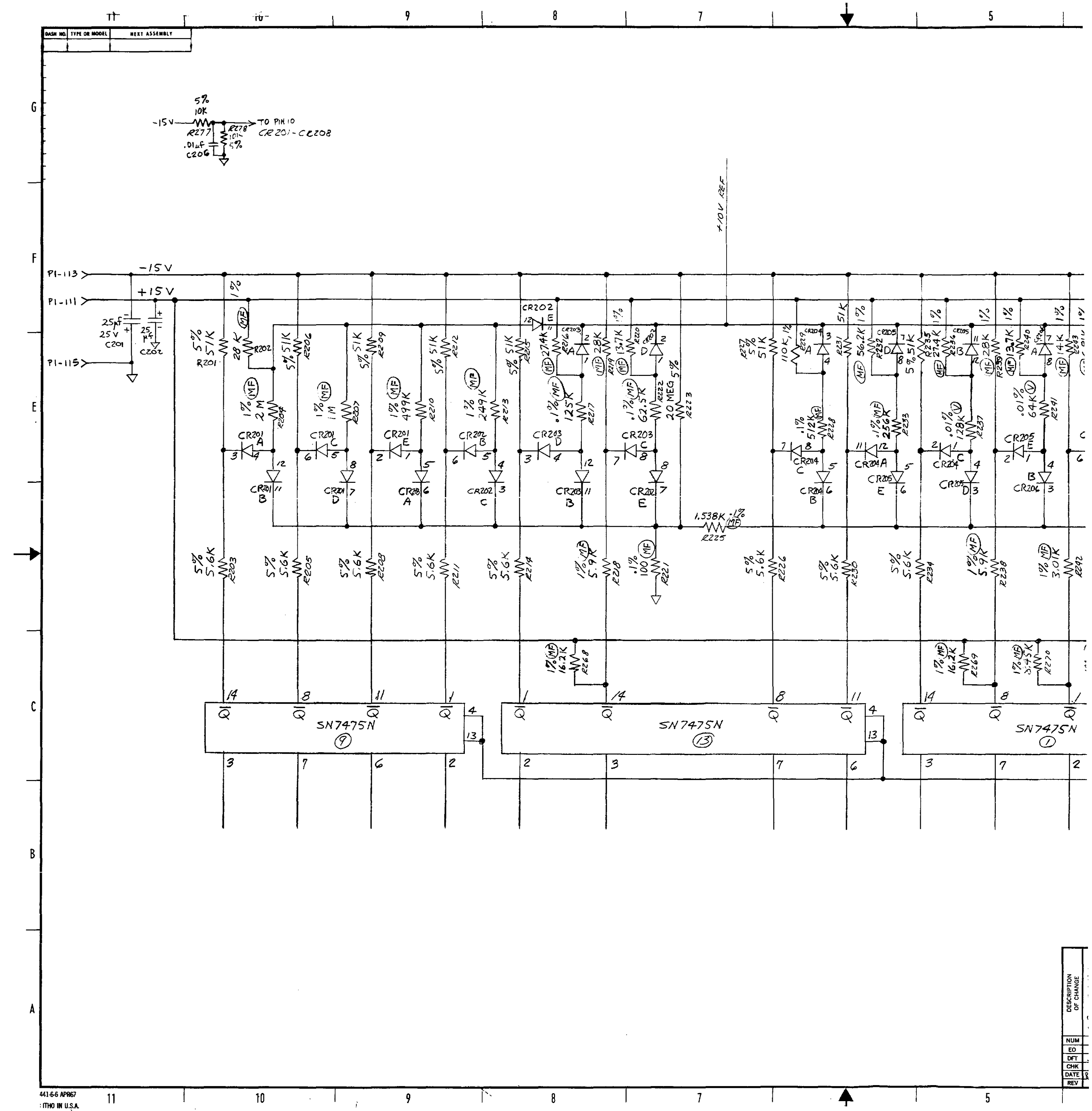
DAC Module 03-950004


DAC MODULE
03-950006 X X


R21
1K
R22
50Ω
R23
10.5K
C11, 1uf
10K
R18
-REF
2605
2K, 1% - ASSY -02,-03,-04 ONLY
1.13K, 1% - ASSY -01 & -10 ONLY
R19
+15V
-15V
+10V REF
TP
+R
5%
10K
-15V
TO PIN 10
CR1-CR5
.01uf
C24
2K, MF
R24
A2007
CR9
IN938
634Ω, A
499Ω, A
R28
MF, 1%
C16, 1uf
47
R27
22pf
C17
1uf
C23
1uf
C15
1uf
C18
P1-113
P1-111
P1-115
-15V
+15V
25uf
25V
C9
C10
5% 51K
R29
R31
R33
R36
R39
R42
5% 5.6K
R30
R34
R37
R40
R43
1% 2M
R32
1% 1M
R35
1% 499K
R38
1% 249K
R41
1.538K 1%
R54
20 MEG 5%
R52
562K
R55
274K
R56
28.7K
R57
R58
R59
R60
R61
R66
R69
R72
R44
R45
R46
R48
R51
R64
R67
R70
R73
R47
R49
R50
R53
R62
R65
R68
R71
R74
SN7475N
(10)
SN7475N
(14)
1, A1 & A201 AMPLIFIER CIRCUITS FOR ASSY 03-950006-13 & -14
SEE SCHEMATIC DWG NO. 03-950724
NOTES:



R21 1K
R23 10.5K
R22 50Ω
C11, 1mf
10K
R18
2605
2K (1%) - ASSY -02,-03,-04 ONLY
1.13K, 1% - ASSY -01 & -10 ONLY
R19
(OMIT IN ASSY -05 THRU -09, -11, -12)
-REF
+10V REF
TP +R
-15V
+15V
5% 10K
TO PIN 10 CR1-CR5
.01mf C24
CR9 IN938
634Ω, ASSY -05,-06,-07,-08,-09,-11,-12 ONLY
499Ω, ASSY -01,-02,-03,-04,-10 ONLY
R28 MF, 1%
-10V REF
2K, MF R24
A2007 A3
47 R27
C16, 1mf
C23 1mf
C14 22mf
C15 1mf
C18 1mf
P1-113
P1-111
P1-115
C9 25mf 25V
C10 .25mf
R29 5K
R31 28
R32 2M
R33 51K
R34 5.6K
R35 1K
R36 51K
R37 5.6K
R38 479K
R39 51K
R40 5.6K
R41 479K
R42 51K
R43 5.6K
R44 125K
R45 51K
R46 16.2K
R48 5.49K
R49 20 MEG
R51 100 (MF)
R52 5K
R54 1.538K 1%
R55 5.49K
R56 5.6K
R57 562K
R58 5.6K
R59 2.55K
R60 5.6K
R61 5.6K
R62 2.55K
R63 27.4K
R64 5.6K
R66 5.6K
R67 2.55K
R68 27.4K
R69 16.2K
R70 11K
R71 5.6K
R72 64K
R73 5.6K
R74 31K
R75 5.6K
R76 42.2K
R77 5.6K
R78 16.9K
R79 5.6K
R80 49.9K
R81 42.2K
R82 2K
R83 620
R84 16.9K
R85 5.6K
R86 178
R87 750
R88 200
R91 16.2K
R92 100
R93 383
R94 100
R97 4.1K-ASSY -01,-02,-03,-04,-10 ONLY
21.5K-ASSY -05,-06,-07,-11 ONLY
OMIT 1W ASSY -08,-09 & -12
R98 523K-1%-MF-ASSY-08,-09,-12
1K-ASSY-01,-02,-03,-04,-05,-06,-07,-10,-11
R99, 50K-ASSY-01,-02,-03,-04,-05,-06,-07,-10,-11
10K-ASSY-08,-09,-12
SEE NOTE #1 FOR ASSY -13 & -14
64K-ASSY -03,-09,-12 ONLY
16K-ASSY -05,-06,-07,-11 ONLY
4K-ASSY -01,-02,-03,-04,-10 ONLY
R100 .01%
C19 11 OPF
R101 82
2605 A1
C20 1mf
C21 1mf
J2-1
J2+3+4+1 2-44
J2R17 10K
-15V +15V
110PF C27
TP SM
TP D1
CR1 A B D
CR2 B 3 E
CR3 A 3 C
CR4 A B E
CR5 A E D
CR6 A D E
CR7 A C E
CR8 A B D
SN7475N (10)
SN7475N (14)
SN7475N (2)
SN7475N (6)
SN7440N
1, A1 & A201 AMPLIFIER CIRCUITS FOR ASSY 03-950006-13 & -14 SEE SCHEMATIC DWG NO. 03-950 724
NOTES:
DO NOT SCALE DRAWING
D 03-950004 R
SHT 1 OF 3


DASH NO. TYPE OR MODEL NEXT ASSEMBLY
-15V 5% 10K R277 R278 10K 5% .01µf C206 TO PIN 10 CR201 - CR208
+10V REF
P1-113 -15V
P1-111 +15V
P1-115
25µf 25V C201
25µf C202
5% 51K R201
28K R202 1%
1% 2M R204
1% 1M R207
1% 499K R210
1% 249K R213
.1% 125K R217
.1% 62.5K R222
20 MEG 5% R223
5% 51K R206
5% 51K R209
5% 51K R212
5% 51K R215
27.4K R216
28K R219
13.7K R220
51K R227
110K 1% R229
51K R231
56.2K R232
.1% 512K R228
.1% 256K R233
5% 51K R235
27.4K R236
.01% 128K R237
28K R239
13.7K R240
.01% 64K R241
14K R243
CR201 CR202 CR203 CR204 CR205 CR206
1.538K .1% R225
5% 5.6K R203
5% 5.6K R205
5% 5.6K R208
5% 5.6K R211
5% 5.6K R214
1% 5.9K R218
.1% 100 R221
5% 5.6K R226
5% 5.6K R230
5% 5.6K R234
1% 5.9K R238
1% 3.01K R242
1% 16.2K R268
1% 16.2K R269
1% 3.45K R270
SN7475N (9)
SN7475N (13)
SN7475N (1)
DESCRIPTION OF CHANGE
NUM EO DFT CHK DATE REV
441-6-6 APR67
LITHO IN U.S.A.

D 03-950004

DASH NO.	TYPE OR MODEL	NEXT ASSEMBLY

REQ	PART NUMBER	DESCRIPTION OR MATERIAL	ITEM

-15V
+15V
P1-113
P1-111
P1-115
C201 25μF 25V
C202 25μF 25V
-15V 5% 10K R277 .01μF C206 TO PIN 10 CR201-CR208 R278 10K 5%
+10V REF
-10V REF
R201 28K 1%
R202 2M 1%
R203 1M 1%
R204 499K 1%
R205 249K 1%
R206 124K 1%
R207 62.5K 1%
R208 20 MEG 5%
R209 51K 5%
R210 51K 5%
R211 51K 5%
R212 51K 5%
R213 51K 5%
R214 51K 5%
R215 110K 1%
R216 51K 1%
R217 56.2K 1%
R218 51K 1%
R219 51K 1%
R220 51K 1%
R221 51K 1%
R222 51K 1%
R223 51K 1%
R224 51K 1%
R225 1.538K 1%
R226 5.6K 5%
R227 5.6K 5%
R228 5.6K 5%
R229 5.6K 5%
R230 5.6K 5%
R231 5.6K 5%
R232 5.6K 5%
R233 5.6K 5%
R234 5.6K 5%
R235 5.6K 5%
R236 5.6K 5%
R237 5.6K 5%
R238 5.6K 5%
R239 5.6K 5%
R240 5.6K 5%
R241 5.6K 5%
R242 5.6K 5%
R243 5.6K 5%
R244 5.6K 5%
R245 5.6K 5%
R246 5.6K 5%
R247 5.6K 5%
R248 5.6K 5%
R249 5.6K 5%
R250 5.6K 5%
R251 5.6K 5%
R252 5.6K 5%
R253 5.6K 5%
R254 5.6K 5%
R255 5.6K 5%
R256 5.6K 5%
R257 5.6K 5%
R258 5.6K 5%
R259 2K 1%
R260 200 1%
R261 100 1W
R274 1.1K-ASSY-01,-10 ONLY; 21.5K-ASSY-02,-05,-11 ONLY; (OMIT IN ASSY-03,-06,-08 & -12)
R275 1K-ASSY-01,-02,-05,-10,-11; 10K-ASSY-03,-06,-08,-12
R276, 50K-ASSY-01,-02,-05,-10,-11; 52.3K,1/4W,MF-ASSY-03,-06,-08,-12
SEE NOTE #1 FOR ASSY -13 & -14: 64K-ASSY-03,-06,-08 ASSY; 16K-ASSY-02,-05 ONLY; 4K-ASSY-01 ONLY
R263, .01%
C205 110pF
C207 110pF
R264 82 5%
R267 50K
1μF 1W
TP 52
TP 02
DAC2 OUTPUT J2-43
J2-3-44 2-44
-15V +15V
CR201 A B C D E
CR202 A B C D E
CR203 A B C D E
CR204 A B C D E
CR205 A B C D E
CR206 A B C D E
CR207 A B C D E
CR208 A B C D E
SN7475N (9)
SN7475N (13)
SN7475N (1)
SN7475N (6)
SN7440N (30)

DO NOT SCALE DRAWING

DESCRIPTION OF CHANGE							
	CIRCUIT CHANGES ADDED REF DES.	ADDED .02 DEACTIVATION	ADDED CR206 REDR WAS 499K Ω REDR = 250K Ω	REDR WAS 56.2K Ω CHANGED TO 51K Ω (ALSO CHANGED R232 & R233 VALUES) ADDED R234 & R235 CHANGED R231 & R232 VALUES	CHANGES PER SHT 1.	REDR FROM 249K TO 124K; CHANGED R216 VALUE FROM 5.9K TO 2.49K; R218 FROM 5.9K TO 3.01K; R219 FROM 5.9K TO 1.47K; R220 FROM 5.9K TO 750Ω; R221 FROM 100Ω TO 383Ω; ADDED R222 & R223	SEE SHT 10F3
NUM							
EO							
DFT	JHT	JED	JHT	JHT	JHT	JHT	
CHK							
DATE	7/6/70	8/17/70	10/1/70	10/27/70	11/2/70	11/6/70	
REV							

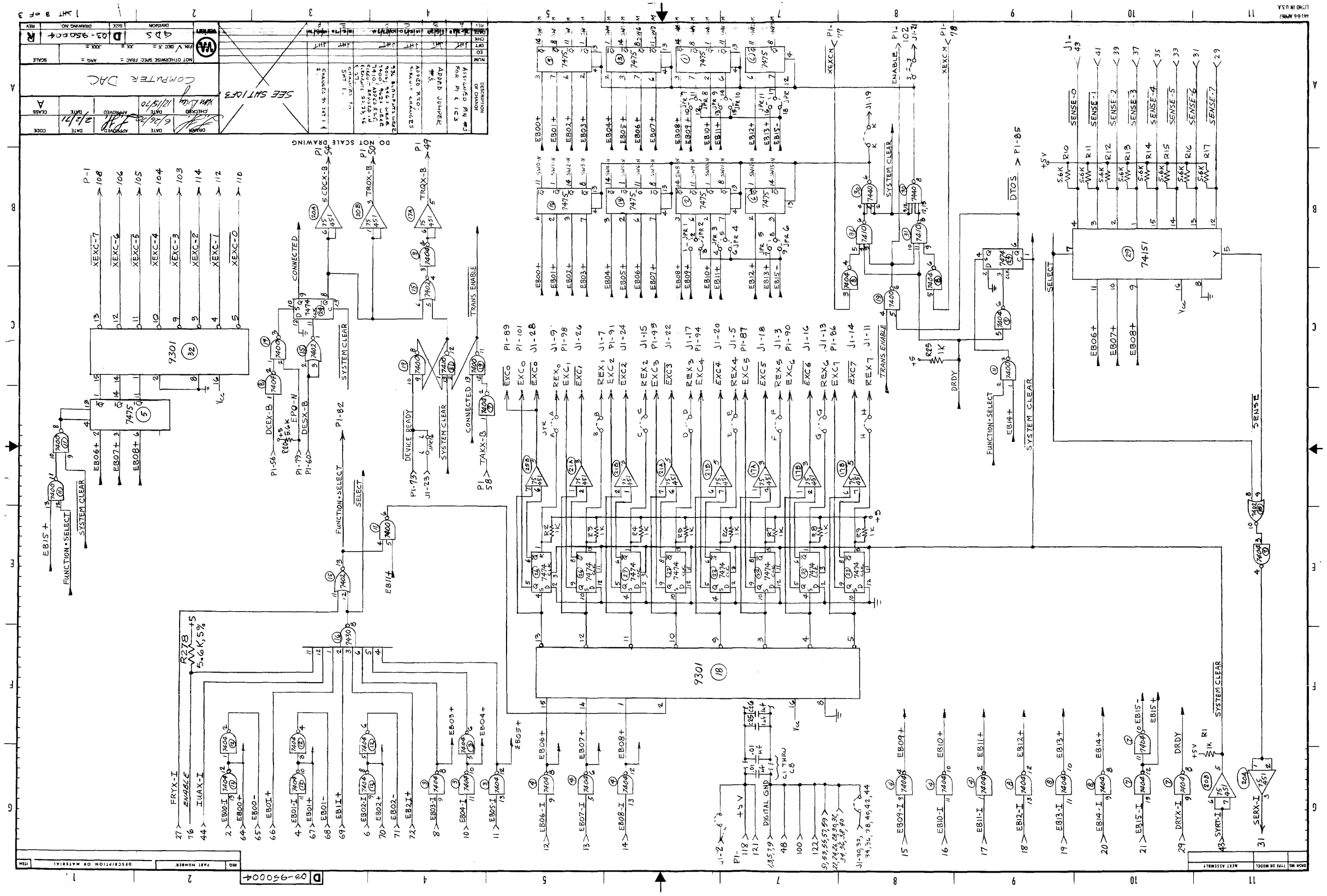
DRAWN	DATE	APPROVED	DATE	CODE
	6/17/70		2/2/71	
CHECKED	DATE	APPROVED	DATE	CLASS
	11/5/70			A

DAC2

NOT OTHERWISE SPEC: FRAC ± ; ANG ± ; SCALE ~
FIN. √ DEC X ± ; XX ± ; XXX ±

varian | GDS | D | 03-950004 | REV

SHT 2 of 3


COMPUTER DAC
SEE SHEET 103
DO NOT SCALE DRAWING
9301
74151
74175
74174
74107
74H00
74H03
74H04
74H10
74H20
74H74
74H40
SYSTEM CLEAR
TRANS ENABLE
DEVICE READY
CONNECTED
FUNCTION-SELECT
SELECT
DRDY
DTOS
SENSE
XEXC-0
XEXC-1
XEXC-2
XEXC-3
XEXC-4
XEXC-5
XEXC-6
XEXC-7
SENSE-0
SENSE-1
SENSE-2
SENSE-3
SENSE-4
SENSE-5
SENSE-6
SENSE-7
+5V
09-95004

DAC MODULE ASSEMBLY, 03-950006

Schematic Reference	Description	Varian Part No.
IC1,2,5,6,9,10, 13,14	IC Element 7475N	62-600351
IC3,4,7,8,12	IC Element 7404N	62-600013
IC11,19	IC Element 7400	62-600355
IC15	IC Element 7402N	62-600356
IC16	IC Element 7430N	62-600359
IC17A,17N,20A, 21A,21B,25B	IC Element 75451P	62-600260
IC18,32	IC Element 9301	62-600400
IC22,23,24,26,27	IC Element 7474N	62-600365
IC29	IC Element 74151N	62-600270
IC 30	IC Element 7440N	62-600310
IC31	IC Element 7410	62-600357
A1,A201,A2	Amplifier, 2605	62-600203
CR1- ,CR201-208	Diode Array, CA 3039	62-600091
CR9	Diode IN 938	66-300938
R1-9,R25	Res, FXD Comp, 1K, 1/4W 5%	32-301410
R-10-17,20,30,34 37,40,43,56,61,66 279,203,205,208, 211,214,226,230, 234	Res, FXD Comp, 5.6K 1/4W, 5%	32-301456
R27	Res, FXD Comp, 47Ω ¼W 5%	32-301247
R29,33,36,39,42 55,60,65,201,206 209,212,215,227, 231,235	Res, FXD Comp, 51K ¼W 5%	32-301551
R52,R223	Res, FXD Comp, 1K, ¼W 5%	32-301820
R101,R264	Res, FXD Comp, 82Ω ¼W 5%	32-301282
R103,R104,277,278	Res, FXD Comp, 10K, ¼W,5%	32-301510
R19	Res, MF, 1.13K, ¼W,1%	31-224113
R19,24	Res, MF 1.13K, ¼W,1%	31-224200
R28	Res, MF 499Ω, ¼W,1%	31-223499

Schematic Reference	Description		Varian Part No.
R28	Res, MF	634Ω ¼W 1%	31-223634
R31,47,70	Res, MF	28K ¼W 1%	31-225280
R202,219,239	Res, MF	28K ¼W 1%	31-225280
R32	Res, MF	2M ¼W 1%	31-607200
R204	Res,MF	2M ¼W 1%	31-607200
R35	Res, MF	1M ¼W 1%	31-227100
R207	Res, MF	1M ¼W, 1%	31-227100
R38	Res, MF	499K, ¼W, 1%	31-226499
R210	Res, MF	499K, ¼W, 1%	31-226499
R41	Res, MF	249K, ¼W, L%	31-226249
R213	Res, MF	249K, ¼W, 1%	31-226249
R44	Res, MF	274K, ¼W, 1%	31-225274
R67,216,236	Res, MF	274K, ¼W, 1%	31-225274
R46,R69	Res, MF	16.2K, ¼W, 1%	31-225162
R268,269	Res, MF	16.2K, ¼W, 1%	31-225162
R48,R71	Res, MF	5.9K, ¼W, 1%	31-224590
R218,238	Res, MF	5.9K, ¼W, 1%	31-224590
R49,R72	Res, MF	13.7K, ¼W, 1%	31-225137
R220,240	Res, MF	13.7K, ¼W, 1%	31-225137
R57	Res, MF	110K, ¼W, 1%	31-226110
R229	Res, MF	110K, ¼W, 1%	31-226110
R62	Res, MF	56.2K, ¼W, 1%	31-225562
R232	Res, MF	56.2K, ¼W, 1%	31-225562
R74	Res, MF	14K, ¼W, 1%	31-225140
R243	Res, MF	14K, ¼W, 1%	31-225140
R75	Res, MF	3.01, ¼W, 1%	31-224301
R242	Res, MF	3.01, ¼W, 1%	31-224301
R76,R270	Res, MF	8.45, ¼W, 1%	31-224845
R79,R247	Res, MF	6.98K, ¼W, 1%	31-224698
R80,R246	Res, MF	1.47K, ¼W, 1%	31-224147
R81,R271	Res, MF	4.22K, ¼W, 1%	31-224422
R83,R248	Res, MF	2.49K, ¼W, 1%	31-224249
R85,R272	Res, MF, 2.15K, ¼W, 1%		31-224215

Schematic Reference	Descri
R86,R251	Res, MF,
R87,R249	Res, MF,
R89,R252	Res, MF,
R93,R254	Res, MF,
R95,R257	Res, MF,
R276,R98	Res, MF,
R18	Res, MF,
R23	Res, MF,
R68,R237	Res, MF,
R73,R100,R241, R263	Res, MF,
R78,R245	Res, MF,
R84,R100,R250 R263,	Res, MF,
R90.R253	Res, MF,
R96,100,258,263	Res, MF,
R97,R274	Res, MF,
R97,R274	Res, MF,
R91,R273	Res, MF,
R92,R256	Res, MF,
R22	Res, VAR
R88,260	Res, VAR
R82,R259	Res, VAR
R94,R261	Res, VAR
R98,R275, R21	Res, VAR
R45,R217	Res, MF,
R50,R222	Res, MF,
R51,R221	Res, MF,
R54,R225	Res, MF,
R59,R228	Res, MF,
R64,R233	Res, MF,
R77,R244	Res, MF,

n No.	Schematic Reference	Description		Varian Part No.
00351	R28	Res, MF	634Ω ¼W 1%	31-223634
	R31,47,70	Res, MF	28K ¼W 1%	31-225280
00013	R202,219,239	Res, MF	28K ¼W 1%	31-225280
00355	R32	Res, MF	2M ¼W 1%	31-607200
00356	R204	Res, MF	2M ¼W 1%	31-607200
00359	R35	Res, MF	1M ¼W 1%	31-227100
00260	R207	Res, MF	1M ¼W, 1%	31-227100
	R38	Res, MF	499K, ¼W, 1%	31-226499
00400	R210	Res, MF	499K, ¼W, 1%	31-226499
00365	R41	Res, MF	249K, ¼W, L%	31-226249
00270	R213	Res, MF	249K, ¼W, 1%	31-226249
00310	R44	Res, MF	274K, ¼W, 1%	31-225274
00357	R67,216,236	Res, MF	274K, ¼W, 1%	31-225274
00203	R46,R69	Res, MF	16.2K, ¼W, 1%	31-225162
00091	R268,269	Res, MF	16.2K, ¼W, 1%	31-225162
00938	R48,R71	Res, MF	5.9K, ¼W, 1%	31-224590
	R218,238	Res, MF	5.9K, ¼W, 1%	31-224590
01410	R49,R72	Res, MF	13.7K, ¼W, 1%	31-225137
01456	R220,240	Res, MF	13.7K, ¼W, 1%	31-225137
	R57	Res, MF	110K, ¼W, 1%	31-226110
	R229	Res, MF	110K, ¼W, 1%	31-226110
01247	R62	Res, MF	56.2K, ¼W, 1%	31-225562
01551	R232	Res, MF	56.2K, ¼W, 1%	31-225562
	R74	Res, MF	14K, ¼W, 1%	31-225140
	R243	Res, MF	14K, ¼W, 1%	31-225140
01820	R75	Res, MF	3.01, ¼W, 1%	31-224301
01282	R242	Res, MF	3.01, ¼W, 1%	31-224301
01510	R76,R270	Res, MF	8.45, ¼W, 1%	31-224845
24113	R79,R247	Res, MF	6.98K, ¼W, 1%	31-224698
24200	R80,R246	Res, MF	1.47K, ¼W, 1%	31-224147
23499	R81,R271	Res, MF	4.22K, ¼W, 1%	31-224422
	R83,R248	Res, MF	2.49K, ¼W, 1%	31-224249
	R85,R272	Res, MF, 2.15K, ¼W, 1%		31-224215

Schematic Reference	Description	Varian Part No.
R86,R251	Res, MF, 3.48, ¼W, 1%	31-224348
R87,R249	Res, MF, 750Ω, ¼W, 1%	31-223750
R89,R252	Res, MF, 1.62K, ¼W, 1%	31-224162
R93,R254	Res, MF, 383Ω, ¼W, 1%	31-223383
R95,R257	Res, MF, 806Ω, ¼W, 1%	31-223806
R276,R98	Res, MF, 52.3K,1%, ¼W	31-225523
R18	Res, MF, 10K, 1%	31-239033
R23	Res, MF, 10.5K, 1%	31-239057
R68,R237	Res, MF, 128K, .01%	31-239114
R73,R100,R241, R263	Res, MF, 64K, .01%	31-239054
R78,R245	Res, MF, 32K,.01%	31-239053
R84,R100,R250 R263,	Res, MF, 16K, .01%	31-239052
R90.R253	Res, MF, 8K, .01%	31-239051
R96,100,258,263	Res, MF, 4k, .01%	31-239050
R97,R274	Res, MF, 4.1K, 1%	31-239048
R97,R274	Res, MF, 21.5K, 1%	31-239060
R91,R273	Res, MF, 1.02K, 1W, 1%	31-464102
R92,R256	Res, MF, 1.78k, 1W, 1%	31-464178
R22	Res, VAR W.W., 50Ω	37-577308
R88,260	Res, VAR W.W., 200Ω	37-577310
R82,R259	Res, VAR W.W., 2K	37-577312
R94,R261	Res, VAR W.W., 100Ω	37-577309
R98,R275, R21	Res, VAR W.W.., 1K	37-577311
R45,R217	Res, MF, 125K, ¼W, .01%	31-613328
R50,R222	Res, MF, 62.5K, ¼W, 01%	31-613341
R51,R221	Res, MF, 100Ω, ¼W, 01%	31-613308
R54,R225	Res, MF, 1.538K, ¼W, .01%	31-613338
R59,R228	Res, MF, 512K, ¼W, 01%	31-613339
R64,R233	Res, MF, 256K, ¼W, .01%	31-613340
R77,R244	Res, MF, 6.81K, ¼W, 0.1%	31-613342

USER'S GUIDE
HIGH-LEVEL MULTIPLEXER MODULE

for use with

Varian 620 and V73 Series Computers

Publication No. 03-996 807A

February 1973

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FIGURES

TABLES

1. INTRODUCTION

1.1 GENERAL

The High-Level Multiplexer Module (MUX) is a hardware option that is used with an Analog-to-Digital Converter Module (ADCM) to expand the analog input capability of Varian 620 and V-73 series computers. The MUX provides high-level multiplexing and channel control.

The MUX provides 16 single-ended or differential external analog channels. In addition, the MUX can be expanded by adding 16-channel Multiplexer Expansion Modules (MUXEs). As many as 15 MUXEs can be attached to each MUX to provide a total of 256 analog input channels for the ADCM.

1.2 FUNCTIONAL DESCRIPTION

Figure 1-1 illustrates the functional elements included in a MUX module. In a configuration employing MUXE modules, the MUX serves as the master module which contains the control logic. The MUXEs, called slave modules, contain only those circuits shown in the shaded area of Figure 1-1. The MUX shares the interface logic shown in the unshaded area with the MUXEs via jumper connections.

Device Address

One to 16 multiplexer and multiplexer expansion modules may be located at one device address. The device address may be any octal number from 40 to 77. The MUX, which is the master module, contains the device address decode logic.

Channel Selection Mode

The multiplexer is designed to operate in either sequential or random mode under computer program control. The mode of channel selection is specified by the program using a standard assembly language instruction.

In sequential mode, the multiplexer module's channel address decode logic automatically increments from channel address 1 to the final address prescribed by the program.

In random mode, the MUX channel address selection is controlled by the computer program. This mode permits the selection of MUX and MUXE channels in any sequence.

Channel Address Decode

The MUX channel address decode logic converts the eight-bit channel address received from the computer into two four-bit select codes. The select codes are routed to the channel on the MUX and MUXEs by jumper connections.

Channel Select Switches

The eight bits of the select code close either one or a pair of channel select switches on a single module to connect the analog input signal on a single-ended or differential channel to the ADCM. Only one switch or pair of switches can be closed at a time.

End of Scan Sense

The program can determine when a sequential channel selection operation is complete by issuing a Sense instruction that selects the End of Scan Sense input line. This line is logically true when the channel address decode selects the final channel address in a sequential operation.

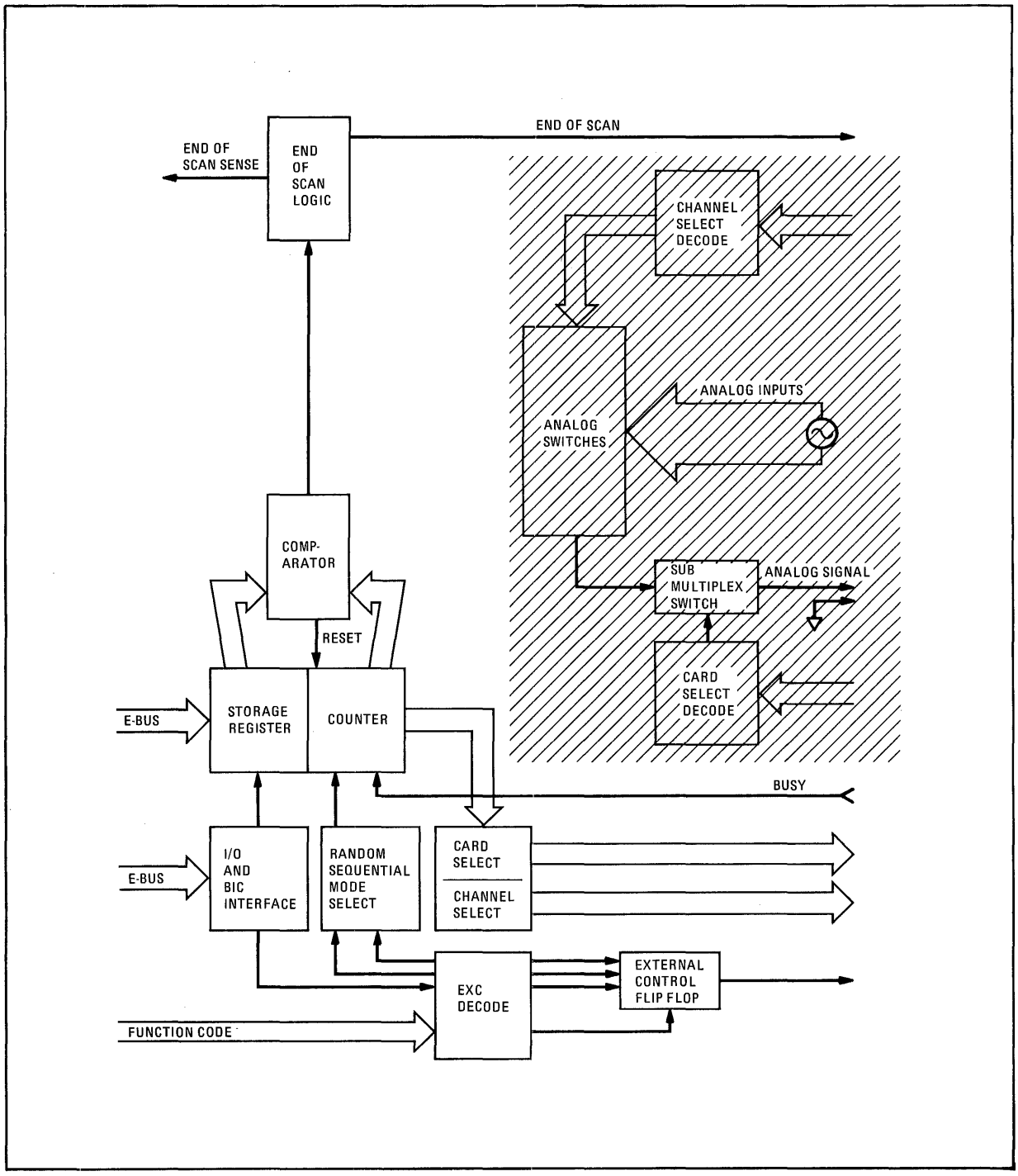


Figure 1-1. Multiplexer Module Block Diagram

2. PROGRAMMING

2.1 INTRODUCTION

This section describes Assembly Language programming techniques for operating the multiplexer. The program directs MUX operation in four ways:

- Determines mode of channel selection.
- Loads channel select codes into the channel select decode logic.
- Enables operation under BIC control.
- Tests for end of scan in sequential mode.

Note that generalized driver programs are supplied with the MUX to accomplish these same functions. Complete details regarding these programs may be found in the Analog-to-Digital Converter User's Guide (Publication No. 03-996 806). That manual also describes the software test package that is provided for ADCM/MUX checkout.

More detailed programming information may be found in the 620 series or V-73 system handbooks.

2.2 MODE SELECTION

The program specifies the mode of channel selection with an EXC instruction. Sequential channel selection is specified with an EXC 02YY instruction, where YY is the MUX device address. Random channel selection is specified with an EXC 01YY instruction.

2.3 CHANNEL SELECT CODE TRANSFER

The program specifies which channel is to be selected by an eight-bit channel select code. This code may be transferred from the computer's A or B register or from memory to the multiplexer using a standard data transfer out operation. The channel select code transfer is accomplished with one of the following instructions:

OAR 0YY Load device YY from A register

OBR 0YY Load device YY from B register

OME 0YY Load device YY from memory

where YY is the MUX device address

In sequential mode, only the channel select code for the final channel address is sent to the multiplexer; all channel select codes from channel address 1 to the final channel address are automatically generated by the MUX once the sequence has begun.

In random mode, each new channel select code requires a separate data transfer out operation. The data transfer operation may be under program control or BIC control.

2.4 BIC ENABLE

The program enables the multiplexer to operate in conjunction with the BIC by issuing an EXC 0YY instruction, where YY is the MUX device address. This sets the MUX in random mode. It also enables it to be connected to the BIC in order to pass random MUX channel addresses to the MUX from memory via the BIC.

2.5 END OF SCAN SENSE

The program can test the status of a sequential channel selection operation to determine if the MUX has selected the final channel (end of scan). It does this by issuing a SEN 0YY instruction. A true level on the computer's sense input line, SERX-I, indicates that the MUX has completed its scan.

The end of scan signal can also provide an interrupt to the program if the optional PIM module is employed.

2.6 TIMING CONSIDERATIONS

The channel selection process requires a delay of approximately 10 microseconds from the start of the channel selection to the start of the analog-to-digital conversion.

For each selected channel in random mode, the delay would extend from the transfer of the channel address to the signal that starts the ADC. In sequential mode, the delay would be required only before the first analog-to-digital conversion. In this case the subsequent delays are provided by the conversions themselves, since the subsequent channel selections occur at the beginning of the following conversions.

The source of the delay will depend on the source of the Start ADC signal. This may be a program start, timer start, or external start. Refer to the ADCM User's Guide for details regarding Start ADC signals.

2.7 PROGRAMMING EXAMPLES

The following examples illustrate typical instruction sequences for programming the multiplexer. In these examples, device address octal 60 is assumed for the ADCM, and device address octal 40 is assumed for the MUX.

Random Mode Channel Selection

```
        LDX     RAN1
        EXC     0140            Select random mode
RAN2    LDA     0,1             Relative to X
        OAR     040             Output to MUX
        LDB     RAN3            Load delay interval
RAN7    DBR                     Delay
        JBZ     RAN6            Check end of delay
        JMP     RAN7            Continue delay
RAN6    EXC     0160            Start ADC
        SEN     060, RAN8       If data ready, read ADC
        JMP     *-2             Not ready continue wait loop
```

```
RAN8    CIA     060         Read ADC
        STA     RAN4, 1     Store data word
        IXR
        TXA
        SUB     RAN5
        SUB     RAN1
        JAN     RAN2
        HLT
RAN1    DATA    xxx         Points to start of channel numbers
RAN3    DATA    xxx         Delay interval
RAN4    DATA    xxx         Points to start of data
RAN5    DATA    xxx         Number of data words
```

Sequential Mode Channel Selection

```
        LDX     SEQ1
        EXC     0240        Select sequential mode
        LDAI    020         Channel 16 is last channel
        OAR     040         Output to MUX
        LDBI    SEQ2        Load delay interval
SEQ5    DBR                 Delay
        JBZ     SEQ3        Check end of delay
        JMP     SEQ5        Continue delay
SEQ3    EXC     0160        Start ADC
        SEN     060, SEQ6   If data ready, read ADC
```

```
        JMP     *-2             Not ready, continue wait loop
SEQ6    CIA     060             Read ADC
        STA     0, 1            Store data word
        IXR
        TXA
        SUB     SEQ4
        SUB     SEQ1
        JAN     SEQ3
        HLT
SEQ1    DATA    xxx             Points to start of data
SEQ2    DATA    xxx             Delay interval
SEQ4    DATA    xxx             Number of data words
```

3. THEORY OF OPERATION

3.1 CHANNEL SELECTION

Channel selection may occur in either of two modes, random or sequential. For sequential operation, the program specifies a final channel address and the multiplexer automatically increments the channel selection logic from channel address 1 to the specified channel. In the random mode, the program specifies the next channel address for each selection; transfer of the channel address word may be under direct program control or BIC control.

Sequential Mode

The program prepares a set of multiplexer modules for sequential channel selection by issuing an EXC 02YY instruction. This sets the Sequential/Random latch on the master module, which remains set until the program issues an EXC 0YY or EXC 01YY instruction or until System Reset is generated. The Q output of the Sequential/Random latch conditions the channel address decode logic for sequential operation.

Following the mode selection, the final channel address is sent to the master module. At the start of the data transfer out operation that executes the address transfer, the DTOS latch is set. The true output of the DTOS latch conditions the clock input gate to the channel address buffer register in preparation for the DRYX (Data Ready) pulse.

The leading edge of DRYX loads the channel address present on E-bus lines EB00 through EB07 into the buffer register. The Load pulse also resets all eight channel address decode latches.

The output of the channel address buffer register and the eight channel address decode latches are set into an eight-bit comparator. The output of the comparator remains logically true (relative high) as long as the present channel address (output of the decode latches) is less than the final channel address (output of the buffer register).

In the sequential mode, the decode latches operate as an eight-bit cascade counter. The counter begins operation reset to 1 (by the Load pulse). A clock input pulse (CLK) increments the counter by one with each analog-to-digital conversion.

At the start of a conversion, the signal Busy from the ADCM goes true. This results in the positive-going pulse CLK, which clocks the channel address decode latches.

When the output of the decode latches equals the final channel address, the output of the comparator goes false (relative low). This output sets the End of Scan latch on the trailing edge of the final CLK pulse in the sequence. The true output of the End of Scan latch is gated with Convert, a signal that is the equivalent of Busy, to reset the channel address decode latches to 1.

If the program issues a SEN 0YY instruction, the signal Select 0 is generated. This signal gates the status of the End of Scan latch onto SERX-I, the sense input to the computer.

End of Scan, inverted once, is also available at P1-89 and may be used with the priority interrupt feature.

Random Mode

The program specifies the random channel selection mode by issuing an EXC 01YY instruction. This resets the Sequential/Random latch on the master module, which remains reset until the program issues an EXC 02YY instruction. The $\overline{Q}$ output of the latch conditions the channel address decode logic for random operation.

Following the mode selection, the address of the first channel to be selected is sent to the master module from the computer. Transfer of the address may be either a program-controlled or BIC-controlled data transfer out operation.

In either case, the channel address is loaded into the buffer register by the Load pulse, which is generated by DRYX from the computer and either DTOS (for program-controlled transfers) or Transfer Enable (for BIC-controlled transfers).

Load is also gated through with the mode signal, Random, to strobe the channel address from the buffer register into the decode latches. Each subsequent channel address transferred in the random mode is loaded into the buffer register and strobed into the decode latches in the same manner. The outputs of the comparator and End of Scan latch have no significance in the random mode.

3.2 CHANNEL SELECT SWITCHES

The eight bits output from the channel address decode logic are routed to the channel select switches on the master and slave modules. The four least significant bits (called A, B, C, and D) select one pair out of 16 pairs of select switches on each module. The four most significant bits (called E, F, G, and H) select the module to which the designated channel is connected.

If there are 32 channels located at the addressed module, the four most significant bits (E, F, G, and H) select the module, and select signal E inhibits one half of each pair of switches selected by signals A, B, C, and D. Jumper wires are required on the module for 32 channel operation. These jumpers are: JPRA, JPRB, JPRC, and JPRD.

The jumper wires used for routing the channel select bits are connected from module to module in an unchanging pattern. The jumper wires that route the card select bits are connected to either the inverting or noninverting input pins of the different modules in combinations that give each module a unique submultiplexing address.

A blanking pulse is applied to all channel select switches with each new channel address selection. This is done to assure that the switch(es) previously selected opens before the newly selected switch(es) closes.

The signal, Blanking, is generated by the Load pulse when channel selection is in the random mode and by CLK when channel selection is in the sequential mode.

3.3 SWITCH DESIGN

The switch design (Figures 3-1 and 3-2) is of monolithic construction with bipolars and FETS on one chip. The design incorporates the following features:

- P-Channel MOS FET switch and driver
- 20-Volt peak-to-peak signal handling capability
- TTL, DTL, RTL direct drive compatibility
- Voltage-limiting diodes protect MOS gate

Each element contains four MOS field-effect transistors designed to function as electronic switches. Level-shifting drivers enable a low-level input (0.8 to 2.0 V) to control the ON-OFF condition of each switch. In the ON state, each switch will conduct current equally well in either direction. In the OFF state, the switches will block voltages up to 20 V peak-to-peak. Positive logic "0" at the driver input will turn each switch ON. A common driver terminal V_L may be used to clock all four switches by switching the device from the ENABLE mode (≥ 4 V) to the INHIBIT mode (≤ 0.4 V).

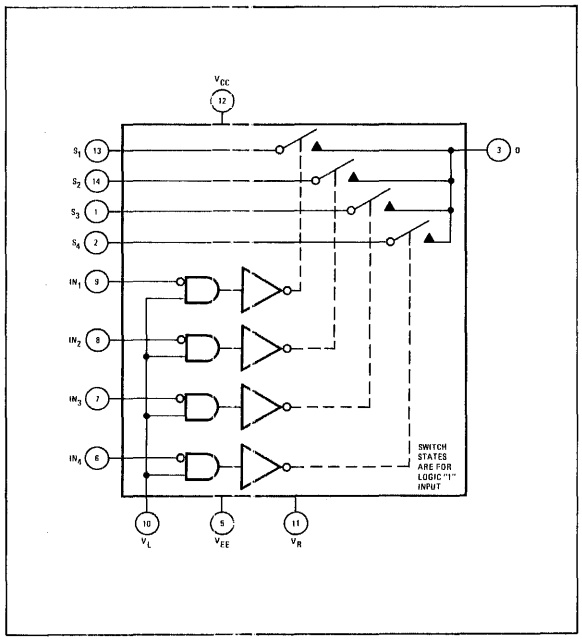


Figure 3-1. MOS Switches With Drivers-Functional Diagram

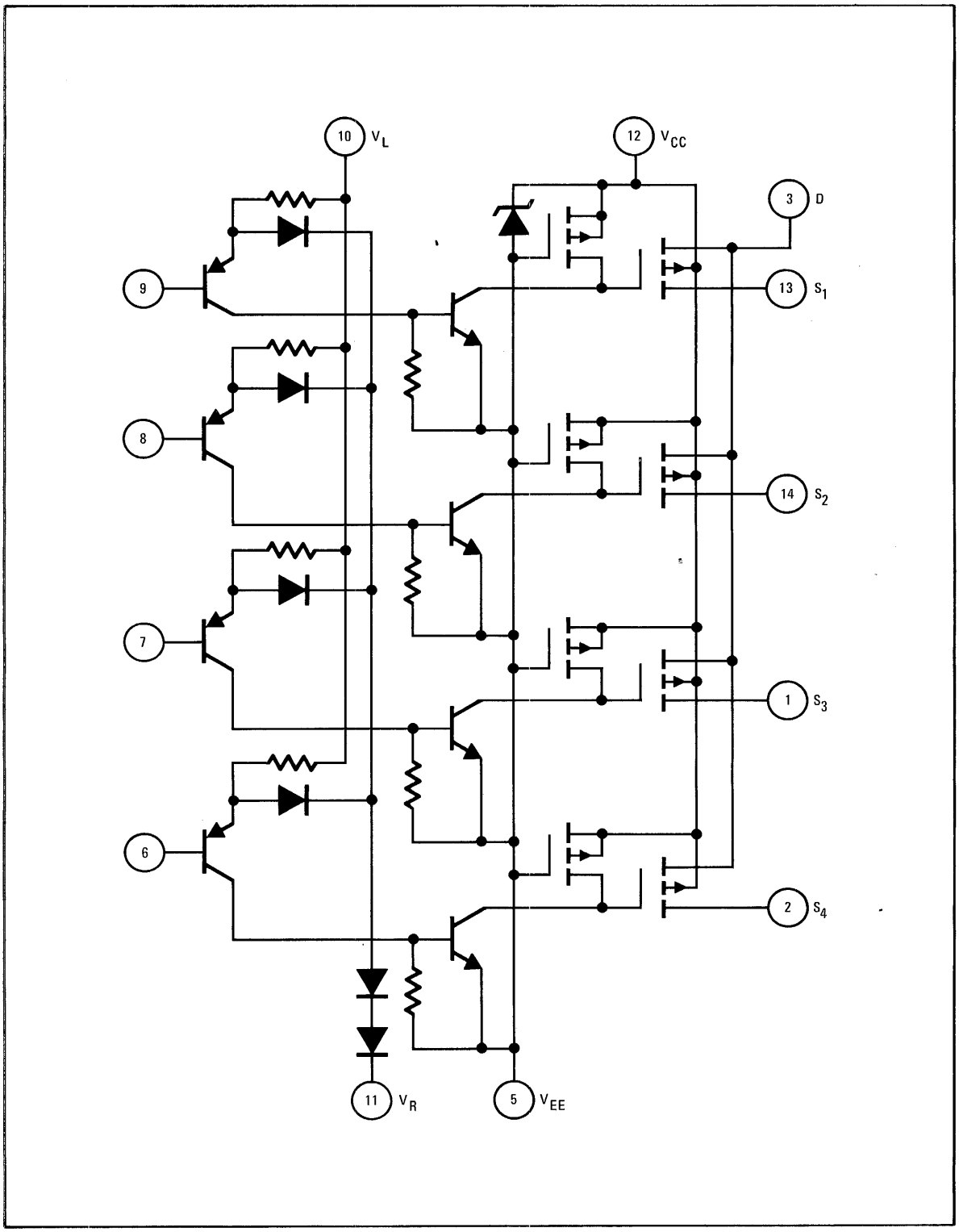


Figure 3-2. MOS Switches With Drivers - Schematic Diagram

4. INSTALLATION

4.1 PREREQUISITES

Each MUX or MUXE requires one card slot in either the mainframe or Memory Expansion/Peripheral Controller frame. No special slots are reserved for use by the multiplexer modules. However, those modules used in conjunction with an ADCM should be installed in adjacent slots to simplify backplane wiring. Note that an example of a typical ADCM/MUX installation procedure is given in the ADCM User's Guide.

A Power Supply Module (Part No. 620-88) must be installed when using one or more multiplexer modules. If a Power Supply Module has been previously installed and sufficient current is available to support the multiplexer modules, an additional module need not be installed.

4.2 INSTALLATION AND INTERCONNECTION

A MUX or MUXE is installed vertically, with its component side to the installer's left in 620/i and 620/L computers, and horizontally in the 620/f computer. Figure 4-1 illustrates a typical installation.

CAUTION

Do not install multiplexer modules in slots that have been previously wired to provide power to other modules; if the intended slot is already wired, remove any connections to power before installing the multiplexer module to protect its components. Refer to Table 4-1 for proper power connections.

The card is installed with the double pin edge pointing toward the installer. Proper orientation of the module is important since the cards are not keyed.

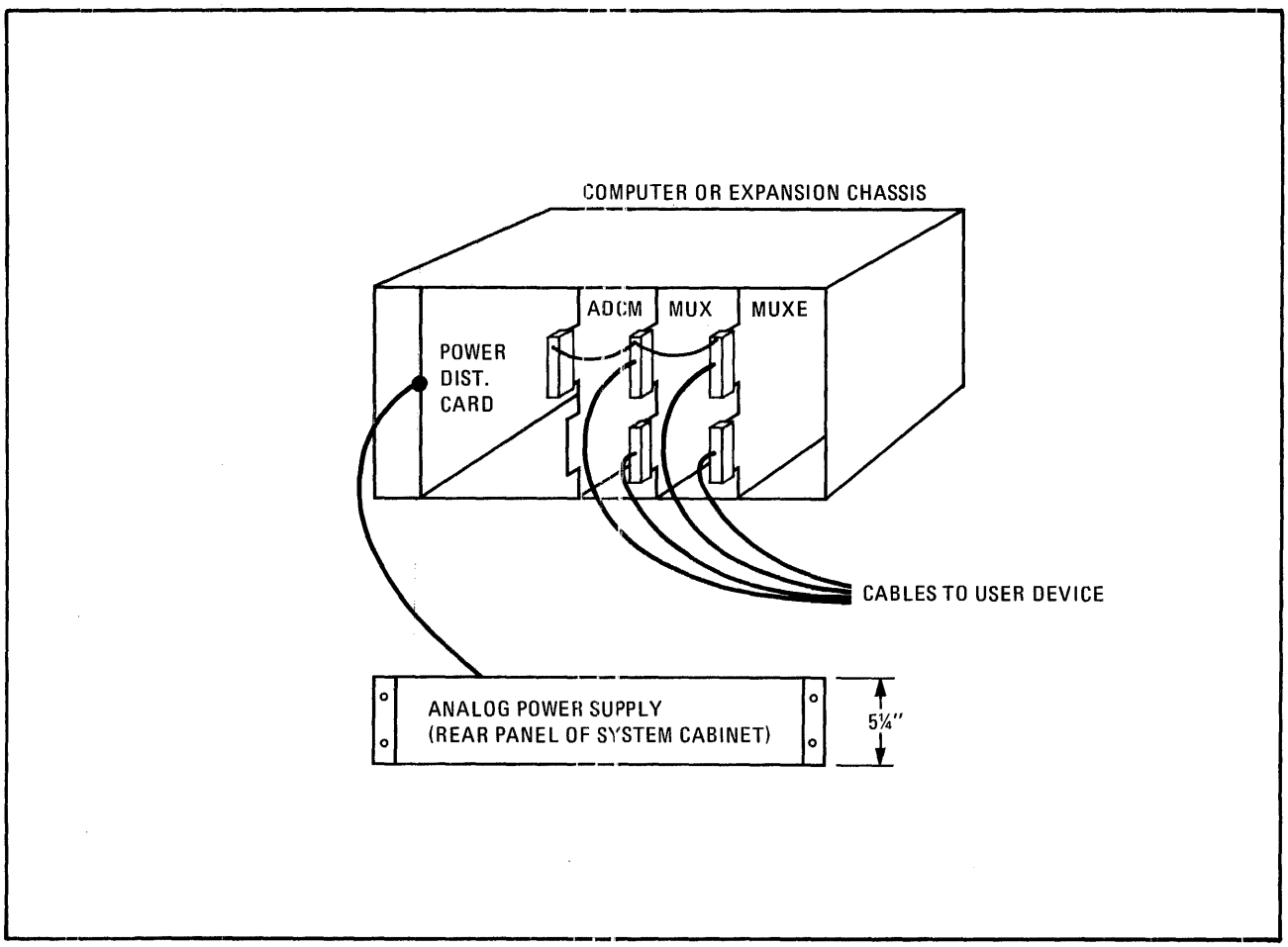


Figure 4-1. Typical Multiplexer Module Installation

Connections to external instruments include, for each multiplexer module, 16 single-ended or 16 differential analog inputs. All pin assignments for these connections are listed in Appendix A.

Power Supply Wiring

Connections to the multiplexer module must be made for five power supply voltages and senses, an analog ground, a digital ground and a digital ground sense. Table 4-1 lists the pin assignments on the MUX wirewrap backplane for these connections. When the multiplexer module is used with other modules (ADCMs, MUXEs, etc.) similar voltages should be tied together, and the voltage sense line should be brought from the mid-point of the voltage tie-line to a voltage sense line on the power supply wirewrap backplane.

The voltages and sense points for the power supply backplane are given in the Power Supply Manual (Publication No. 03-996-812).

Table 4-1. MUX Wirewrap Backplane Pin Connections for Power Supply

Power Supply Voltage	Multiplexer Pins
Digital Ground	P1-1, 22, 48, 51, 100, and 122
+5 Vdc	P1-118, 121
+15 Vdc	P1-111, 112
+20 Vdc	P1-107, 108
-15 Vdc	P1-113, 114
-22 Vdc	P1-109, 110
Analog Ground	P1-115

Device Address Wiring

Table 4-2 lists the jumper connections required to wire a device address for a multiplexer module. Although Table 4-2 lists the connections for device addresses 040 through 077, multiplexer modules are typically assigned device addresses 060 through 067. Note that P1-74 (Enable) is not normally used. It is available, however, and may be used as an additional addressing condition. For example, if two multiplexer modules are assigned the same device address, the Enable input can be used to permit only one module to respond to that address at a given time.

Card/Channel Selection Wiring

Tables 4-3 through 4-5 list the jumper connections required for preparing MUX and MUXE modules for card and channel selection. Note that Tables 4-3 and 4-5 apply only to those configurations in which MUXEs are used.

Table 4-3 shows the initial connections for daisy chain wirewrap of MUX and MUXE modules used in the same configuration.

Table 4-2. Multiplexer Module Device Address Wiring

Address	Wirewrap Jumpers (P1xx to P1xx)				
040	77 to 78	74 to 75	71 to 72	68 to 69	65 to 66
041	77 to 78	74 to 75	71 to 72	68 to 69	64 to 66
042	77 to 78	74 to 75	71 to 72	67 to 69	65 to 66
043	77 to 78	74 to 75	71 to 72	67 to 69	64 to 66
044	77 to 78	74 to 75	70 to 72	68 to 69	65 to 66
045	77 to 78	74 to 75	70 to 72	68 to 69	64 to 66
046	77 to 78	74 to 75	70 to 72	67 to 69	65 to 66
047	77 to 78	74 to 75	70 to 72	67 to 69	64 to 66
050	77 to 78	73 to 75	71 to 72	68 to 69	65 to 66
051	77 to 78	73 to 75	71 to 72	68 to 69	64 to 66
052	77 to 78	73 to 75	71 to 72	67 to 69	65 to 66
053	77 to 78	73 to 75	71 to 72	67 to 69	64 to 66
054	77 to 78	73 to 75	70 to 72	68 to 69	65 to 66
055	77 to 78	73 to 75	70 to 72	68 to 69	64 to 66
056	77 to 78	73 to 75	70 to 72	67 to 69	65 to 66
057	77 to 78	73 to 75	70 to 72	67 to 69	64 to 66
060	76 to 78	74 to 75	71 to 72	68 to 69	65 to 66
061	76 to 78	74 to 75	71 to 72	68 to 69	64 to 66
062	76 to 78	74 to 75	71 to 72	67 to 69	65 to 66
063	76 to 78	74 to 75	71 to 72	67 to 69	64 to 66
064	76 to 78	74 to 75	70 to 72	68 to 69	65 to 66
065	76 to 78	74 to 75	70 to 72	68 to 69	64 to 66
066	76 to 78	74 to 75	70 to 72	67 to 69	65 to 66
067	76 to 78	74 to 75	70 to 72	67 to 69	64 to 66
070	76 to 78	73 to 75	71 to 72	68 to 69	65 to 66
071	76 to 78	73 to 75	71 to 72	68 to 69	64 to 66
072	76 to 78	73 to 75	71 to 72	67 to 69	65 to 66
073	76 to 78	73 to 75	71 to 72	67 to 69	64 to 66

Table 4-2. Multiplexer Module Device Address Wiring (Con't.)

Address	Wirewrap Jumpers (P1xx to P1xx)				
074	76 to 78	73 to 75	70 to 72	68 to 69	65 to 66
075	76 to 78	73 to 72	70 to 72	68 to 69	64 to 66
076	76 to 78	73 to 75	70 to 72	67 to 69	65 to 66
077	76 to 78	73 to 75	70 to 72	67 to 69	64 to 66

Table 4-3. Daisy Chain Wirewrap Connections for Multiplexer Modules

Signal	MUX to	MUXE1 to . . .	to	MUXEn
Blanking	P1-42	P1-42	P1-42	P1-42
Chan Sel-A	P1-86	P1-86	P1-86	P1-86
Chan Sel-B	P1-85	P1-85	P1-85	P1-85
Chan Sel-C	P1-84	P1-84	P1-84	P1-84
Chan Sel-D	P1-102	P1-102	P1-102	P1-102
Card Sel-E	P1-104	P1-104	P1-104	P1-104
Card Sel-F	P1-105	P1-105	P1-105	P1-105
Card Sel-G	P1-90	P1-90	P1-90	P1-90
Card Sel-H*	P1-92	P1-92	P1-92	P1-92

*Card Sel-H must be inverted to operate modules with channel addresses above 128.

Signal	(Any slot below chan 129)	to	(Any slot above chan 128)	to	(Any slot above chan 128)
Card Sel-H	P1-92		P1-83		P1-83
H-Inverted			P1-94 to P1-92		P1-94 to P1-92

Table 4-4 shows the connections required on the master MUX module to provide 16-channel operation.

Table 4-4. MUX Wirewrap Jumpers

Signal	MUX	to	ADC
Busy	P1-101		P1-75
Decode 0	P1-91 to P1-80		
Decode 1	P1-93 to P1-81		

Table 4-5 lists the internal connections to wire each MUXE channel address group.

Table 4-5. MUXE Wirewrap Jumpers

Channel Address Group	From P1-xx	To P1-xx
17 to 32 (MUXE1)	93 95	80 81
33 to 48 (MUXE2)	95 96	80 81
49 to 64 (MUXE3)	96 97	80 81
65 to 80 (MUXE4)	97 98	80 81
81 to 96 (MUXE5)	98 99	80 81
97 to 112 (MUXE6)	99 103	80 81
113 to 128 (MUXE7)	103 106	80 81

Table 4-5. MUXE Wirewrap Jumpers (Con't)

Channel Address Group	From P-1xx	To P1-xx
129 to 144 (MUXE8)	91 93	80 81
145 to 160 (MUXE9)	93 95	80 81
161 to 176 (MUXE10)	95 96	80 81
177 to 192 (MUXE11)	96 97	80 81
193 to 208 (MUXE12)	97 98	80 81
209 to 224 (MUXE13)	98 99	80 81
225 to 240 (MUXE14)	99 103	80 81
241 to 256 (MUXE15)	103 106	80 81

Analog Input Wiring

Connections for analog inputs are available at J1 and J2. Inputs may be either single-ended or differential for a differential MUX. If the MUX is single-ended, only single-ended inputs may be used. Note that differential is recommended since it simplifies system grounding procedures.

To allow full scale swing ($\pm$ 10 V) of the analog input signal, that signal must be referenced to the multiplexer ground. Figure 4-2 illustrates a typical application where the differential input leads are connected to J1-9 (high) and J1-7 (low), and the ground

line is connected to J1-8 (analog ground). Figure 4-3 shows a typical application where the single-ended input lead is connected to J1-7 (low) and the ground line is connected to J1-8 (analog ground). Figure 4-4 illustrates ground connections for sequencing the analog output signal through the multiplexer modules to the ADCM.

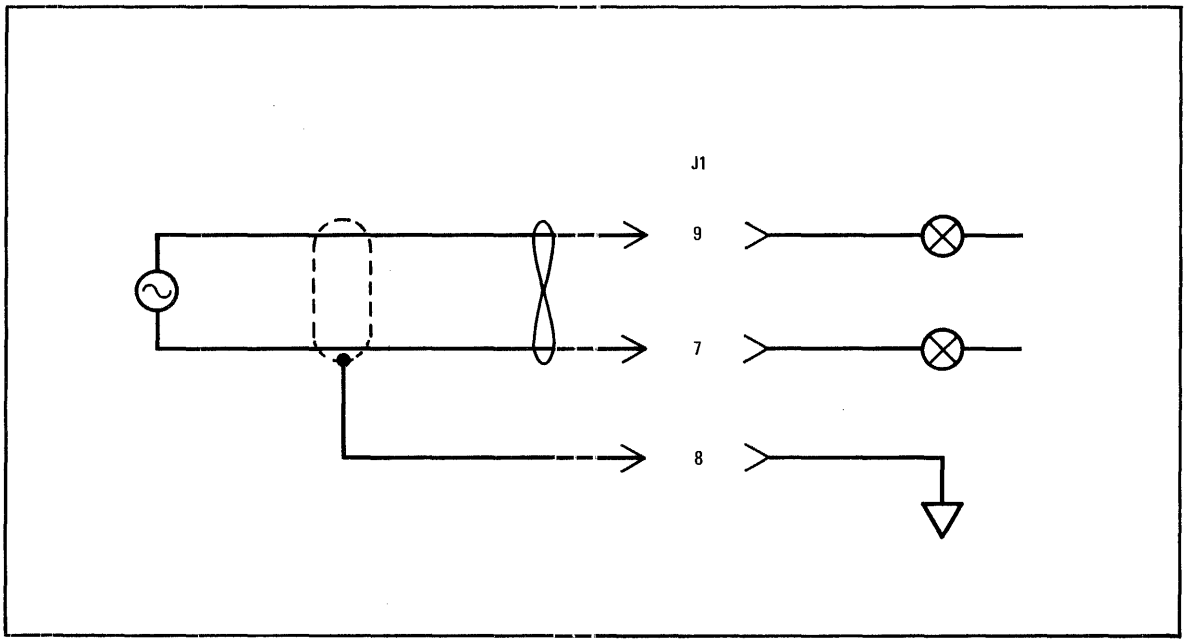


Figure 4-2. Differential Input Connections

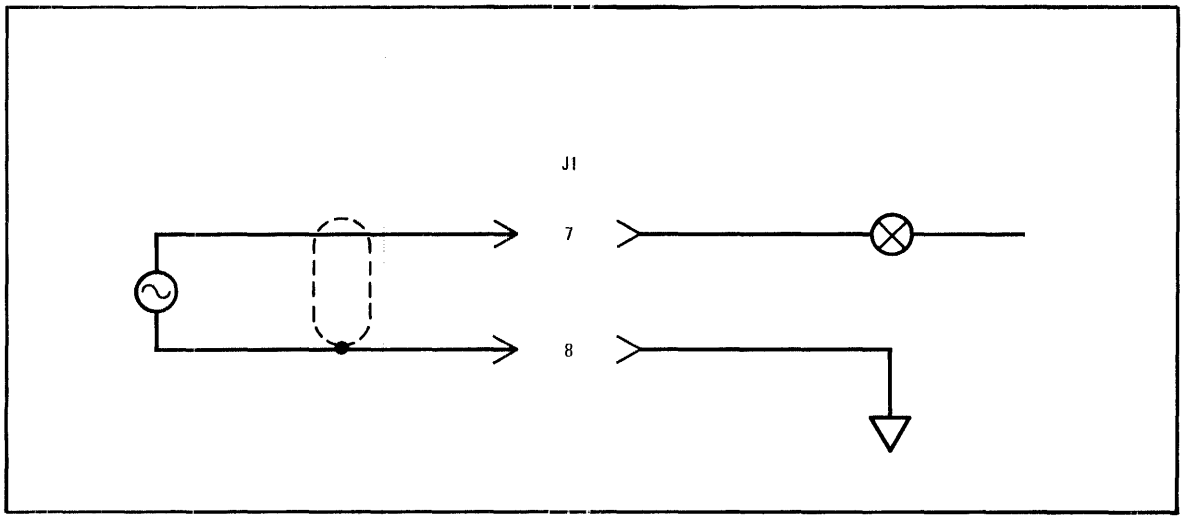


Figure 4-3. Single-Ended Input Connections

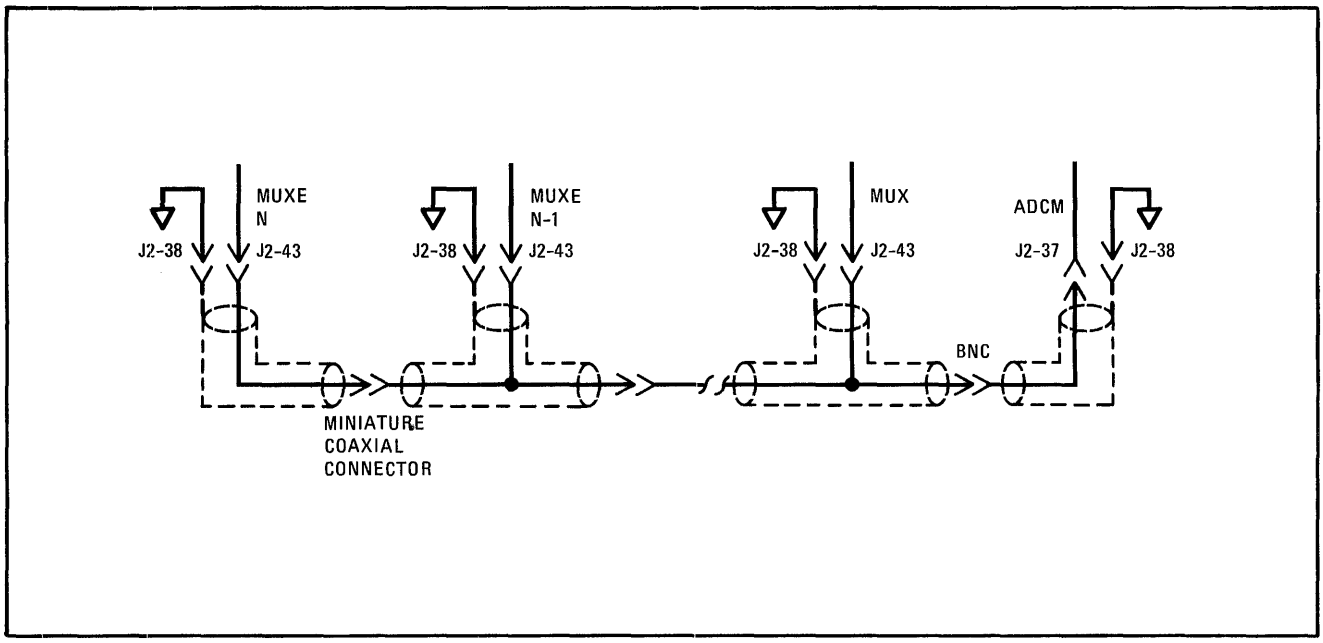


Figure 4-4. Daisy Chain of Analog Output Signal from MUX to ADCM

APPENDIX A: MUX PIN ASSIGNMENTS

BACKPLANE WIRING

Pin No.	Name	Name Function
P1-1	Digital Ground	Digital Ground
-2	EB00-I	EB00-I
-3	Digital Ground	Digital Ground
-4	EB01-I	EB01-I
-5	Digital Ground	Digital Ground
-6	EB02-I	EB02-I
-7	Digital Ground	Digital Ground
-8	EB03-I	EB03-I
-9	Digital Ground	Digital Ground
-10	EB04-I	EB04-I
-11	EB05-I	EB05-I
-12	EB06-I	EB06-I
-13	EB07-I	EB07-I
-14	EB08-I	EB08-I
-15	EB09-I	EB09-I
-16	EB10-I	EB10-I
-17	EB11-I	EB11-I
-18	EB12-I	EB12-I
-19	Not used	Not used
-20	EB14-I	EB14-I
-21	EB15-I	EB15-I
-22	Digital Ground	Digital Ground
-23	Not used	Not used
-24	Digtial Ground	Digital Ground
-25	Not used	Not used
-26	Digital Ground	Digtial Ground
-27	FRYX-I	FRYX-I
-28	Digital Ground	Digital Ground
-29	DRYX-I	DRYX-I
-30	Digital Ground	Digital Ground
-31	SERX-I	SERX-I
-32	Digital Ground	Digital Ground
-33	Not used	Not used
-34	Digital Ground	Digital Ground
-35	Not used	Not used
-36	Digital Ground	Digital Ground
-37	Not used	Not used
-38	Digital Ground	Digital Ground

Pin No.	Name	Name Function
-39	Not used	Not used
-40	Digital Ground	Digital Ground
-41	Not used	Not used
-42	BLANK	BLANK Assures channel select switches break before make
-43	SYRT-I	SYRT-I Resets system logic
-44	IUAX-I	IUAX-I Interrupt acknowledge from computer
-45	Not used	Not used
-46	Not used	Not used
-47	Not used	Not used
-48	Digital Ground	Digital Ground
-49	TRQX-B	TRQX-B Transfer request from multiplexer to BIC
-50	TROX-B	TROX-B Not used
-51	Digital Ground	Digital Ground
-52	Not used	Not used
-53	Digital Ground	Digital Ground
-54	CDCX-B	CDCX-B Notifies BIC that multiplexer is connected
-55	Digital Ground	Digital Ground
-56	DCEX-B	DCEX-B Connect signal from BIC
-57	Digital Ground	Digital Ground
-58	TAKX-B	TAKX-B Transfer request acknowledge from BIC
-59	Digital Ground	Digital Ground
-60	DESX-B	DESX-B Disconnect from BIC
-61	Not used	Not used
-62	Not used	Not used
-63		Output for EXC 3 latch
-64	EB00+	EB00+ Jumper connection for wiring device address
-65	EB00-	EB00- Jumper connection for wiring device address
-66	EB0I+	EB0I+ Jumper connection for wiring device address
-67	EB01+	EB01+ Jumper connection for wiring device address
-68	EB01-	EB01- Jumper connection for wiring device address
-69	EB1I+	EB1I+ Jumper connection for wiring device address
-70	EB02+	EB02+ Jumper connection for wiring device address
-71	EB02-	EB02- Jumper connection for wiring device address
-72	EB2I+	EB2I+ Jumper connection for wiring device address
-73	EB03+	EB03+ Jumper connection for wiring device address
-74	EB03-	EB03- Jumper connection for wiring device address
-75	EB3I+	EB3I+ Jumper connection for wiring device address
-76	EB04+	EB04+ Jumper connection for wiring device address

BACKPLANE WIRING

Pin No.	Name	Name Function
P1-77	EB04-	EB04- Jumper connection for wiring device address
-78	EB4I+	EB4I+ Jumper connection for wiring device address
-79	ENABLE	ENABLE Not normally used
-80	H	H Jumper connection for wiring card select code
-81	G	G Jumper connection for wiring card select code
-82	F	F Jumper connection for wiring card select code
-83	E	E Jumper connection for wiring card select code
-84	C	C Jumper connection for wiring channel select code
-85	B	B Jumper connection for wiring channel select code
-86	A	A Jumper connection for wiring channel select code
-87	Not used	Not used
-88	Not used	Not used
-89	EOS	EOS End of scan output to PIM
-90	G	G Jumper connection for wiring card select code
-91	Not used	Not used
-92	H	H Jumper connection for wiring card select code
-93	Not used	Not used
-94	H	H Jumper connection for wiring card select code
-95	Not used	Not used
-96	Not used	Not used
-97	Not used	Not used
-98	Not used	Not used
-99	Not used	Not used
-100	Digital Ground	Digital Ground
-101	Busy	Busy Busy input from ADCM
-102	D	D Jumper connection for wiring channel select code
-103	Not used	Not used
-104	E	E Jumper connection for wiring card select code
-105	F	F Jumper connection for wiring card select code
-106	Not used	Not used
-107	+20 V	+20 V
-108	+20 V	+20 V
-109	-20 V	-20 V
-110	-20 V	-20 V
-111	+15 V	+15 V
-112	+15 V	+15 V
-113	-15 V	-15 V
-114	-15 V	-15 V
-115	Analog Ground	Analog Ground
-116	Not used	Not used
-117	Not used	Not used

Pin No.	Name	Name Function
-118	+5 V	+ 5 V
-119	Not used	Not used
-120	Not used	Not used.
-121	+5 V	+5 V
-122	Digital Ground	Digital Ground

TERMINAL EDGE CONNECTOR WIRING

Pin No.	Name	Name Function
J1-1	Not used	Not used
-2	Not used	Not used
-3	Not used	Not used
-4	Not used	Not used
-5	Not used	Not used
-6	Not used	Not used
-7	CH-9L	CH-9L Analog input channel (DIFF and Single Ended)
-8	Analog Ground	Analog Ground
-9	CH-9H	CH-9H Analog input channel (DIFF only)
-10	Analog Ground	Analog Ground
-11	CH-10L	CH-10L Analog input channel (DIFF and Single Ended)
-12	Analog Ground	Analog Ground
-13	CH-10H	CH-10H Analog input channel (DIFF only)
-14	Analog Ground	Analog Ground
-15	CH-11L	CH-11L Analog input channel (DIFF and Single Ended)
-16	Analog Ground	Analog Ground
-17	CH-11H	CH-11H Analog input channel (DIFF only)
-18	Analog Ground	Analog Ground
-19	CH-12L	CH-12L Analog input channel (DIFF and Single Ended)
-20	Analog Ground	Analog Ground
-21	CH-12H	CH-12H Analog input channel (DIFF only)
-22	Analog Ground	Analog Ground
-23	CH-13L	CH-13L Analog input channel (DIFF and Single Ended)
-24	Analog Ground	Analog Ground
-25	CH-13H	CH-13H Analog input channel (DIFF only)
-26	Analog Ground	Analog Ground
-27	CH-14L	CH-14L Analog input channel (DIFF and Single Ended)
-28	Analog Ground	Analog Ground
-29	CH-14H	CH-14H Analog input channel (DIFF only)
-30	Analog Ground	Analog Ground
-31	CH-15L	CH-15L Analog input channel (DIFF and Single Ended)
-32	Analog Ground	Analog Ground
-33	CH-15H	CH-15H Analog input channel (DIFF only)

Pin No.	Name	Name Function
-34	Analog Ground	Analog Ground
-35	CH-16L	CH-16L Analog input channel (DIFF and Single Ended)
-36	Analog Ground	Analog Ground
-37	CH-16H	CH-16H Analog input channel (DIFF only)
-38	Analog Ground	Analog Ground
-39	Not used	Not used
-40	Not used	Not used
-41	Not used	Not used
-42	Not used	Not used
-43	Not used	Not used
-44	Not used	Not used
J2-1	Not used	Not used
-2	Not used	Not used
-3	Not used	Not used
-4	Not used	Not used
-5	Not used	Not used
-6	Not used	Not used
-7	CH-1L	CH-1L Analog input channel (DIFF and Single Ended)
-8	Analog Ground	Analog Ground
-9	CH-1H	CH-1H Analog input channel (DIFF only)
-10	Analog Ground	Analog Ground
-11	CH-2L	CH-2L Analog input channel (DIFF and Single Ended)
-12	Analog Ground	Analog Ground
-13	CH-2H	CH-2H Analog input channel (DIFF only)
-14	Analog Ground	Analog Ground
-15	CH-3L	CH-3L Analog input channel (DIFF and Single Ended)
-16	Analog Ground	Analog Ground
-17	CH-3H	CH-3H Analog input channel (DIFF only)
-18	Analog Ground	Analog Ground
-19	CH-4L	CH-4L Analog input channel (DIFF and Single Ended)
-20	Analog Ground	Analog Ground
-21	CH-4H	CH-4H Analog input channel (DIFF only)
-22	Analog Ground	Analog Ground
-23	CH-5L	CH-5L Analog input channel (DIFF and Single Ended)
-24	Analog Ground	Analog Ground
-25	CH-5H	CH-5H Analog input channel (DIFF only)
-26	Analog Ground	Analog Ground
-27	CH-6L	CH-6L Analog input channel (DIFF and Single Ended)
-28	Analog Ground	Analog Ground
-29	CH-6H	CH-6H Analog input channel (DIFF only)
-30	Analog Ground	Analog Ground

Pin No.	Name	Name Function
-31	CH-7L	CH-7L Analog input channel (DIFF and Single Ended)
-32	Analog Ground	Analog Ground
-33	CH-7H	CH-7H Analog input channel (DIFF only)
-34	Analog Ground	Analog Ground
-35	CH-8L	CH-8L Analog input channel (DIFF and Single Ended)
-36	Analog Ground	Analog Ground
-37	CH-8H	CH-8H Analog input channel (DIFF only)
-38	Analog Ground	Analog Ground
-39	Not used	Not used
-40	Not used	Not used
-41	Not used	Not used
-42	Not used	Not used
-43		Analog output to ADCM
-44	Not used	Not used

APPENDIX B: SPECIFICATIONS

GAIN AND ACCURACY

Voltage Gain	+1 or +10
Accuracy	± 0.01% of F.S.
Gain Temp. Coefficient	± 10 PPM/°C

INPUT SPECIFICATIONS

Signal Voltage	± 10 V or ± 1 V
Maximum Source Impedance	1 K ohms
Common Mode Voltage Plus Signal Voltage	± 10 V
Absolute Maximum	± 15 V

"ON" CHANNEL SPECIFICATIONS

Switch Impedance	500 ohms (typical)
Input Impedance	10^9 ohms, 80 pF
Common Mode Rejection	80 dB, 0 to 60 Hz

"OFF" CHANNEL SPECIFICATIONS

Impedance	10^{10} ohms, 4 pF

Note: All switches open when power is turned off.

OUTPUT SPECIFICATIONS

Output Voltage Range	± 10 V
Output Current	100 mA
Output Impedance	20 ohms
Voltage Drift	± 50 μV/°C

DYNAMIC RESPONSE

Frequency Response	Tracking error with F.S. peak-to-peak sine wave applied to a single ON channel. 1K source impedance.
Accuracy of 0.01%	250 Hz
Accuracy of 0.1%	2500 Hz

CROSS TALK

ON Channel 1K to ground	< 1 mV. F.S. peak-to-peak 1 kHz sine wave applied to 15 OFF channels.

SETTLING TIME

To 0.01% of 10 volts	10 microseconds (switching between two channels with dc voltage of +10 V and -10 V on each channel respectively).

DIGITAL OUTPUTS

End of Scan	Low true signal which begins when ADC starts to convert the data for the "Last Channel" of the Multiplexer Sequential Mode, and ends when the ADC starts to convert the next time. Held high when the Multiplexer is in the Random Mode. Fanout 10 logic loads. Maximum capacitive load, 1000 pF.
Control Flip-Flop	R-S flip-flop which is set high true by EXC 03YY, and is reset by EXC 0YY, EXC 01YY, EXC 02YY, or System Clear. Also may be wire-ORed and reset by pulling down the output. 1K pull-up to +5 V. Available fanout, 30 logic loads. Maximum capacitive load 100 pF.

TEMPERATURE RANGE

Specification	0°C to 50°C
Operating	-25°C to 70°C
Storage	-55°C to 100°C

POWER

+5 Vdc ± 5%; 725 mA

± 15 Vdc ± 3%; 15 mA

+22 Vdc ± 5%; 10 mA

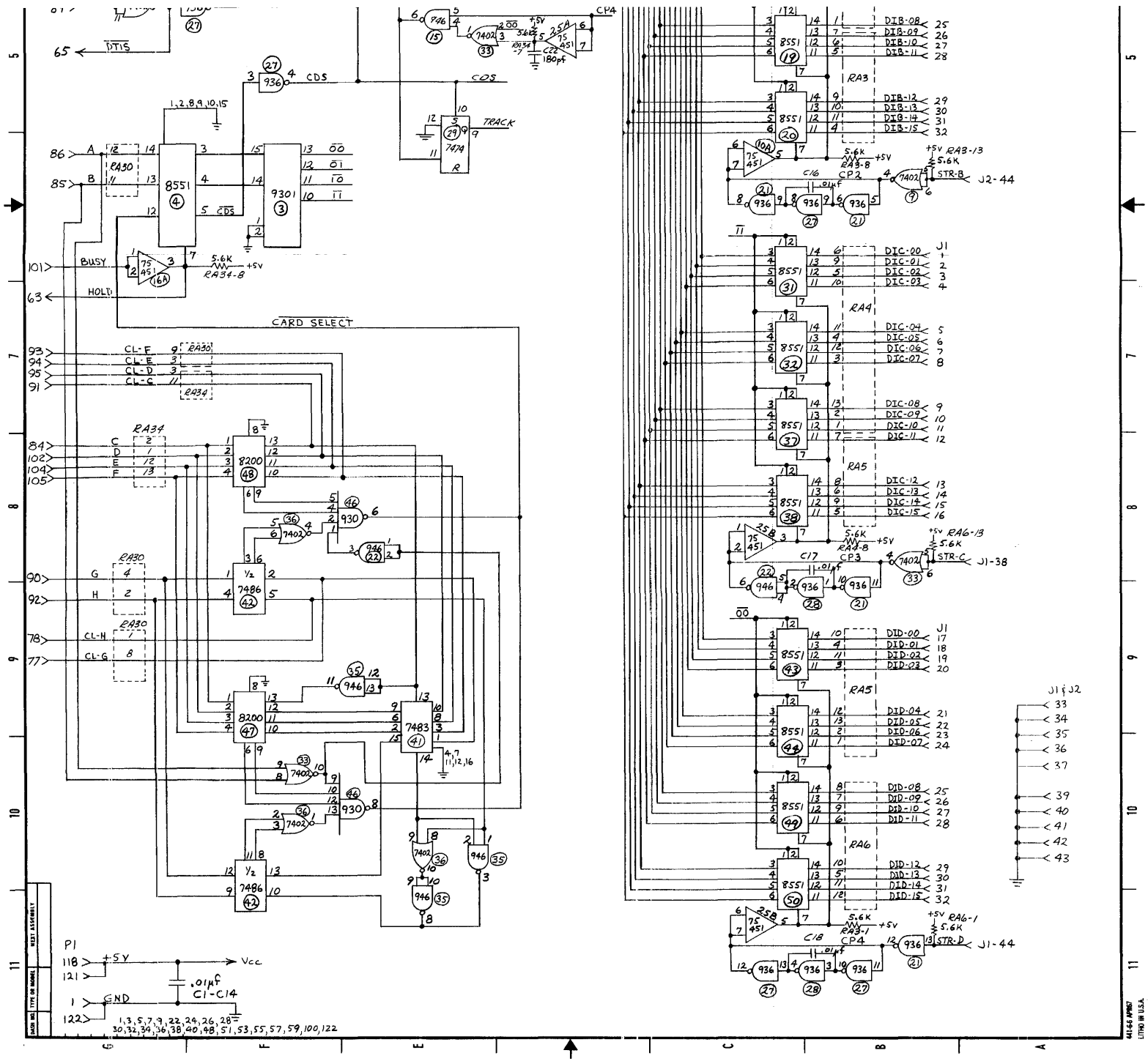
-22 Vdc ± 5%; 5 mA

PHYSICAL CHARACTERISTICS

Dimensions	One printed circuit board 7-3/4 x 12 x 1/2 inches
Connectors	Two 44-terminal card edge connectors One 122-terminal card edge connector

APPENDIX C: SCHEMATICS, ASSEMBLIES, PARTS LIST

Modular Multiplexer	03-950115 (2 Sheets)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CDS
TRACK
CP4
BUSY
HOLD
CARD SELECT
CL-F
CL-E
CL-D
CL-C
CL-H
CL-G
DIB-08
DIB-09
DIB-10
DIB-11
DIB-12
DIB-13
DIB-14
DIB-15
DIC-00
DIC-01
DIC-02
DIC-03
DIC-04
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DID-10
DID-11
DID-12
DID-13
DID-14
DID-15
STR-B
STR-C
STR-D
J1-44
J1-38
J2-44
J1 & J2
P1
+5V
Vcc
GND
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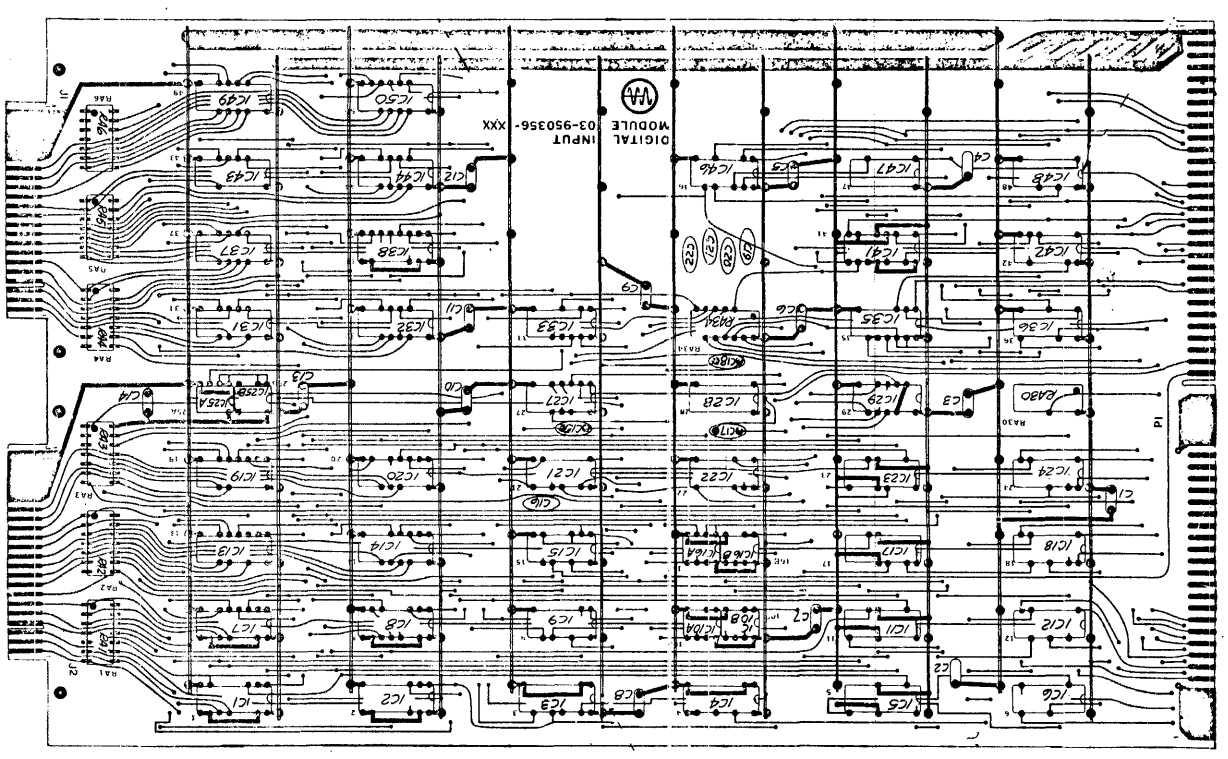
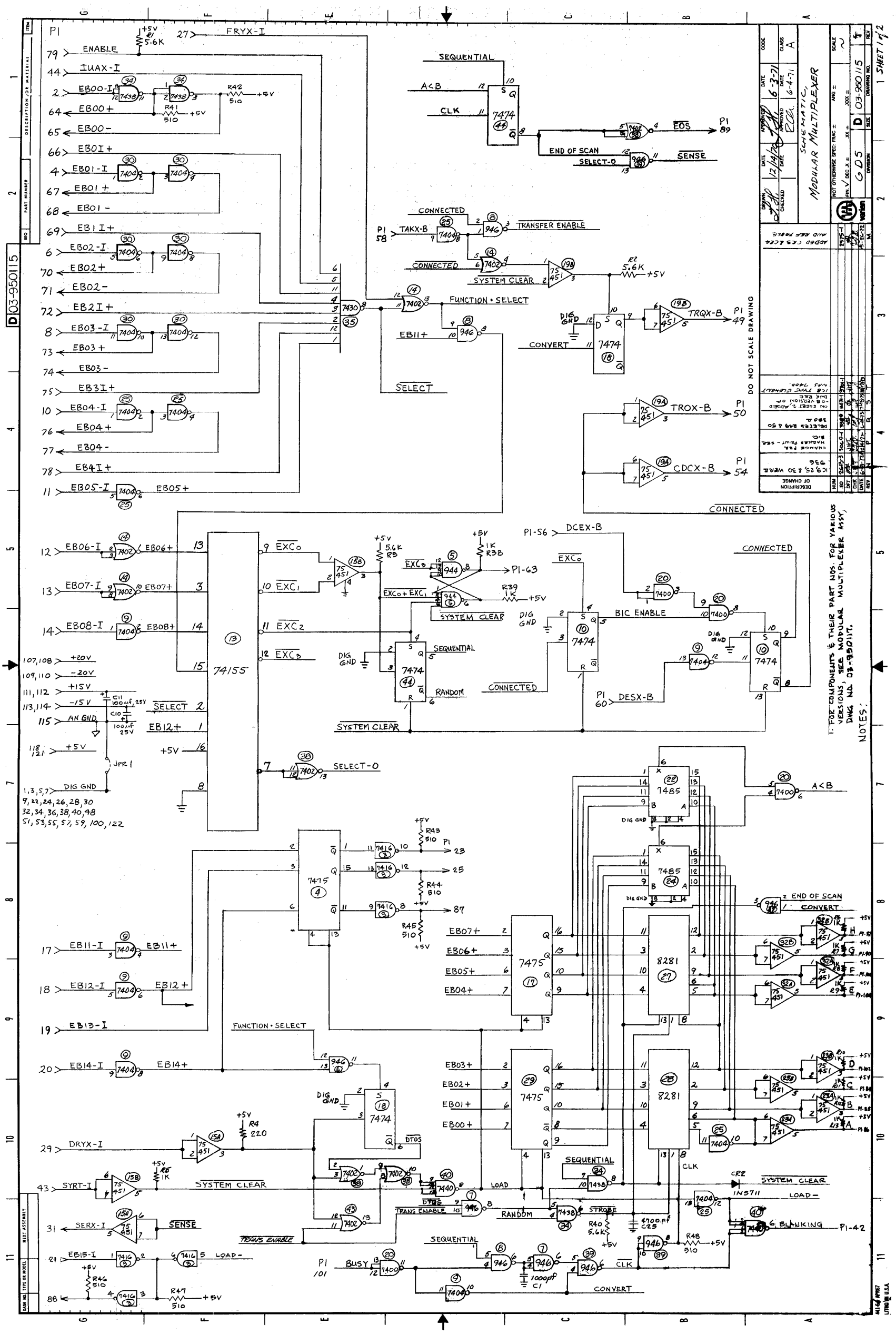

DIGITAL INPUT
MODULE 03-950356-XXX



NOTES:
1. FOR COMPONENTS & THEIR PART NOS. FOR VARIOUS VERSIONS, SEE MODULAR MULTIPLEXER ASSY DWG NO. 03-950117.

DO NOT SCALE DRAWING

D 03-950115

SCHEMATIC, MODULAR MULTIPLEXER

DRAWN CHECKED — DATE 6-3-71 — APPROVED — DATE 6-4-71 — APPROVED — DATE 12/14/72

CODE — CLASS A — SCALE ~ — SIZE D — DRAWING NO. 03-950115 — REV F

NOT OTHERWISE SPEC: FRAC ± — ANG ± — XX ± — XXX ± — DEC. X ± — FIN. √ — DIVISION GDS

SHEET 1 of 2

DESCRIPTION OF CHANGE

ADDED CAS LATCH AND REF TABLE — 5-12-72

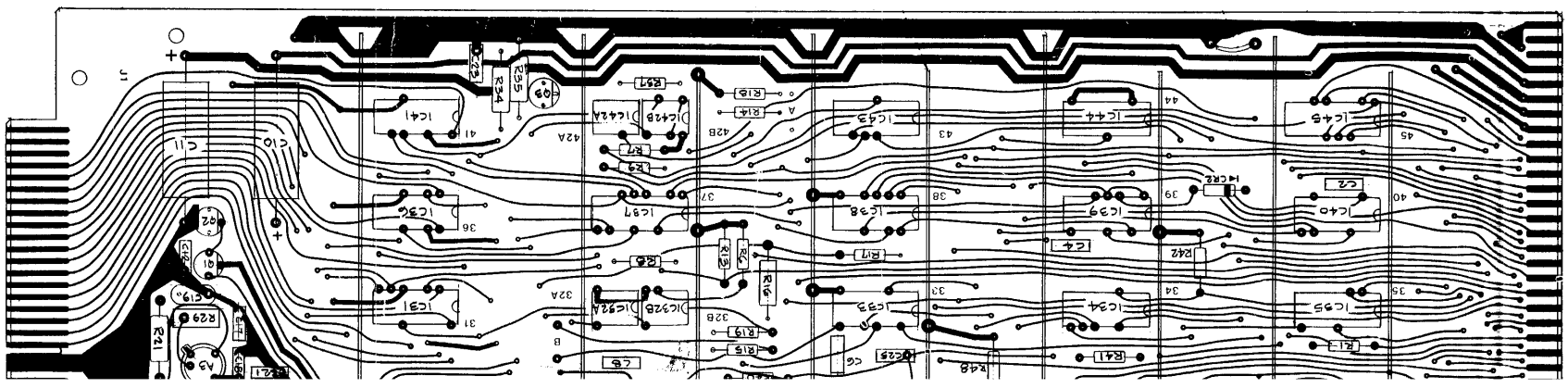
ICs TYPE CLEARLY MAG TAPE.

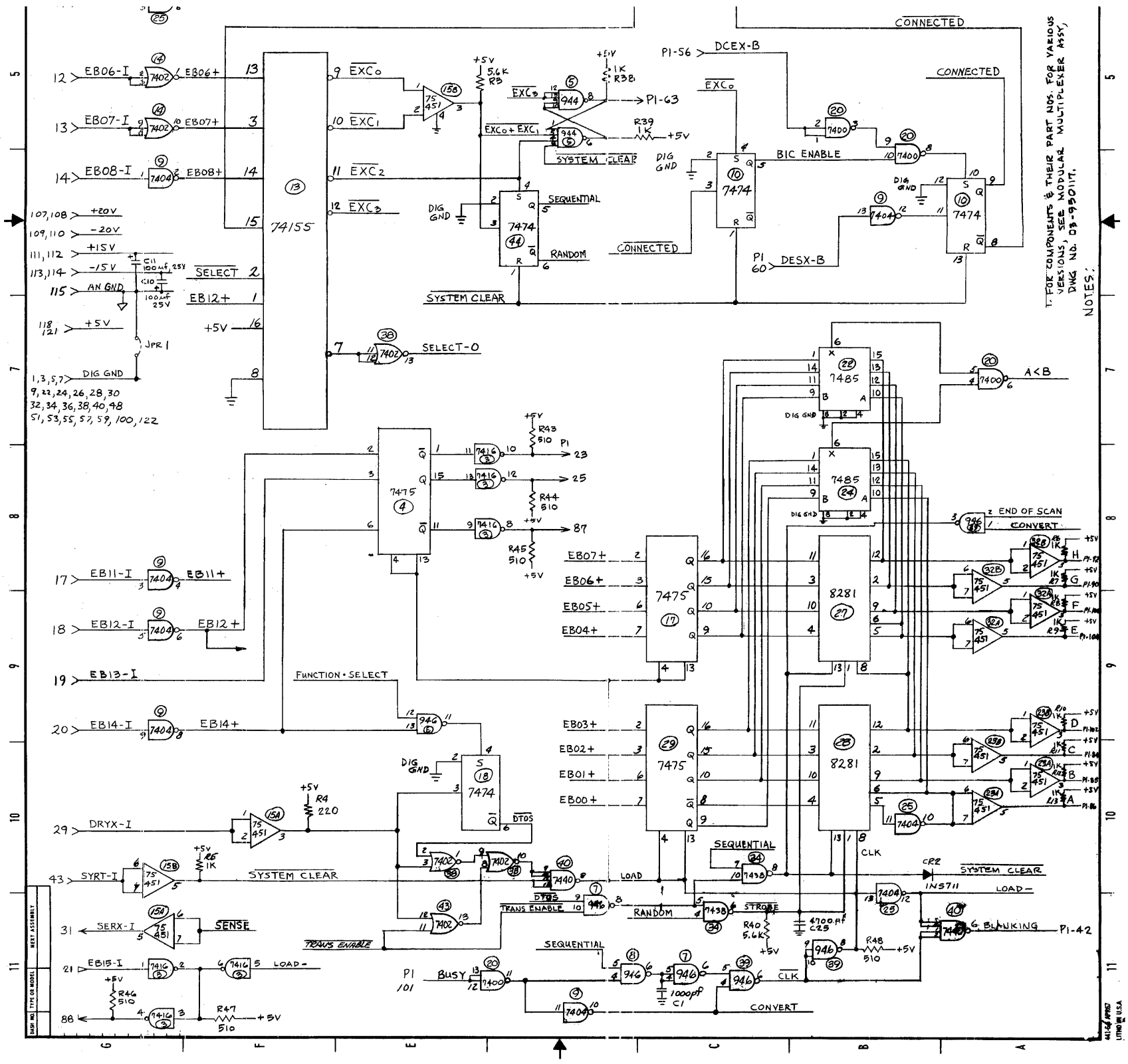
ADDED 2 SHEET 2 DUE TO VERSION OF

DELETED R49 & 50

CHANGE PART - SEE B.O.

ICs 25, 30 WERE 956




NOTES:
1. FOR COMPONENTS & THEIR PART NOS. FOR VARIOUS VERSIONS, SEE MODULAR MULTIPLEXER ASSY, DWG NO. 03-950117.
CONNECTED
P1-56 DCEX-B
P1 60 DESX-B
BIC ENABLE
SYSTEM CLEAR
SEQUENTIAL
RANDOM
SELECT
EB12+
+5V
SELECT-0
DIG GND
+20V
-20V
+15V
-15V
AN GND
+5V
JPR 1
1,3,5,7 DIG GND
9,22,24,26,28,30
32,34,36,38,40,48
51,53,55,57,59,100,122
107,108
109,110
111,112
113,114
115
118,121
74155
7474
7475
7485
8281
7400
7402
7404
7410
7416
7436
7438
7440
946
75451
EB06-I
EB07-I
EB08-I
EB11-I
EB12-I
EB13-I
EB14-I
EB15-I
EB06+
EB07+
EB08+
EB11+
EB12+
EB14+
EXC0
EXC1
EXC2
EXC3
EXC0+EXC1
DRYX-I
SYRT-I
SERX-I
SENSE
TRANS ENABLE
DTOS
LOAD
LOAD-
STROBE
CLK
CONVERT
BUSY
FUNCTION • SELECT
EB07+
EB06+
EB05+
EB04+
EB03+
EB02+
EB01+
EB00+
A<B
END OF SCAN
CONVERT
P1-23
P1-25
P1-87
P1-63
P1-42
P1-102
P1-86
P1-88
P1-100
R4 220
R34 510
R35 510
R43 510
R44 510
R45 510
R46 510
R47 510
R48 510
R40 5.6K
5.6K R3
1K R38
R39 1K
1K R6
C11 100uf 25V
C10 100uf 25V
4700pf C25
1000pf C1
CR2 IN5711
MODULAR MULTIPLEXER 03-950117-XXX

DWG NO REFERENCE	C19	R22,R31	R24,R33
09-950117-01	5 pf	10K 1%	10K 1%
02	↕	↕	↕
03	↕	↕	↕
04	5 pf	10K 1%	10K 1%
05	——	——	——
06	↕	↕	↕
09-950117-07	110 pf	5K .1%	50K .1%
09-950117-08	110 pf	5K .1%	50K .1%

SEE SHT 1

SCHEMATIC, MODULAR MULTIPLEXER

DRAWN	DATE	APPROVED	DATE	CODE
CHECKED	DATE	APPROVED	DATE	CLASS A

REV	DIVISION	SIZE	DRAWING NO.	REV
	GDS	D	03-950115	T

DO NOT SCALE DRAWING

ITEM	DESCRIPTION OR MATERIAL	PART NUMBER	REQ	DATA NO.	TYPE OR MODEL	NEXT ASSEMBLY

03-950115

1 SHEET 2 of 2

44-66 AP467
LITHO IN U.S.A.

Modular Multiplexer, 950117

Schematic Reference	Description	Varian Part No.
Q1	Transistor, 2N3906	62-903 906
Q2, Q3	Transistor, 2N3904	62-903 904
Q4, Q5	Transistor, U1897E	62-798 125
A1	Amplifier, 310H	62-600 212
A2, A3	Amplifier, 2605	62-600 203
A4	Amplifier, NH0002C	62-600 185
C1	Cap, MICA 1000 Pf	41-159 599
C2-9, 12-18, 21-23	Cap, Cer, 1 uf, 50 V	41-228 009
C10, 11	Cap, Elect, 100 μf, 25 V	41-506 258
C19	Cap, MICA 5 pf	41-159 505
C20	Cap, Cer, 51 pf, 500 V	41-205 860
C25	Cap, Cer, 4700 pf, 200 V	41-229 947
IC6, 11, 16, 21, 26, 31, 36, 41	IC Element DG 172	62-600 261
IC9, 25, 30	IC Element 7404N	62-600 013
IC7, 9, 25, 30, 33, 39	IC Element 946	62-600 303
IC35	IC Element 7430 N	62-600 359
IC40	IC Element 7440N	62-600 310
IC5	IC Element 944	62-600 306
IC10, 18, 44	IC Element 7474N	62-600 365
IC4, 17, 29	IC Element 7475	62-600 351
IC22, 24	IC Element 7485	62-600 338
IC27, 28	IC Element 8281	62-600 364
IC12, 37, 45	IC Element 9301	62-600 400
IC13	IC Element 74155	62-600 271
IC14, 38, 43	IC Element 7402N	62-600 356
IC15A&B, IC19A&B, IC23A&B, IC32A&B, IC42A&B	IC Element 75451	62-600 260
IC3	IC Element 7416	62-600 019
JPR1, C, D	Wire, Bus, Bare, #24 Awg	81-099 924
IC34	IC Element 7438	62-600 294
IC8, 20	IC Element 7400	62-600 355
R28	Res, FXD, Comp, 100Ω, $\frac{1}{4}$W, 5%	32-301 310
R14, 19	Res, FXD, Comp, 180Ω, $\frac{1}{4}$W, 5%	32-301 318
R4	Res, FXD, Comp, 220_, $\frac{1}{4}$W, 5%	32-301 322
R5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 38, 39	Res, FXD, Comp, 1 K, $\frac{1}{4}$W, 5%	32-301 410
R1, 2, 3, 15, 18, 37, 40	Res, FXD, Comp, 5.6 K, $\frac{1}{4}$W, 5%	32-301 456
R20	Res, FXD, Comp, 30 K, $\frac{1}{4}$W, 5%	32-301 530
R41-48	Res, FXD Comp, 510Ω, $\frac{1}{4}$W, 5%	32-301 351
R49, R50	Res, FXD Comp, 390Ω, $\frac{1}{4}$W, 5%	32-301 339

Modular Multiplexer, 950117 (Cont'd)

Schematic Reference	Description	Varian Part No.
R21, 26, 30	Res, MF, 3.16 K, $\frac{1}{4}$W, 1%	31-224 316
R26	Res, MF, 6.34 K, $\frac{1}{4}$W, 1%	31-224 634
R34	Res, MF, 10 K, $\frac{1}{4}$W, 1%	31-225 100
R25, 35	Res, Var, W.W. 200Ω	37-577 310
R23, 32	Res, Var, W.W. 1 K	37-577 311
R27	Res, Var, W.W. 50 K	37-577 315
R29	Res, MF 10 K, 1%	31-239 033
R22, 24, 31, 33	Res, MF 750Ω, 1%	31-223 750
R16	Diode, 1N914	66-304 148
CR1, 3, 4	Diode 1N5711	66-981 101
CR2	Terminal	16-229 862
TP1-TP6	Cap, MICA - 110 pf	41-159 564
C19	Res, MF - 50 K, .1%	31-239 064
R24, 33	Res, MF - 5 K, .1%	31-239 011
R22, 31		

USER'S GUIDE

DIGITAL INPUT MODULE

for use with

Varian 620 or V73 Series Computers

Publication No. 03-996 811B

August 1973

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TABLES

FIGURES

1. INTRODUCTION

1.1 GENERAL

The Digital Input Module (DIM) is a hardware option which provides digital inputs to Varian 620 and V73 series computers. The module can be configured in either a mixed analog and digital system or a digital-only system.

The DIM is not a freestanding module; it requires various control functions from other modules. In a digital-only system, the DIM is supplied with abridged versions of the Varian Analog-to-Digital Converter (ADC) and Multiplexer (MUX) modules, which provide the necessary control logic. In a mixed analog and digital system, the DIM utilizes the control functions of standard ADC and MUX modules. An existing analog input system can be easily expanded, therefore, to accommodate both analog and digital inputs.

For details regarding the control functions supplied by the ADC and MUX modules, refer to the ADCM User's Guide (Publication No. 03-996 806) and High-Level Multiplexer User's Guide (Publication No. 03-996 807).

Each DIM provides four 16-bit digital input registers. Expansion to as many as 256 input registers is possible, since up to 64 DIMs can utilize a single pair of control cards.

Simple installation procedures allow the DIM to be installed either at the factory or on-site at the user's facility. A comprehensive software test package is provided with the DIM for post-installation checkout of its operational status. In addition, the module is fully supported by standard Varian software and input/output options.

1.2 FUNCTIONAL DESCRIPTION

Figure 1-1 illustrates the functional elements included in a complete digital input system. These elements are packaged on three plug-in printed circuit boards. Those elements contained on the ADC control card are shown in the dotted portion of the figure; the elements contained on the MUX control card are shown in the diagonally striped portion of the figure; the unshaded area of the figure represents the elements contained on a DIM card.

Device Address

Each DIM requires two device addresses, which are set when the module is installed. The device addresses are used by the computer to select a particular DIM for operation. The addresses are actually assigned to the ADC and MUX cards which control the DIM and through which the DIM is accessed. Typically, the ADC is assigned device address 60 octal, and the MUX is assigned address 61 octal. The MUX contains the device address decode logic.

Channel Selection

DIM channels can be selected in either sequential or random mode via the MUX control card. The mode of channel selection is specified by the computer program using a standard assembly language instruction. In sequential mode, the channel address decode logic on the MUX control card automatically increments from channel address 1 to the final address prescribed by the program. In random mode, the DIM channel address is specified by the program. This mode permits the selection of DIM channels in any sequence.

End-Of-Scan Sense

The program can determine when a sequential channel selection operation is complete by issuing a Sense instruction that selects the End-of-Scan Sense input line

on the MUX control card. This line is logically true when the channel address decode logic selects the final channel address in a sequential operation.

Data Transfer

An internally-generated strobe signal automatically transfers data from the external source to a DIM storage register at 20-microsecond intervals. Optionally, the DIM can be wired to accept an external strobe from the data source.

Data transfers from DIM storage registers to the computer can be performed under program control or under control of the optional Buffer Interlace Controller (BIC). When operating under program control, data transfers are initiated by the computer and are executed under input instruction control. When operating with a BIC, data transfers are initiated by the computer and executed without input instruction control. The BIC permits automatic, high or low speed, block data transfers from the DIM to computer memory without disturbing the sequence of the main program.

Programmable Timer

A programmable timer is contained on the ADC control card. The timer provides a train of pulses in which the interval between pulses is determined by a data word that is loaded into the timer by the computer program. An internal crystal-controlled oscillator provides the time base used by the timer; there is also a provision for an external signal to be used as the time base. With the standard internal oscillator, the timer pulse can be varied between 1 microsecond and 65 milliseconds with a resolution of 1 microsecond. The programmable timer can be especially useful in setting the rate of sampling of input channels.

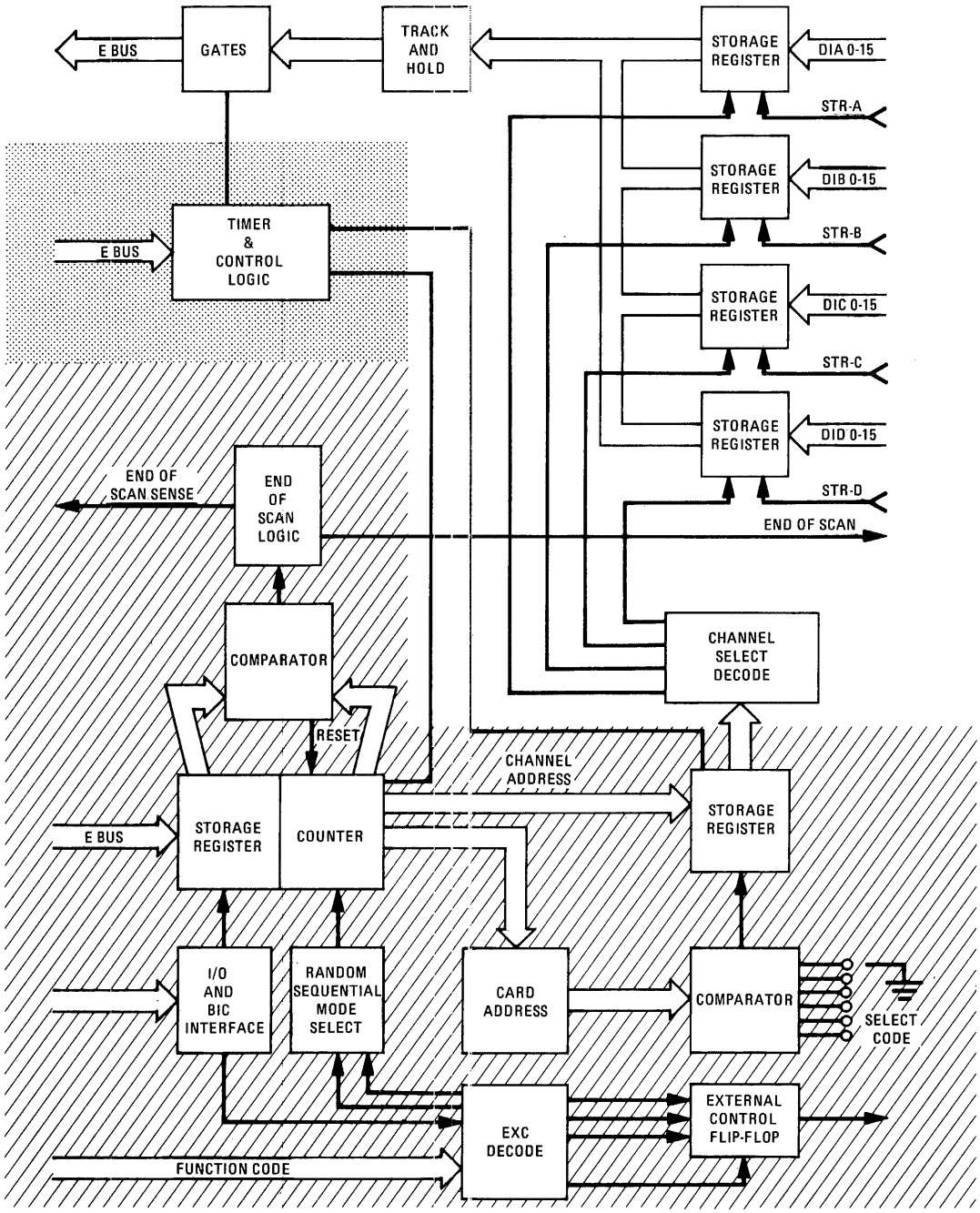


Figure 1-1. Digital Input System Block Diagram

2. PROGRAMMING

2.1 INTRODUCTION

This section describes Assembly Language programming techniques for operating the DIM and presents instructions for using the software test package for module checkout. More detailed programming information may be found in the 620 series and V73 system handbooks.

A program is able to direct DIM operation in the following ways:

- Sets mode of channel selection.
- Outputs channel select codes.
- Tests for end-of-scan in sequential mode.
- Transfers data from digital input registers.
- Sets interval for programmable timer.
- Enables operation under BIC control.

Note that these programmed features deal primarily with the ADC and MUX modules which provide control functions for the DIM. Further information regarding these programmed functions is given in the User's Guides for the ADC and MUX modules. Also the ADC driver programs, which are described in the ADC User's Guide, may be used with the DIM.

Table 2-1 provides a summary of the basic assembly language instruction set used with the DIM.

Table 2-1. DIM Assembly Language Instruction Set

Instruction		Description
EXC	00YY	Connects MUX control module to BIC.
EXC	01YY	Selects Random Scan Mode.
EXC	02YY	Selects Sequential Scan Mode.
SEN	00YY	Senses End of Sequential Scan.
OAR	0YY	Outputs channel select code from the A register.
OBR	0YY	Outputs channel select code from the B register.
OME	0YY	Outputs channel select code from memory.
EXC	00XX	Connects ADC control module to BIC.
EXC	01XX	Starts data input under program control.
EXC	02XX	Enables DIM for start from external pulse or timer pulse.
EXC	03XX	Disables external pulses when starting the DIM under program control.
SEN	00XX	Senses DIM Data Ready.
SEN	01XX	Senses timer interval pulse.
SEN	02XX	Utility sense input. Can be used to sense external start.
OAR	0XX	Outputs timer interval word from register A.
OBR	0XX	Outputs timer interval word from register B.
OME	0XX	Outputs timer interval word from memory.
CIA	0XX	Clears A register and inputs DIM data to A.
CIB	0XX	Clears B register and inputs DIM data to B.
INA	0XX	Inputs DIM data to A register.
INB	0XX	Inputs DIM data to B register.
IME	0XX	Inputs DIM data to memory.

Note: YY is the device address for the MUX control module.
XX is the device address for the ADC control module.

2.2 CHANNEL SELECTION MODE

A program specifies the mode of channel selection with an EXC instruction. Sequential channel selection is specified with an EXC 02YY instruction, where YY is the device address of the MUX control card. Random channel selection is specified with an EXC 01YY instruction.

2.3 CHANNEL SELECT CODE TRANSFER

A program specifies the DIM input channel which is to be selected by means of an eight-bit channel select code. (Channels are numbered from 1 to 256.) This code may be transferred from the computer's A or B register or from memory to the MUX control card by means of a standard data-transfer-out operation. Transfer of the channel select code is accomplished with one of the following instructions:

OAR	0YY	Load device YY from A register
OBR	0YY	Load device YY from B register
OME	0YY	Load device YY from memory

where YY is the device address of the MUX control card.

In sequential mode, only the channel select code for the final channel address is sent to the MUX; all select codes from channel address 1 to the final address are generated automatically once the sequence has begun.

In random mode, each selection of a channel requires a separate data-transfer-out of the appropriate channel select code. The data transfer operation may be under program control or BIC control.

2.4 END-OF-SCAN SENSE

The program can test the status of a sequential channel selection to determine if the final channel has been selected (end-of-scan). It does this by executing SEN 0YY,

where YY is the device address of the MUX control card. A true level on the computer's sense input line, SERX-I, indicates that the DIM has completed its scan. If the computer does not intervene, the DIM will return to channel 1 and continue its scanning sequence.

2.5 BIC ENABLE

The BIC option can be used either to output a block of random channel addresses from memory to the DIM or to input a block of sequential or single-channel readings from the DIM to memory. If it is desirable to perform both of these operations under BIC control, two BICs are required.

The MUX control card is used to output random channel addresses via the BIC. In this case, the program enables the MUX to operate under BIC control by an EXC 0YY instruction, where YY is the MUX control card's device address. This sets the MUX to random mode and establishes the connection to the BIC so that random channel addresses may be passed to the MUX from memory via the BIC.

The ADC control card is used with the BIC to input a block of DIM readings from sequential channels. In this case, an EXC 0XX instruction is used to connect the DIM to the BIC; XX is the device address of the ADC control card.

2.6 TIMER INTERVAL PROGRAMMING

The timer on the ADC control card may be programmed to provide a single pulse after a predefined delay or a train of pulses at a predefined frequency. This is accomplished by outputting the desired pulse interval value to the timer register.

The defined value for the pulse interval is transmitted from the computer to the timer register as a 16-bit number (less than or equal to 65535_{10}). The timer decrements this number at the rate of one count per miscrosecond and issues an output pulse when the count reaches zero. In continuous mode, the timer auto-

matically reloads to the value in the buffer register and begins a new cycle. In single cycle mode, the next cycle must be initiated by an external signal. The timer mode is prewired to user specifications, but may be changed after installation.

The pulse interval may be loaded into the timer buffer register either directly from memory or via the computer's input/output registers. One of three statements is used to load the timer buffer register:

OAR	0XX	Output value from A Register to buffer register
OBR	0XX	Output value from B Register to buffer register
OME	0XX	Output value from memory to buffer register

where XX is the ADC control card's device address.

The status of the timer can be sensed by issuing a SEN 01XX instruction. A true sense response on Sense line 1 indicates that the timer has decremented to zero; a false level indicates that it has not. The timer continues operation whether or not the sense line is sampled. The line is automatically reset to false as soon as it has been sensed true.

2.7 DATA TRANSFER

Data is transferred from the DIM input registers to the computer using any of the standard input instructions INA, INB, CIA, CIB, or IME. Data is read from ADC device address (0XX). Note that in a combined analog and digital system, all data is received from the ADC device address.

2.8 PROGRAMMING EXAMPLES

The following examples illustrate typical sequences of program instructions which may be used to direct DIM operation. The examples assume device address 60 octal

for the ADC control card and device address 61 octal for the MUX control card.

Example 1 - Random Selection Under Program Control

In this example, a set of random channel numbers is used to select DIM channels. The channel numbers are transferred from an array in memory, and the resulting input values from the selected channels are stored in another array in memory. Note that a Sense instruction is used to check for data ready before reading each input channel. This is necessary since the hardware requires approximately 20 microseconds to advance to a new random channel, and this delay is not provided by the program code.

```
        LDB     INPT    Load First Word Address of Input Data Array.
        LDX     CHAN    Load First Word Address Channel Number
                        Array.
        EXC     0360    Lock Out External Start on DIM.
        EXC     0161    Select Random Mode.
        CIA     060     Clear Data Ready Flag.
RAN1    LDA     0,1     Load First Channel Number.
        OAR     061     Output Channel Number to DIM.
        EXC     0160    Request Input.
LOOP    SEN     060,READ Check if Data Ready.
        NOP
        JMP     LOOP    Not Ready.
READ    CIA     060     Read Input Data.
        STA     0,2     Store Data in Array.
        IBR
        IXR
        TXA             } Check If All Values Have Been Read.
        SUB     WRDS
        SUB     CHAN
```

```
         JAN     RAN1
         HLT
CHAN     DATA    xxx     First Word Address of Channel Number
                         Array.
INPT     DATA    xxx     First Word Address of Input Data Array.
WRDS     DATA    xxx     Number of Data Words.
```

Example 2 - Sequential Selection Under Program Control

In this example, DIM input channels are selected sequentially from channel 1 to the channel number specified by the program. The input values are stored in an array in memory, and the scan is terminated when the desired number of values have been read.

```
         LDX     INPT    Load First Word Address of Input Array.
         EXC     0360    Lock Out External Starts.
         EXC     0261    Select Sequential Mode.
         CIA     060     Clear Data Ready Flag.
         LDA     LAST    Load Last Channel Number.
         OAR     061     Output Last Channel Number.
SEQ1     EXC     0160    Request Input from Channel.
LOOP     SEN     060,READ Check if Data Ready.
         NOP
         JMP     LOOP    Not Ready.
READ     CIA     060     Read Input Data.
         STA     0,1     Store Data in Array.
         IXR             \
         TXA             |
         SUB     WRDS    | Check If All Values Have Been Read.
         SUB     INPT    |
         JAN     SEQ1    /
```

```
        HLT
INPT    DATA    xxx     First Word Address Of Input Data Array.
WRDS    DATA    xxx     Number of Data Words.
LAST    DATA    xxx     Last Channel Number.
```

2.9 DIM TEST PROGRAMS

A set of test programs is provided for checkout of the DIM and its ADC and MUX control cards. Four of these programs, which test the ADC and MUX control cards, are described in the ADC User's Guide. These test programs are numbered 1, 2, 3, and 6. An additional test program, number 7, is designed specifically for DIM checkout. Test 7 is described in this manual.

Program loading and selection procedures, as well as sense switch conventions, are described in the ADC User's Guide.

Test 7 -- Digital Input Test

This test is designed to check out one DIM card in both random and sequential modes. The test requires the installation of a special test shoe, which can be purchased from Varian (Part No. 03-950329). The test shoe provides a known 16-bit word as input to two of the DIM registers, while the other two registers not currently on the test shoe will be unaffected and will read the last strobed-in value. A three-position toggle switch on test shoe gives the ones complement of the output to each of the two registers as shown in Table 2-2.

Table 2-2. DIM Test Shoe Output

Channel Number	J1			J2		
	Switch Setting			Switch Setting		
	A	Off	B	A	Off	B
1 + 4n	N/A	N/A	N/A	0114631	N/A	0063146
2 + 4n	N/A	N/A	N/A	0063146	N/A	0114631
3 + 4n	0114631	0	0063146	N/A	0	N/A
4 + 4n	0063146	0	0114631	N/A	0	N/A
Where, n = integer 0 to 63						

The test exercises each column in the table in both sequential and random modes.

After the test is selected, the program prints:

```
DIM TEST
ENTER CHANNEL NO?
```

In response to this message, the user should enter the first channel number of the DIM card being tested. The channel number must be the value (1 + 4n) where n is an integer from 0 to 63; otherwise, the program will request the number again.

After the channel has been selected, the test program issues a series of requests to place the test shoe on J1 and J2 and to set the test shoe switch to position A or B. After complying with each request, the user types a period to initiate the test.

Note that it is important to set the test shoe toggle switch to OFF prior to removing the test shoe from J1 or J2. This causes the associated registers to be cleared.

The program checks the sequential mode of operation by reading all channels sequentially, beginning with channel number 1. The program first checks all channels

except the block of four for which the test has been requested to insure that neither test pattern is present on any channel. If either of these readings is found, the program prints the channel number and reading.

The program then checks the block of four channels requested by the user. Each is read and the input data is checked according the appropriate column of Table 2-2. If any error is detected, all four channel numbers and readings are printed.

After the sequential test, the program checks the random mode of operation. In this check, the four channels of interest are read and compared against the appropriate column of the table. If any error is detected, all four channel numbers and readings are printed.

If no errors are found in either the sequential or random check, "OK" is printed, and the test is repeated for the next column in the table. All four A/B columns of the table are tested in sequence and then control is returned to the test selection statement.

If sense switch 2 is set, the test will loop on the same column after a period is entered following the test shoe connection request.

3. THEORY OF OPERATION

3.1 GENERAL SYSTEM DESCRIPTION

The Digital Input Module operates in close conjunction with the ADC module. From the computer's standpoint, multiplexer channels are selected and 16-bit data words are acquired with no distinction as to whether a given channel contains analog or digital raw data.

If the DIM determines that one of its own channels is selected when a data input sequence begins at the ADC device address, it prevents the ADC from gating data to the E-bus and substitutes its own 16-bit data word to the E-bus. Therefore, if CDS is true (H) at device 29 pin 4, when ENABLE goes true (L→H) it clocks flip-flop 29 pin 5 (L) which forces ENABLE false (L) at P1 pin 83. ENABLE must be true (H) for ADC data to be gated to the E-bus. A zero level (L) at pin 11 of devices 6, 12, 18, and 24 gates the 16-bit data word of the selected DIM channel to the E-bus.

The CARD SELECT logic designed to compare the 6-bit code composed of signals C, D, E, F, G, and H (defined as "variable") with the 6-bit code composed of signals CL-C, CL-D, CL-E, CL-F, CL-G, and CL-H (defined as "fixed").

CARD SELECT is true (1) if either A or B is true and the variable code is the same as the fixed code, or (2) if both A and B are false and the variable code is one count greater than the fixed code.

When the Multiplexer module is operated in sequential mode, the "variable" channel address code changes each time the ADC BUSY signal goes true. In analog systems the signal information of the previous channel is retained for the ADC by the sample and hold circuit. Similarly, the DIM holds the A, B, and CARD SELECT signals with device 4 (see schematic 03-950354).

The DIM also contains a storage register (devices 5, 11, 17, and 23) which holds the 16-bit data word steady and unchanged while the data is gated to the computer E-bus. For example, if CP1 should occur just prior to DTIS, the TRACK signal would remain true and the computer would receive the 16-bits entered by that CP1 (L→H) transition. If CP1 should occur during DTIS, the TRACK signal would have already been clocked false by the leading edge of DTIS and the computer would receive the 16-bits entered by the last CP1 that occurred just prior to DTIS.

3.2 INPUT MODULE DESCRIPTION

Each DIM register is composed of four identical input devices. This basic input device (see Figure 3-1) provides four D-type flip-flops which operate synchronously from a common clock.

A three-state output facilitates usage of the device in a bus-organized system. The outputs can be wired directly to outputs of other devices without encountering the problems normally met with "collector-ORing" TTL circuits. This is accomplished by gating the normally low impedance logical "1" or logical "0" output into a high impedance state.

The high impedance state occurs on all outputs of all devices except the four outputs of the device selected. The result is that the selected device has a normal TTL low impedance output providing good capacitive drive capability and waveform integrity, especially during the transition from a logical "0" to logical "1". The other outputs are all in the "third-state" and take only a small amount of leakage current from the driving outputs.

The following logic levels control the device:

- Clocking occurs on the positive-going transistion.
- Clearing is enabled by taking the input to a logical "1" level.
- Outputs are placed in the "third-state" if either of the two Output Disable inputs is taken to a logical "1" level.

- If either of the two Data Input Disable inputs is a logical "1" level, the flip-flops will remain in their previous state when clocked.

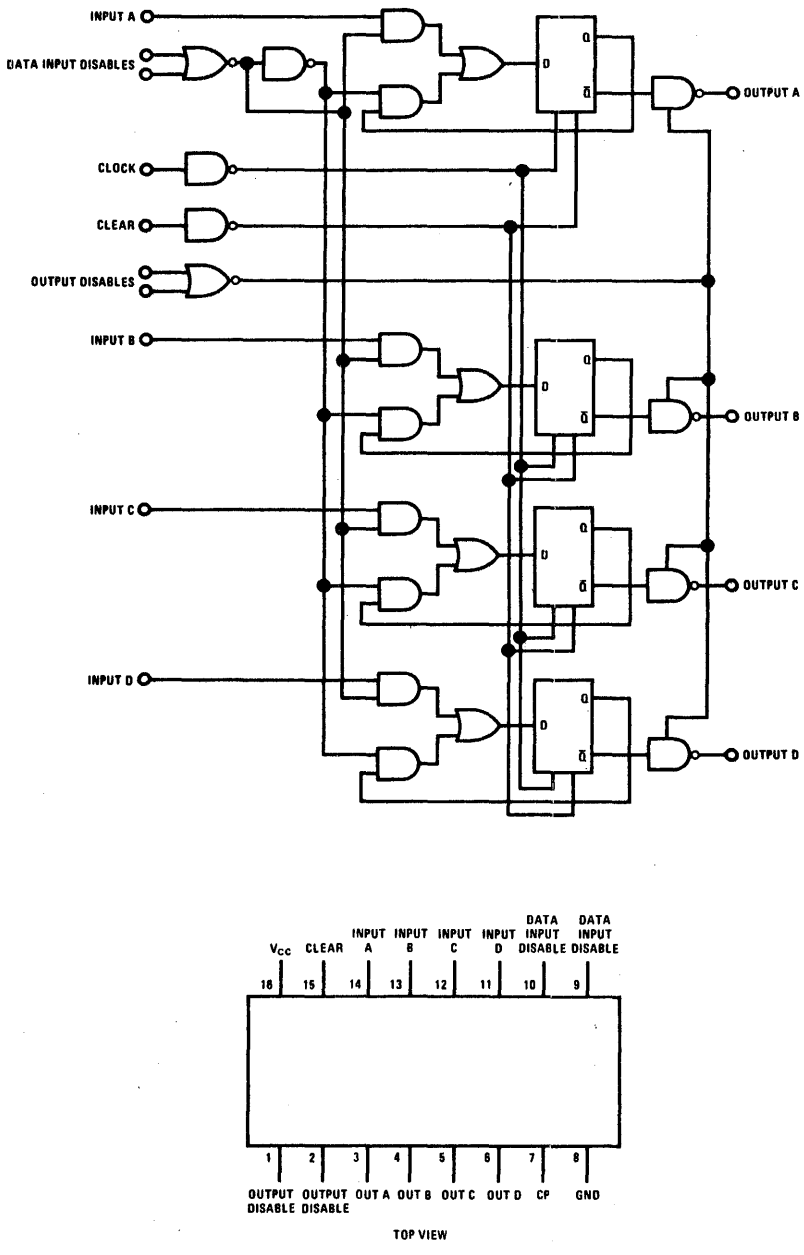


Figure 3-1. Input Device Functional Diagram

4. INSTALLATION

4.1 PREREQUISTIES

Each DIM requires one card slot in either the mainframe or Memory Expansion/ Peripheral Controller frame. The ADC and MUX control cards each require an additional card slot. No special slots are reserved for these cards, and their location in the frame is determined solely by considerations of convenience in backplane wiring.

For additional information on installation of the ADC and MUX cards, refer to the User's Guides for those modules.

4.2 INSTALLATION AND INTERCONNECTION

A DIM is installed vertically with its component side to the left in 620/i and 620/L computers, and horizontally with its component side up in the 620/f computer. The card is installed with the double pin edge pointing toward the installer.

Figure 4-1 illustrates a typical digital input installation, including a DIM with ADC and MUX control cards. Note that in a mixed analog and digital system, an analog power supply would also be required.

Connection to the computer I/O bus and the BIC option B-bus is provided through backplane wiring. Pin assignments for the I/O bus and B-bus are listed in the appendices of the ADC and MUX User's Guides.

Device Address Wiring

In a standard configuration, the DIM's ADC control card is assigned device address 60_8 and the MUX control card is assigned device address 61_8. The jumper connections

for wiring these addresses are listed in Table 4-1.

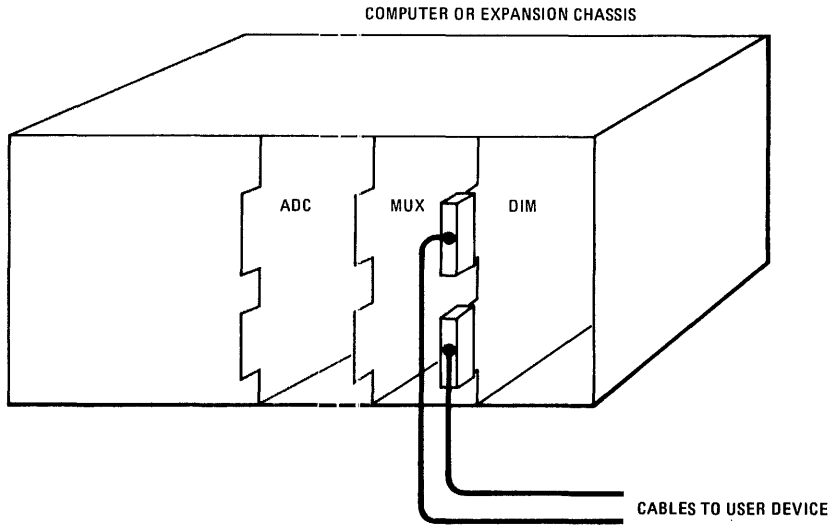


Figure 4-1. Typical Module Installation

Table 4-1. ADC And MUX Device Address Wiring

Signal Name	ADC to ADC		MUX to MUX	
EB-0	P1-65	P1-66		
EB-1	P1-68	P1-69		
EB-2	P1-71	P1-72		
EB-0			P1-64	P1-66
EB-1			P1-68	P1-69
EB-2			P1-71	P1-72
EB-3			P1-74	P1-75
EB-4			P1-76	P1-78

Card/Channel Selection Wiring

Tables 4-2 through 4-4 list the jumper connections required for preparing the MUX control card and DIM modules for card and channel selection.

Table 4-2 lists the daisy chain wirewrap connections for attaching multiple DIM cards to the MUX control card.

Table 4-2. Daisy Chain Wirewrap Connections for MUX And DIM Modules

Signal	MUX to DIM1	to . . .	to DIMn
Blanking	P1-42	P1-42	P1-42
Chan Sel-A	P1-86	P1-86	P1-86
Chan Sel-B	P1-85	P1-85	P1-85
Chan Sel-C	P1-84	P1-84	P1-84
Chan Sel-D	P1-102	P1-102	P1-102
Card Sel-E	P1-104	P1-104	P1-104
Card Sel-F	P1-105	P1-105	P1-105
Card Sel-G	P1-90	P1-90	P1-90
Card Sel-H*	P1-92	P1-92	P1-92

*Card Sel-H must be inverted to operate modules with channel addresses above 128.

Signal	(Any slot below chan 129) to	(Any slot above chan 128) to	(Any slot above chan 128)
Card Sel-H	P1-92	P1-83	P1-83
H-Inverted		P1-94 to P1-92	P1-94 to P1-92

Table 4-3 lists the connections required for the ADC, MUX, and first DIM card to provide operation of channels 1 through 4.

Table 4-3. Jumper Connections for Channel Group 1-4

Signal	From ADC	To MUX	To DIM
ENABLE	P1-83		P1-83
DTIS	P1-89		P1-89
BUSY	P1-75	P1-101	P1-101
A		P1-86	P1-86
B		P1-85	P1-85
C		P1-84	P1-84
D		P1-102	P1-102
E		P1-104	P1-104
F		P1-105	P1-105
G		P1-90	P1-90
H		P1-92	P1-92
CL-F			P1-93
CL-E			P1-94
CL-D			P1-95
CL-C			P1-91
CL-H			P1-78
CL-G			P1-77

Table 4-4 lists the internal connections for wiring each DIM channel address group.

Table 4-4. Wirewrap Jumpers for DIM Channel Address Groups

Channel Group	P1-78 CL-H	P1-77 CL-G	P1-93 CL-F	P1-94 CL-E	P1-95 CL-D	P1-91 CL-C
5-8	x	x	x	x	x	
9-12	x	x	x	x		x
13-16	x	x	x	x		
17-20	x	x	x		x	x
21-24	x	x	x		x	
25-28	x	x	x			x
29-32	x	x	x			
33-36	x	x		x	x	x
37-40	x	x		x	x	
41-44	x	x		x		x
45-48	x	x		x		
49-52	x	x			x	x
53-56	x	x			x	
57-60	x	x				x
61-64	x	x				
65-68	x		x	x	x	x
69-72	x		x	x	x	
73-76	x		x	x		x
77-80	x		x	x		
81-84	x		x		x	x
85-88	x		x		x	
89-92	x		x			x
93-96	x		x			
97-100	x			x	x	x
101-104	x			x	x	
105-108	x			x		x
109-112	x			x		

X indicates ground connection

Table 4-4. (Continued)

Channel Group	P1-78 CL-H	P1-77 CL-G	P1-93 CL-F	P1-94 CL-E	P1-95 CL-D	P1-91 CL-C
113-116	x				x	x
117-120	x				x	
121-124	x					x
125-128	x					
129-132		x	x	x	x	x
133-136		x	x	x	x	
137-140		x	x	x		x
141-144		x	x	x		
145-148		x	x		x	x
149-152		x	x		x	
153-156		x	x			x
157-160		x	x			
161-164		x		x	x	x
165-168		x		x	x	
169-172		x		x		x
173-176		x		x		
177-180		x			x	x
181-184		x			x	
185-188		x				x
189-192		x				
193-196			x	x	x	x
197-200			x	x	x	
201-204			x	x		x
205-208			x	x		
209-212			x		x	x
213-216			x		x	

X indicates ground connection.

Table 4-4. (Continued)

Channel Group	P1-78 CL-H	P1-77 CL-G	P1-93 CL-F	P1-94 CL-E	P1-95 CL-D	P1-91 CL-C
217-220			x			x
221-224			x			
225-228				x	x	x
229-232				x	x	
233-236				x		x
237-240				x		
241-244					x	x
245-248					x	
249-252						x
253-256						

X indicates ground connection.

APPENDIX A: DIM PIN ASSIGNMENTS

Backplane Wiring

Pin No.	Name	Function
P1- 1	Digital Ground	
2	EB00-I	
3	Digital Ground	
4	EB01-I	
5	Digital Ground	
6	EB02-I	
7	Digital Ground	
8	EB03-I	
9	Digital Ground	
10	EB04-I	
11	EB05-I	
12	EB06-I	
13	EB07-I	
14	EB08-I	
15	EB09-I	
16	EB10-I	
17	EB11-I	
18	EB12-I	
19	EB13-I	
20	EB14-I	
21	EB15-I	
22	Digital Ground	
23	Not used	
24	Digital Ground	
25	Not used	
26	Digital Ground	
27	Not used	
28	Digital Ground	
29	Not used	
30	Digital Ground	
31	Not used	
32	Digital Ground	
33	Not used	
34	Digital Ground	
35	Not used	
36	Digital Ground	

Pin No.	Name	Function
P1-37	Not used	
38	Digital Ground	
39	Not used	
40	Digital Ground	
41	Not used	
42	Not used	
43	Not used	
44	Not used	
45	Not used	
46	Not used	
47	Not used	
48	Digital Ground	
49	Not used	
50	Not used	
51	Digital Ground	
52	Not used	
53	Digital Ground	
54	Not used	
55	Digital Ground	
56	Not used	
57	Digital Ground	
58	Not used	
59	Digital Ground	
60	Not used	
61	Not used	
62	Not used	
63	Not used	
64	Not used	
65	Not used	
66	Not used	
67	Not used	
68	Not used	
69	Not used	
70	Not used	
71	Not used	
72	Not used	
73	Not used	
74	Not used	
75	Not used	
76	Not used	
77	Ground Connect	Channel selection for group (N+1) through (N+4) (see Table 4-4)

Pin No.	Name	Function
P1-78	Ground Connect	Channel selection for group (N+1) through (N+4) (see Table 4-4)
79	Not used	
80	Not used	
81	Not used	
82	Not used	
83	Not used	
84	C	Jumper connection for wiring channel select code
85	B	Jumper connection for wiring channel select code
86	A	Jumper connection for wiring channel select code
87	Not used	
88	Not used	
89	Not used	
90	G	Jumper connection for wiring channel select code
91	Ground Connect	Channel selection for group (N+1) through (N+4) (see Table 4-4)
92	H	Jumper connection for wiring channel select code
93	Ground Connect	Channel selection for group (N+1) through (N+4) (see Table 4-4)
94	Ground Connect	Channel selection for group (N+1) through (N+4) (see Table 4-4)
95	Ground Connect	Channel selection for group (N+1) through (N+4) (see Table 4-4)
96	Not used	
97	Not used	
98	Not used	
99	Not used	
100	Digital Ground	
101	Busy	Busy input from ADC Control Card
102	D	Jumper connection for wiring channel select code
103	Not used	
104	E	Jumper connection for wiring channel select code
105	F	Jumper connection for wiring channel select code
106	Not used	
107	Not used	
108	Not used	
109	Not used	
110	Not used	
111	Not used	
112	Not used	
113	Not used	
114	Not used	
115	Not used	

Pin No.	Name	Function
P1 -116	Not used	
117	Not used	
118	+5 V	
119	Not used	
120	Not used	
121	+5 V	
122	Digital Ground	

Terminal Edge Connector Wiring

Pin No.	Name	Function
J1-1	DIC-00	Input word Channel N+1, bit 1
2	DIC-01	Input word Channel N+1, bit 2
3	DIC-02	Input word Channel N+1, bit 3
4	DIC-03	Input word Channel N+1, bit 4
5	DIC-04	Input word Channel N+1, bit 5
6	DIC-05	Input word Channel N+1, bit 6
7	DIC-06	Input word Channel N+1, bit 7
8	DIC-07	Input word channel N+1, bit 8
9	DIC-08	Input word Channel N+1, bit 9
10	DIC-09	Input word Channel N+1, bit 10
11	DIC-10	Input word Channel N+1, bit 11
12	DIC-11	Input word Channel N+1, bit 12
13	DIC-12	Input word Channel N+1, bit 13
14	DIC-13	Input word Channel N+1, bit 14
15	DIC-14	Input word Channel N+1, bit 15
16	DIC-15	Input word Channel N+1, bit 16
17	DID-00	Input word Channel N+2, bit 1
18	DID-01	Input word Channel N+2, bit 2
19	DID-02	Input word Channel N+2, bit 3
20	DID-03	Input word Channel N+2, bit 4
21	DID-04	Input word Channel N+2, bit 5
22	DID-05	Input word Channel N+2, bit 6
23	DID-06	Input word Channel N+2, bit 7
24	DID-07	Input word Channel N+2, bit 8
25	DID-08	Input word Channel N+2, bit 9
26	DID-09	Input word Channel N+2, bit 10
27	DID-10	Input word Channel N+2, bit 11
28	DID-11	Input word Channel N+2, bit 12
29	DID-12	Input word Channel N+2, bit 13

Pin No.	Name	Function
J 1-30	DID-13	Input word Channel N+2, bit 14
31	DID-14	Input word Channel N+2, bit 15
32	DID-15	Input word Channel N+2, bit 16
33	Digital Ground	
34	Digital Ground	
35	Digital Ground	
36	Digital Ground	
37	Digital Ground	
38	STR-C	External strobe for Channel N+1 (or Ground Connect)
39	Digital Ground	
40	Digital Ground	
41	Digital Ground	
42	Digital Ground	
43	Digital Ground	
44	STR-D	External strobe for Channel N+2 (or Ground Connect)
J 2-1	DIA-00	Input word Channel N+3, bit 1
2	DIA-01	Input word Channel N+3, bit 2
3	DIA-02	Input word Channel N+3, bit 3
4	DIA-03	Input word Channel N+3, bit 4
5	DIA-04	Input word Channel N+3, bit 5
6	DIA-05	Input word Channel N+3, bit 6
7	DIA-06	Input word Channel N+3, bit 7
8	DIA-07	Input word Channel N+3, bit 8
9	DIA-08	Input word Channel N+3, bit 9
10	DIA-09	Input word Channel N+3, bit 10
11	DIA-10	Input word Channel N+3, bit 11
12	DIA-11	Input word Channel N+3, bit 12
13	DIA-12	Input word Channel N+3, bit 13
14	DIA-13	Input word Channel N+3, bit 14
15	DIA-14	Input word Channel N+3, bit 15
16	DIA-15	Input word Channel N+3, bit 16
17	DIB-00	Input word Channel N+4, bit 1
18	DIB-01	Input word Channel N+4, bit 2
19	DIB-02	Input word Channel N+4, bit 3
20	DIB-03	Input word Channel N+4, bit 4
21	DIB-04	Input word Channel N+4, bit 5
22	DIB-05	Input word Channel N+4, bit 6
23	DIB-06	Input word Channel N+4, bit 7
24	DIB-07	Input word Channel N+4, bit 8
25	DIB-08	Input word Channel N+4, bit 9
26	DIB-09	Input word Channel N+4, bit 10

Pin No.	Name	Function
J2-27	DIB-10	Input word Channel N+4, bit 11
28	DIB-11	Input word Channel N+4, bit 12
29	DIB-12	Input word Channel N+4, bit 13
30	DIB-13	Input word Channel N+4, bit 14
31	DIB-14	Input word Channel N+4, bit 15
32	DIB-15	Input word Channel N+4, bit 16
33	Digital Ground	
34	Digital Ground	
35	Digital Ground	
36	Digital Ground	
37	Digital Ground	
38	STR-A	External strobe for Channel N+3 (or Ground Connect)
39	Digital Ground	
40	Digital Ground	
41	Digital Ground	
42	Digital Ground	
43	Digital Ground	
44	STR-B	External strobe for Channel N+4 (or Ground Connect)

APPENDIX B: SPECIFICATIONS

DIGITAL INPUTS

Number	Four 16-bit registers.
Type	Low true; 1 TTL logic load plus 5.6 K ohms to +5 Vdc. Logic "1" Input = 0.0 to +0.8 Volts. Logic "0" Input = +2.0 to +5.0 Volts. Input Data Setup Time $\geq$ 0 nsec before (H$\rightarrow$L) strobe. Input Data Hold Time $\geq$ 100 nsec after (H$\rightarrow$L) strobe.

STROBE INPUTS

Number	Four
Type	One logic load plus 5.6 K ohms to +5 Vdc. Data is clocked into one input storage register on the high to low transition of its strobe signal. Data remains fixed as long as the strobe signal is high. If the strobe remains low for more than 20 microseconds, new data is automatically clocked into the storage register at 20 microsecond intervals.

TEMPERATURE RANGE

Specification	0^{o}	to	50^{o} C
Operating	-10^{o}	to	70^{o} C
Storage	-55^{o}	to	85^{o} C

PHYSICAL CHARACTERISTICS

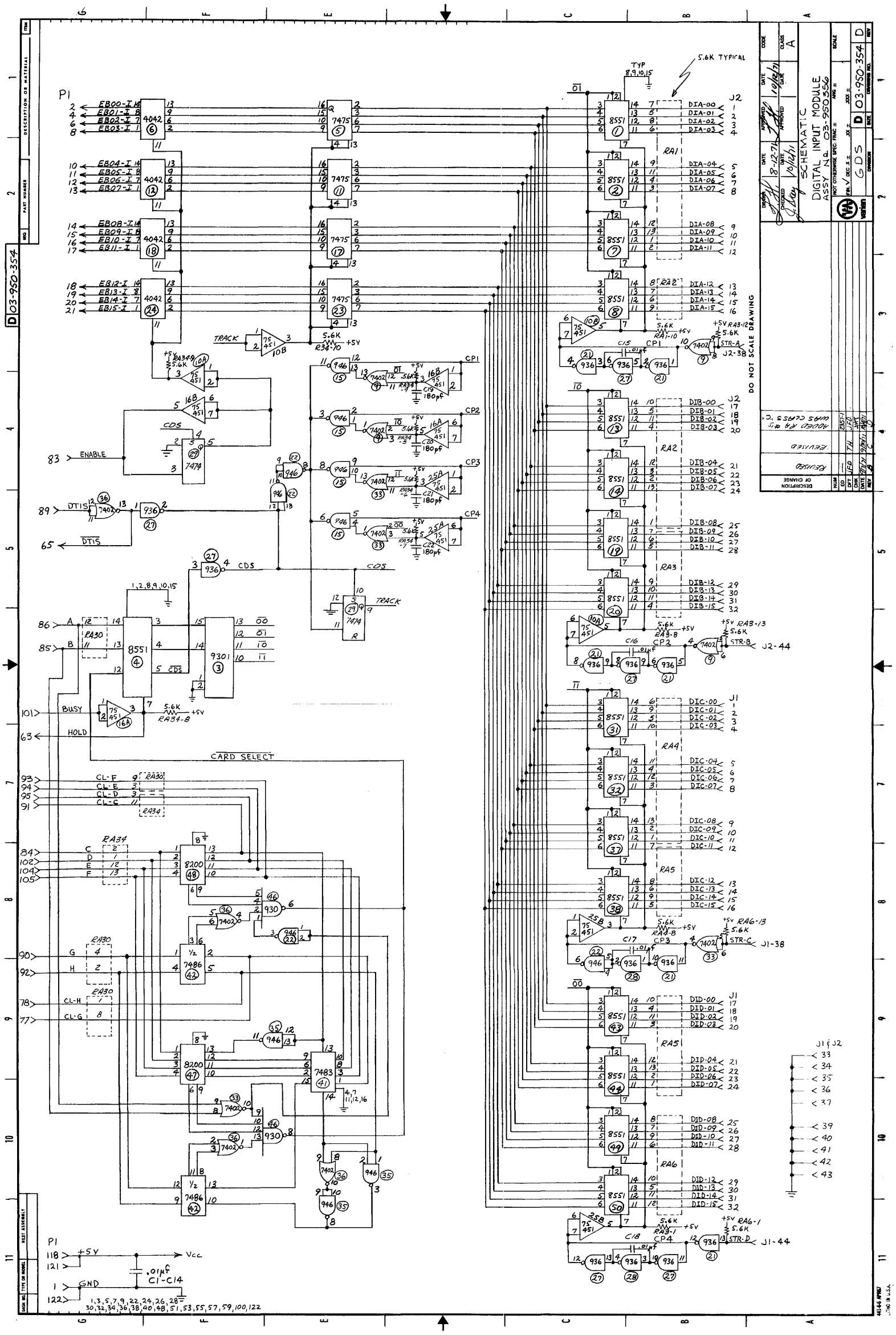
Dimensions	One printed circuit board 7-3/4 x 12 x 1/2 inches.
Connectors	Two 44-terminal card edge connectors. One 122-terminal card edge connector.

APPENDIX C: SCHEMATICS, ASSEMBLIES, PARTS LIST

Digital Input Module 03-950354

DIGITAL INPUT MODULE, 950356

Schematic Reference	Description	Varian Part No.
IC2,4,7,8,13,14, 19,20,31,32,37,38, 43,44,49,50	IC Element 8551	62-600 317
IC6,12,18,24	IC Element 4042	62-600 316
IC9,33,36	IC Element 7402	62-600 356
IC10A,10B,16A, 16B,25A,25B	IC Element 75451	62-600 260
IC3	IC Element 9301	62-600 400
IC29	IC Element 7474	62-600 365
IC 5,11,17,23	IC Element 7475	62-600 343
IC21,27,28	IC Element 936	62-600 309
IC15,22,35	IC Element 946	62-600 303
IC47,48	IC Element 8200	62-600 347
IC42	IC Element 7486	62-600 366
IC41	IC Element 7483	62-600 373
IC46	IC Element 930	62-600 308
C1-C18	Capacitor, Ceramic - .01 μf	41-228 004
C19-C22	Capacitor, Mica - 180 pf	41-159 568
RA1-RA6,RA30,34	Resistor Array - 5.6 K	03-998 011


D03-950-354
DESCRIPTION OF MATERIAL
PART NUMBER
REQ
ITEM
P1
EB00-I
EB01-I
EB02-I
EB03-I
EB04-I
EB05-I
EB06-I
EB07-I
EB08-I
EB09-I
EB10-I
EB11-I
EB12-I
EB13-I
EB14-I
EB15-I
4042
7475
8551
RA1
RA2
RA3
RA4
RA5
RA6
DIA-00
DIA-01
DIA-02
DIA-03
DIA-04
DIA-05
DIA-06
DIA-07
DIA-08
DIA-09
DIA-10
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DIA-12
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DIB-08
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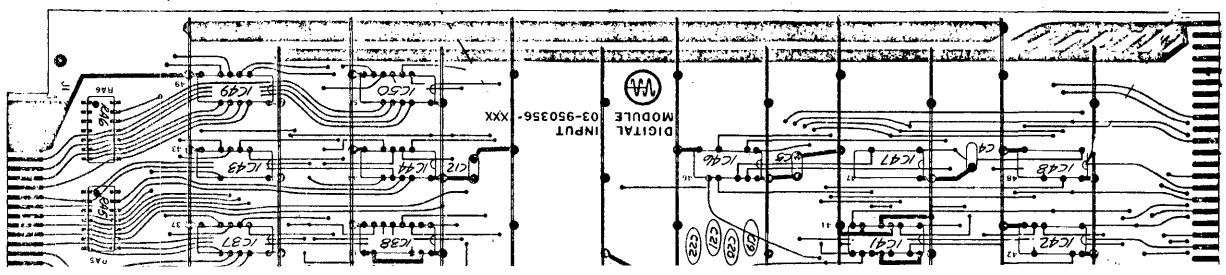
DIB-10
DIB-11
DIB-12
DIB-13
DIB-14
DIB-15
DIC-00
DIC-01
DIC-02
DIC-03
DIC-04
DIC-05
DIC-06
DIC-07
DIC-08
DIC-09
DIC-10
DIC-11
DIC-12
DIC-13
DIC-14
DIC-15
DID-00
DID-01
DID-02
DID-03
DID-04
DID-05
DID-06
DID-07
DID-08
DID-09
DID-10
DID-11
DID-12
DID-13
DID-14
DID-15
J1
J2
J1 & J2
5.6K TYPICAL
TYP 8,9,10,15
TRACK
ENABLE
DTIS
CDS
BUSY
HOLD
CARD SELECT
CL-E
CL-F
CL-D
CL-C
CL-H
CL-G
STR-A
STR-B
STR-C
STR-D
CP1
CP2
CP3
CP4
P1 118 +5V
121
1 GND
122
.01µf C1-C14
Vcc
1,3,5,7,9,22,24,26,28,30,32,34,36,38,40,48,51,53,55,57,59,100,122
DO NOT SCALE DRAWING
SCHEMATIC
DIGITAL INPUT MODULE
ASSY No. 03-950356
GDS
D
03-950-354
DESCRIPTION OF CHANGE
REVISED
ADDED R# #'s
CHAS CHAS 3 'C'
DRAWN
CHECKED
APPROVED
DATE
CODE
CLASS
A
SCALE
DIMENSION
DRAWING NO.
REV
NOT OTHERWISE SPEC: FRAC ± ANG ± XXX ± DEC X ± XX ± XXX ±
FSN √
MATL
FINISH
NEXT ASSEMBLY
USED ON MODEL
ITEM NO.
TYPE OR MODEL
QTY REQ'D
DESCRIPTION
PART NUMBER
MATERIAL
REMARKS
441-66 APR67
PRINTED IN U.S.A.


DIGITAL INPUT MODULE
03-950356-XXX

USER'S GUIDE
DIGITAL OUTPUT MODULE
for use with
Varian 620 or V73 Series Computers

Publication No. 03-996 810B

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TABLE OF CONTENTS

FIGURES

TABLES

1. INTRODUCTION

1.1 GENERAL

The Digital Output Module (DOM) and Digital Output Expansion Module (DOME) are hardware options that interface Varian 620 and V73 series computers with external devices which require digital data as their inputs.

A DOM includes four functional features:

- Digital Output Registers, which transfer digital data from the computer to an external device.
- Gated Inputs, which gate digital data from an external device into the computer.
- External Control (EXC) Interface Logic, which allows a computer program to control external devices via logic-signal EXC output lines.
- Sense (SEN) Interface Logic, which allows a computer program to test the status of external devices by sampling logic levels present on Sense input lines.

A DOME, which includes digital output registers and gated inputs, is used to expand the DOM's capability. Up to three DOMEs can be connected to each DOM. As many as 32 DOM and DOME modules can be attached to a single computer to provide the following I/O capability:

64 Digital Output Registers -	Each module (DOM or DOME) contains two 16-bit registers.
32 Gated 16-bit Inputs -	Each module (DOM or DOME) contains 16 gated inputs.

64 External Control Outputs -	Each DOM contains eight External Control output lines.
64 Sense Inputs -	Each DOM contains eight Sense input lines.

Simple installation procedures allow the DOM to be installed either at the factory or on-site at the user's facility. A comprehensive software test package is provided with the DOM for post-installation checkout of its operational status. In addition the module is fully supported by standard Varian software and input/output options.

1.2 FUNCTIONAL DESCRIPTION

All elements needed to perform the four basic DOM functions are packaged on a single plug-in printed circuit board. Figure 1-1 illustrates the functional elements included in a DOM module. A DOME contains only those elements shown in the shaded portion of Figure 1-1.

Device Address

The computer program must select a DOM by its device address before any DOM operation can be performed. There are eight device addresses reserved for DOMs (50_8 to 57_8). As many as four modules can be located at a single device address; one of the four, known as the master DOM, contains the device address decode logic. The other three are DOMEs which function as slaves to the DOM but provide the same basic capability.

DOM Select

An individual register or gated input must be selected by the computer program, using an Extended EXC (EXC2) instruction. There are eight select lines located at each device address; each line is enabled by the corresponding EXC2 instruction.

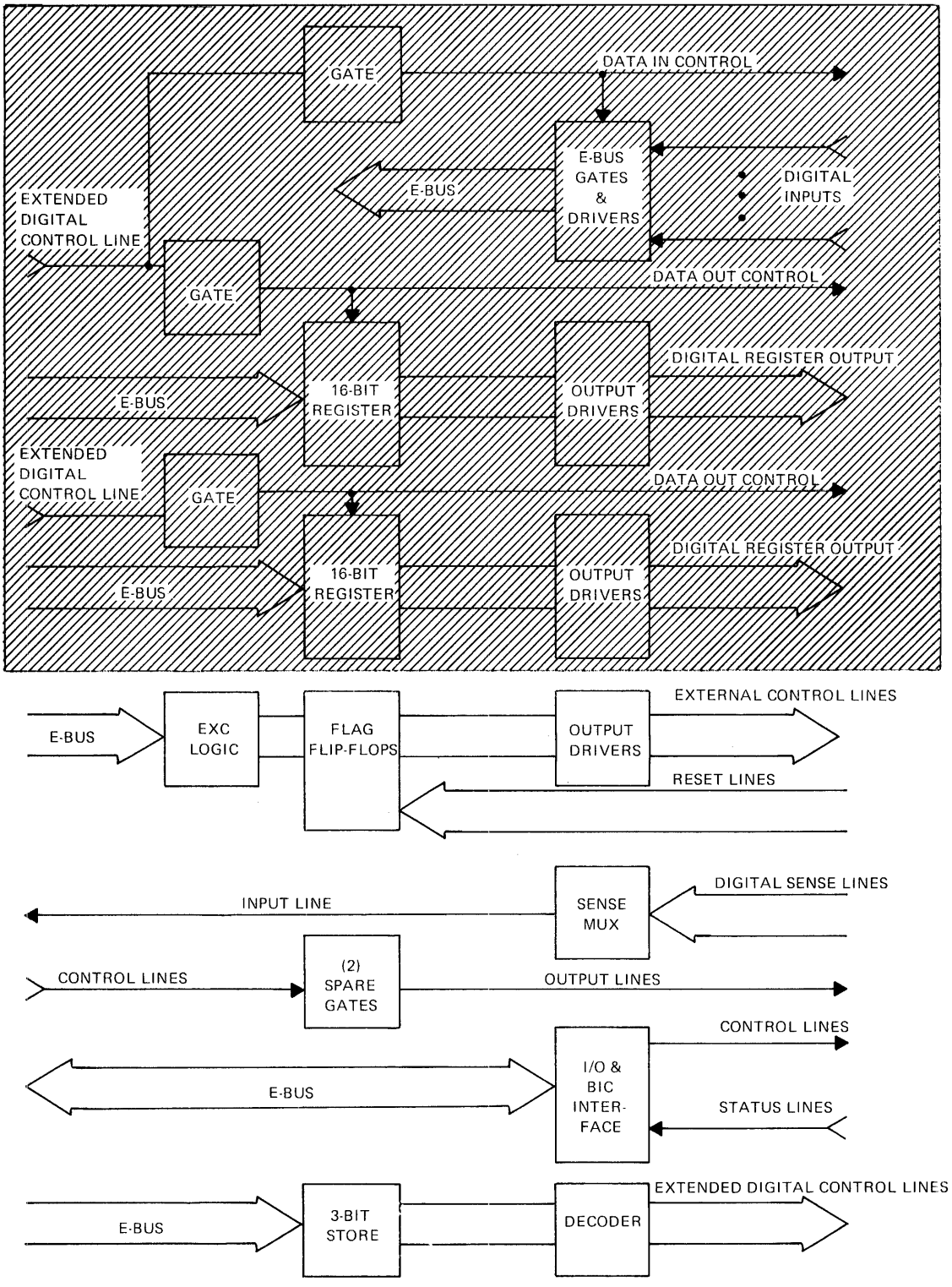


Figure 1-1. Digital Output Module Block Diagram

The master DOM contains the Select logic. Once selected, a register or gated input remains selected until a different register or gated input at the same address is selected, until SYSTEM CLEAR occurs, or until power is interrupted.

Data transfers may be performed under program control or via direct memory access (DMA); interface logic to the required Buffer Interlace Controller (BIC) is provided for the DMA transfer.

External Control (EXC) Interface

External Control signals, which are generated by the computer to control operations in external devices, are distributed to the external devices via eight EXC output lines. The DOM's EXC interface logic selects one of the eight output lines according to the contents of the function code received from the computer. The master DOM contains all EXC interface logic for that device address.

Sense Interface

The Sense multiplexer on the Digital Output Module selects one of eight sense input lines from external devices and gates the logic level present on that line to the computer. The master DOM contains all Sense interface logic for that device address.

2. PROGRAMMING

2.1 INTRODUCTION

This section describes Assembly Language programming techniques for operating the DOM and presents instructions for using the DOM software test package for module checkout. This section also describes the usage of two special driver programs which are supplied with the DOM. More detailed programming information may be found in the 620 series or V73 system handbooks.

A program directs DOM operation in four ways:

- Transfers data to digital output registers.
- Reads gated inputs.
- Distributes signals to External Control lines.
- Checks Sense input lines.

Note that data transfers may also be performed using the Buffer Interlace Controller (BIC) hardware option.

2.2 DATA TRANSFER UNDER PROGRAM CONTROL

The essential programming instructions for transferring data to a DOM output register are shown in Table 2-1. The instructions are given in the form of a block of code from a typical program.

A digital output register is selected for a data transfer operation by means of an EXC2 instruction. For example, an instruction with the format EXC2 XYY selects register number X at device address YY. Table 2-2 shows the standard register

and gated input number assignments for a DOM device address. After a register is selected, data is transferred to it by means of an OAR, OBR, or OME instruction.

Table 2-1. Instructions To Output Data Under Program Control

Program Step			Function
ONE	LDA	J	Load value of variable J into the computer A register. (LDB may be used instead of LDA.)
TWO	EXC2	XYY	Select module's register or gated input number X (0 to 7) at device address YY (50 to 57).
THRE	OAR	OYY	Output data from A register to module at address YY (50 to 57). (OBR would be used if LDB had been used. OME could also be used to output data.)
(Time Delay Code)			
(Code to Generate Next Output Number)			
	JMP	ONE	

Table 2-2. Digital Register and Gated Input Number Assignments

Module	Register Number	Input Number
DOM (master)	0, 1	0
DOME (first slave)	2, 3	2
DOME (second slave)	4, 5	4
DOME (third slave)	6, 7	6

When an output register is selected at a particular device address, it remains selected until another EXC2 instruction selects a different register at the same device address. For example, assume the following sequence of coding:

EXC2	153	Select Second Register on First Module at Device Address 53.
⋮		
EXC2	253	Select First Register on Second Module at Device Address 53. This changes the selection specified by the previous EXC2 since both registers are located at the same device address.
⋮		
EXC2	252	Select First Register on Second Module at Device Address 52. This has no effect on the previous EXC2 instructions since the registers are located at different device addresses.

Thus, it is possible to select one register or gated input at each DOM device address. The following example illustrates the selection and usage of registers and inputs at four different device addresses.

EXC2	050	Select First Register on First Module at Device Address 50.
EXC2	351	Select Second Register on Second Module at Device Address 51.
EXC2	453	Select First Register on Third Module at Device Address 53.
EXC2	452	Select Gated Input on Third Module at Device Address 52.
LDA	V1	Load Variable V1 into Computer Register A.
LDB	V2	Load Variable V2 into Computer Register B.
OAR	050	Output V1 to Selected Register at Device Address 50.
OBR	051	Output V2 to Selected Register at Device Address 51.
LDA	V3	Load Variable V3 into Computer Register A.

OAR	053	Output Variable V3 to Selected register at Device Address 53.
CIB	052	Read Selected Input at Device Address 52 into Computer Register B.

2.3 DATA TRANSFER WITH BUFFER INTERLACE CONTROLLER

The Buffer Interlace Controller (BIC) is a hardware option which allows the user to transfer a block of data to or from a peripheral device using only one set of instructions. The user loads the first and last memory address location for a data block into special registers in the BIC; the BIC then transfers the specified data block to (or from) the peripheral device.

Once a program initiates the BIC data transfer, the BIC operates in parallel to the computer program, stealing cycles to access data from memory via direct memory access. Thus, the program can proceed independently with other processing.

Typically, the program instructions for initializing a BIC are coded as a separate subroutine. The applications program then calls this subroutine when BIC usage is required. Table 2-3 illustrates the coding of a BIC initialization subroutine and demonstrates the usage of the subroutine within an applications program. The sequence of operations is as follows:

BIC Subroutine -

1. Sense that BIC is not busy, using a standard SEN 020 instruction. The BIC cannot be initialized while it is busy. If busy, loop until BIC completes its operation.
2. Initialize the BIC, using a standard EXC 021 instruction.
3. Store data block's initial and final addresses in the appropriate BIC address registers.
4. Enable the BIC, causing data transfer.

Table 2-3. Instructions To Output Data Under BIC Control

Program Step			Function
BIC Subroutine -			
BICS	ENTR	0	
WAIT	SEN	020, GO	Go when BIC not busy.
	NOP		
	NOP		
	JMP	WAIT	
GO	EXC	021	Initialize BIC.
	OME	020, FIRST	Set start address of memory block.
	OME	021, LAST	Set end address of memory block.
	EXC	020	Enable BIC.
	RETU*	BICS	
Applications Program -			
	EXC2	0650	Select channel.
WAIT	SEN	MNN, READY	Loop if device not ready.
	JMP	WAIT	
READY	CALL	BICS	Set up BIC.
	EXC	050	Connect BIC to DOM.
TWO	NOP		
	NOP		
	SEN	020, TWO	Check BIC not busy; return to TWO if busy.
	SEN	021, TEN	Check for abnormal stop.

Applications Program -

1. Select the DOM or DOME output channel by using the appropriate EXC2 instruction.

2. Wait until the peripheral device is ready to receive data. Sense line M at device address NN (50 to 57) is used to declare the device's status. Loop if the device is busy.

3. Call BIC subroutine.

4. Connect BIC to DOM, using an EXC instruction. An EXC 0YY instruction, where YY is the DOM device address, is used to output data. An EXC 1YY instruction is used to read gated input data.

5. The sample program in Table 2-3 suspends computation while the BIC is busy by looping around the statements,

```
TWO   NOP
      NOP
      SEN  020,  TWO
```

   until data transfer has been completed.

6. Check for an abnormal stop; if yes, branch to suitable diagnosis or correction code.

Note that the BIC initial and final register addresses may be any pair of octal numbers in the range 20 through 27. Ordinarily, in systems employing more than one BIC, addresses 20 and 21 are assigned to the first BIC's registers; 22 and 23, 24 and 25, and 26 and 27 are assigned to the second, third, and fourth pairs of registers, respectively.

2.4 GATED INPUTS

DOM gated inputs are selected in the same manner as digital output registers, using EXC2 instructions. For example, the instruction EXC2 XYY selects gated input number X (0, 2, 4, or 6) at device address YY (50 to 57). Table 2-2 shows the gated input number assignments for each DOM device address. Once selected, the gated input at a particular device address remains selected until another EXC2 instruction selects a different register or gated input at the same device address.

After an input is selected, it is read by means of an INA, INB, IME, CIA, or CIB instruction.

2.5 EXTERNAL CONTROL

External Control signals may be generated by a computer program to provide a variety of logic controls for external devices.

The user has eight External Control lines available at each DOM. The instruction that causes an External Control Signal is:

EXC XYY

where X (0 to 7) defines one of eight External Control lines at DOM device address YY (50 to 57).

The signals are also made available to the backplane connectors so that they may be used to control certain portions of DOM logic when required by the use of an option such as the BIC. This use of EXC signals will depend on specific applications of the DOM.

A program can set, but cannot reset, an External Control signal; reset is a function of external hardware. As determined by external interconnections, one External Control signal can reset another, other external electronic components can control reset, or the External Control signal can reset itself (pulse operation). Several methods for resetting External Control output signals are discussed in this section. These methods illustrate how the program can use the EXC command to trigger sequences of operations that have been predetermined by system hardware interconnection. The wiring configurations for these methods are illustrated in Figures 2-1 through 2-6. In all cases, some external wiring is required; the external modifications for each method are shown to the right of the vertical dashed line in each figure. Section 3.2 discusses the circuit logic for these reset types.

Command Sequence Reset

By connecting the EXC-N output of one latch to the REX-M of another latch, selecting the first will reset the second. This requires that the function codes in a series

of EXC commands always follow the sequence prescribed by the latch interconnections. Figure 2-1 illustrates one configuration. In this example, the command sequence would progress from EXC-0 to EXC-7.

For example, in the following sequence of instructions used with this configuration, one External Control line resets one other line.

EXC	050	EXC 750 is automatically reset, EXC 050 is set.
EXC	150	EXC 050 is automatically reset, EXC 150 is set.
EXC	250	EXC 150 is automatically reset, EXC 250 is set.

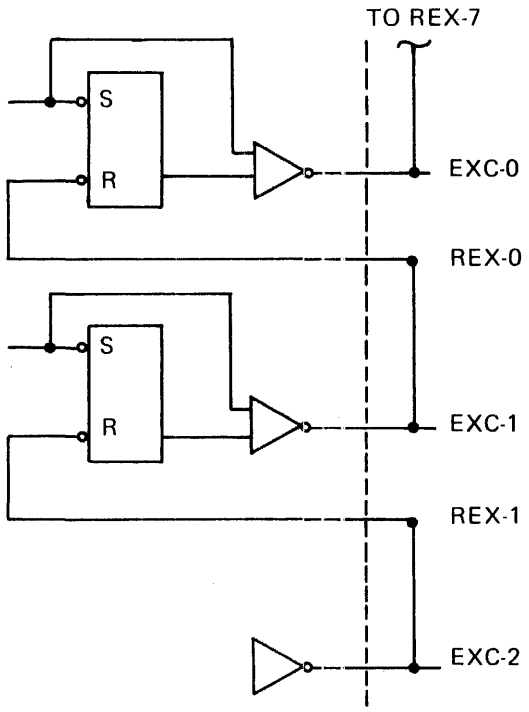


Figure 2-1. Command Sequence Reset Wiring

Special Assignment Reset

One latch can be assigned as the reset latch. An EXC command selecting that latch will then reset all other EXC latches. Figure 2-2 illustrates this configuration. The following sequence of program instructions used with this configuration functions as follows:

EXC	050	Set EXC 050.
EXC	150	Set EXC 150.
EXC	250	Set EXC 250.
EXC	750	EXC 050, EXC 150, and EXC 250 are automatically reset.

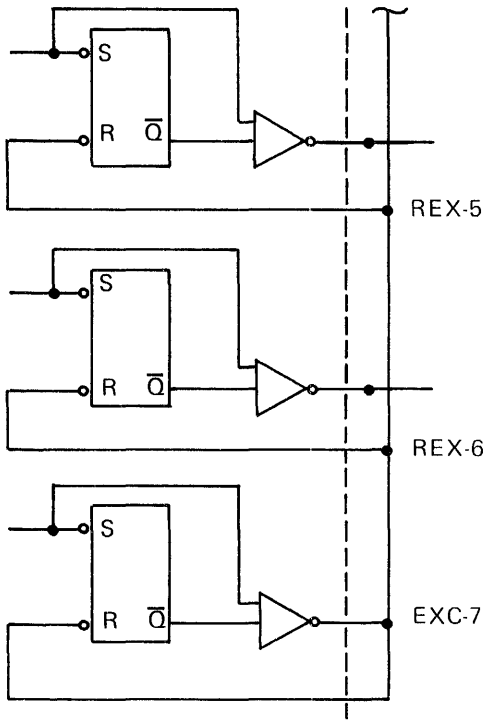


Figure 2-2. Special Assignment Reset Wiring

Fixed Delay Reset

An EXC latch can reset itself, following a suitable delay provided by an RC, transmission line, or other delay circuit. Figure 2-3 illustrates a typical latch circuit

with an RC delay. An example of an instruction which can be used with such a configuration is as follows:

EXC 050 EXC is set for nn μsec then resets itself. (nn is determined by delay hardware added to the EXC output.)

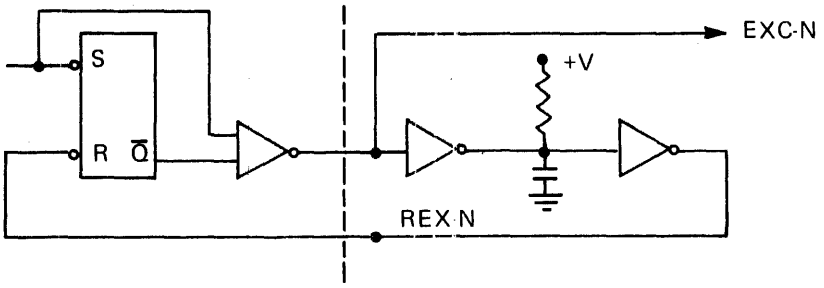


Figure 2-3. Fixed Delay Reset Wiring

Reset Returned By Receiving Device

The reset signal can be returned by the receiving device as shown in Figure 2-4. In this case, the pulse width is determined by the cable length. This insures that the pulse width is great enough for proper reception, regardless of cable capacitance.

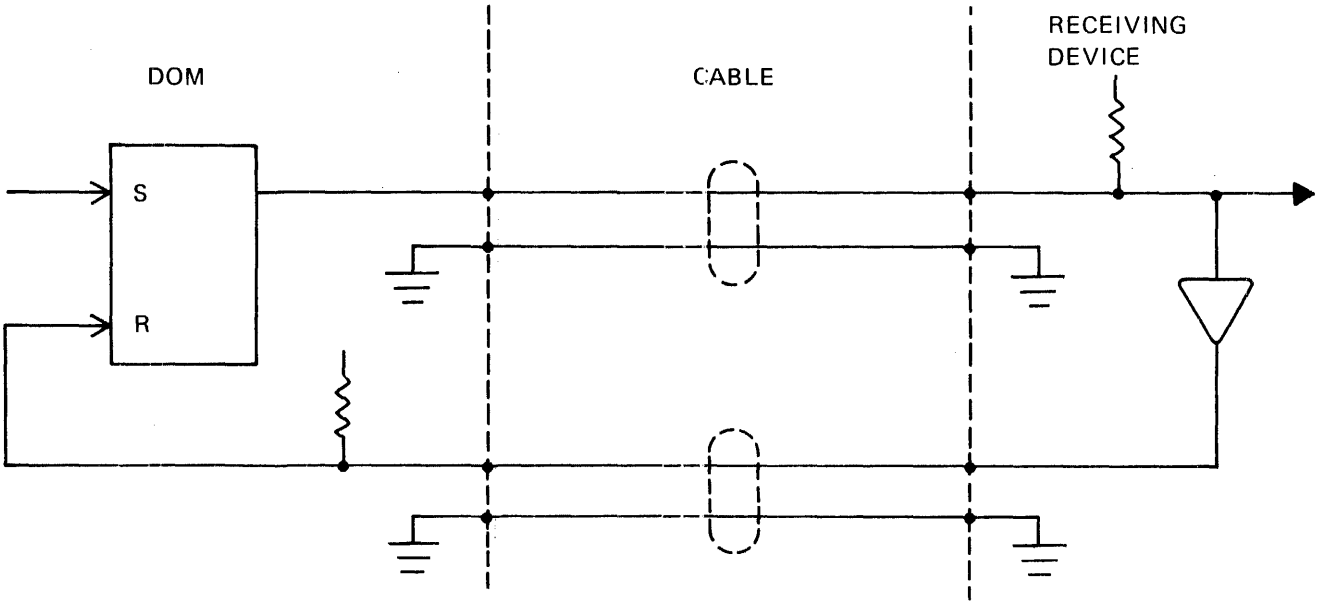


Figure 2-4. Reset Returned By Receiving Device

Automatic Reset

Connecting a REX-N output to ground will cause the EXC-N output to reset as soon as the EXC input to the latch goes false. In the 620/L computer, this produces a 200 nanosecond pulse. (The pulse duration will differ for other computers.) Figure 2-5 illustrates such a configuration. In this configuration, an EXC is set, and then reset after 200 nanoseconds. This is accomplished by making the EXC latch output follow the latch input, which is a 200 nanosecond pulse. Normally, the input pulse causes the EXC to be set "on", but the input pulse in no way influences resetting the EXC to "off".

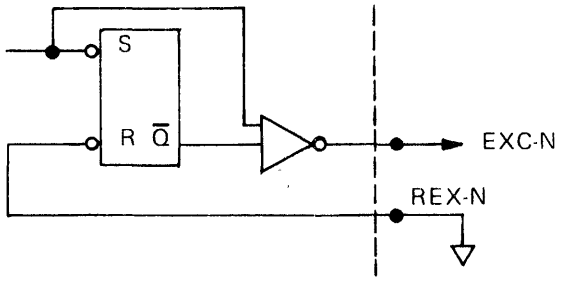


Figure 2-5. Automatic Reset Wiring

External Logic Reset

In this case, the flip-flop is set by the program and reset by the external device. This is especially useful in passing data or control commands; the program sets the EXC flag to indicate that data is ready, and the external device resets it to acknowledge that it has received the data or that it is ready to accept additional data. The EXC output is connected to a Sense input as well as to the external device, so the program can determine that the acknowledgement has been received. (See Figure 2-6.) The same scheme can, of course, be used for receipt of data by the computer.

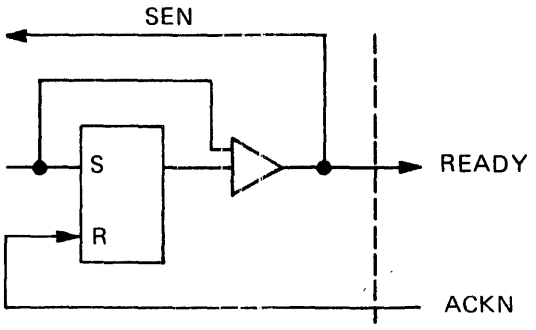


Figure 2-6. External Logic Reset Wiring

External Control Usage With BIC

Table 2-4 illustrates a program using External Control Line 150 to connect the BIC to the Digital Output Module at device address 050. As discussed in Section 3.1, the execution of EXC 150 also establishes the direction of data flow into memory.

2.6 SENSE LINES

Sense lines allow the program to sense a signal from an external device, and branch depending on whether the Sense line is true or false.

There are eight external sense lines associated with each DOM device address. The command which selects a sense line is:

SEN XYY

X (0 to 7) defines a specific line at device address YY (50 to 57).

Table 2-4 illustrates three uses of the SEN statement. Statement TWO inhibits data transfer via the BIC until Sense line 4 at device address 50 is sensed "false". The other two SEN statements are BIC system commands. (See 620 series or V73 system handbooks.)

Table 2-4. Use of External Sense Logic

	Program Step		Function
WAIT	SEN	020, ONE	Sense BIC not busy.
	NOP		
	NOP		
	JMP	WAIT	
ONE	EXC	021	Initialize BIC.
	OAR	020	Set start address in BIC register.
	OBR	021	Set end address in BIC register.
	EXC	020	Enable BIC
NOP	NOP		
	NOP		
TWO	SEN	450, NOP	Start data transfer when Sense line 4 at device address 50 is "false". Branch back if "true".
FIVE	EXC	150	Connect BIC to DOM.
	SEN	021, TEN	Check for abnormal stop.

2.7 DOM SOFTWARE DRIVERS

Two driver programs are supplied to provide convenient access to Digital Output Modules without detailed knowledge of hardware. These drivers may be used by themselves or embedded in an operating system.

The drivers and their functions are:

PDOM - Provides programmed data transfers, either input or output.

DDOM - Provides direct memory transfers, either input or output.

Note that these drivers assume the following device address assignments:

Address (Octal)	Device
050	DOM
020-021	BIC, No. 1
022-023	BIC, No. 2
024-025	BIC, No. 3
026-027	BIC, No. 4

If other device addresses are required, a reassembly of the drivers must be performed.

Programmed Data Transfer (PDOM)

The programmed data transfer driver (PDOM) provides programmed data transfers to or from a selected DOM. A variable number of 16-bit words are transferred each time the driver is called.

PDOM is called with the following assembly language sequence:

CALL PDOM, DOMNR, I/O SELECT, NUM, STRT ADDR, ERROR EXIT

All entries in the calling sequence are either direct addresses or indirect addresses which point to the actual arguments. Multiple levels of indirect addresses are permitted. The arguments are defined as follows:

DOMNR - An integer value which specifies the DOM register or input to be selected. The range of DOMNR must be between 1 and 64, inclusive;

otherwise control passes to ERROR EXIT. The DOMNR arguments correspond to the actual device address codes as follows:

DOMNR	Device Address
1	050
2	150
3	250
•	•
•	•
•	•
9	051
•	•
•	•
•	•
64	757

I/O SELECT - A pointer to the location of an I/O select code. The select code must be a one (1) which specifies input, or a zero (0) which specifies output. Note that the DOM hardware provides 32 input channels and 64 output channels. The DOMNR argument must be an odd number (1, 3, 5, 7, etc.) when calling for input. A conflict between the DOMNR and I/O SELECT arguments causes the driver to pass control to ERROR EXIT.

NUM - An integer value which specifies the total number of 16-bit words to be transferred to or from the selected DOM. If NUM is zero or less control passes to ERROR EXIT.

STRT ADDR - A pointer to the location containing the first word address of the input or output buffer.

ERROR EXIT - The actual start address of the user's error routine. Control is transferred to ERROR EXIT when illegal input arguments are detected.

Appendix C contains a sample program which illustrates the use of PDOM.

Direct Memory Data Transfer

Two programs, DDOM and SDOM, are provided to utilize the BIC to transfer data directly from memory to a selected DOM without programmed intervention. DDOM and SDOM offer two advantages over PDOM:

- Data transfer rates are not limited by software overhead.
- The applications program is freed to work on other processes while the BIC supervises and controls the data transfer.

Unlike other peripherals, DOMs do not have built-in logic to determine when the next data item should be transferred to them. Therefore, external hardware must be provided to indicate when data from memory is to be transferred to the DOM. This is accomphished by providing a Data Ready line at P1-73 on the computer backplane. The data transfer timing is completely under the control of this line, which is also available on J1-9.

In addition to this external signal, two of the eight External Control outputs on the DOM control module must be dedicated. One jumper connects P1-79 to P1-74, and another jumper connects P1-80 to P1-75. The DDOM driver uses the following External Control lines for this function:

DOMNR	EXC Used For BIC Connect	
	Output From Memory	Input to Memory
1-8	EXC 050	EXC 150
9-16	EXC 051	EXC 151
17-24	EXC 052	EXC 152
25-32	EXC 053	EXC 153
33-40	EXC 054	EXC 154
41-48	EXC 055	EXC 155
49-56	EXC 056	EXC 156
57-64	EXC 057	EXC 157

DTO-X and DTI-X must be wired in daisy chain fashion from each master DOM to its slave DOMEs. P1-102 is wired to P1-102 of each DOME, and P1-63 is wired to P1-63 of each DOME. J1-5 and J1-8 also must be grounded so that the flip-flops associated with EXC 0XX and EXC 1XX are automatically reset.

Direct memory data transfer to a DOM is accomplished by a two-step process. First, DDOM is called to initiate the transfer and return control immediately. Then, SDOM is called at the user's convenience to determine when the transfer is complete.

DDOM Driver

The DDOM driver is called with the following assembly language sequence:

CALL DDOM, BICNR, DOMNR, I/O SELECT, STRT ADDR, ERROR EXIT

All entries in the calling sequence are either direct addresses or indirect addresses of the actual arguments. Multiple levels of indirect addresses are permitted. The arguments are defined as follows:

BICNR - An integer value which specifies the BIC to be used for data transfer. The range of BICNR is from 1 to 4 corresponding to BIC device addresses $20\text{-}21_8$ through $26\text{-}27_8$. A value outside the legal range causes control to pass to ERROR EXIT.

DOMNR - An integer value which specifies the DOM register or input to be selected. The range of DOMNR must be between 1 and 64, inclusive; otherwise control passes to ERROR EXIT. (See PDOM driver for a description of DOMNR and actual device address relationship.)

I/O SELECT - A pointer to the location of an I/O select code. The select code must be a one (1) which specifies input, or a zero (0) which specifies output. Note that the DOM hardware provides 32 input channels and 64 output channels. The DOMNR argument must be an odd number when calling for input. A conflict between the DOMNR and I/O SELECT causes the driver to pass control to ERROR EXIT.

NUM - An integer value which specifies the total number of 16-bit words to be transferred to or from the selected DOM. If NUM is zero or less, control passes to ERROR EXIT.

STRT ADDR - A pointer to the location containing the first word address of the input or output buffer.

ERROR EXIT - The actual start address of the user's error routine. Control is transferred to ERROR EXIT when illegal input arguments are detected.

Appendix C shows a sample program which illustrates the use of DDOM.

SDOM Routine

The SDOM routine checks the status of a previously initiated direct memory data transfer. SDOM is called with the following assembly language sequence:

```
CALL SDOM, STATUS
```

The single entry in the calling sequence can be either a direct address or an indirect address which points to the actual argument. The argument is defined as follows:

STATUS - This argument receives a value of 0, 1, or 2 to indicate the status of the transfer operation:

Value	Meaning
0	Operation not complete
1	Operation complete; no errors
2	Operation aborted

2.8 TEST PROGRAMS

A set of test programs is provided for DOM checkout. The set consists of three programs which may be selected through the Maintain II Test Executive. The programs, numbered 0 through 3, are as follows:

Test No.	Description
0	Returns control to the Test Executive Program.
1	Tests External Control and Sense lines.
2	Tests registers and gated inputs.
3	Tests BIC interface.

These programs may be selected in any order and may be run as often as desired. This allows registers and inputs with different device codes to be tested.

The minimum computer configuration on which the tests may be run is a 620 or V73 series computer with 4 K of memory, a teletype terminal, and a DOM card. In addition, a DOM test shoe (Part No. 03-950401) is required for running the tests.

Supervisor Program

A simple supervisor or test program selector is provided as part of the test package to allow the user to select individual tests and return control to the Test Executive Program. The Test Executive Program is a standard Varian software option which must be loaded and run prior to the initiation of the DOM test package. Instructions for operating this program are given in the Test Program Manual (Publication No. 98A 9908-960). The DOM test package is loaded through the Test Executive.

When the Test Executive Program is running, the "L" command may be used to load the test package and transfer control to its supervisor. If the test package is already loaded, the "G500" command may be used to transfer control to the supervisor.

When the supervisor is activated, it responds by issuing a carriage return/line feed and by starting to print a series of prompting messages. The user must enter a valid response to each message as it is printed. An invalid response causes the message to be repeated. The first message is:

```
DIGITAL OUTPUT TEST SUPERVISOR
ENTER DEVICE ADDRESS?
```

The user must enter the DOM device address, which is an octal number between 050 and 057, followed by a period. The supervisor will then print:

ENTER BIC DEVICE ADDRESS?

The user must enter any of the following assigned octal numbers: 020, 022, 024, or 026 followed by a period.

The DOM and BIC device addresses entered at this time will be used throughout the three tests, where applicable. To change device address selections, the supervisor must be reactivated from the Test Executive Program or run from location 500. After the device addresses have been entered, the supervisor will print:

ENTER TEST NO. ?

The user should enter any number between 0 and 3 followed by a period. The supervisor will then transfer control to the selected test program, which will identify itself and perform its specified functions.

Test 1 should be used for each master DOM to test the EXC and Sense logic.

Test 2 should be used for each digital output register in the system.

Test 3 should be used to check the BIC interface to the DOM and should be exercised on each digital output register that will be driven under BIC control.

Sense Switches

During all DOM tests, the sense switches may be used to control the mode of operation. The normal mode is followed when all switches are OFF; one or more switches may be set to control operation as follows:

SS1 — Sense switch 1 suppresses teletype printouts of test results and error messages. This function is useful to speed up the

continuous execution of a test so that an oscilloscope may be used to monitor signals.

SS2 Sense switch 2 causes a test to repeat indefinitely without user intervention.

SS3 Sense switch 3 terminates execution of a test and returns control to the supervisor. If sense switch 3 is set when the supervisor requests a new test number, the following message will be printed:

RESET SENSE SWITCH 3

A new test may be selected after SS3 is reset.

Test 1 - External Control and Sense Test

This test uses a special test shoe which must be plugged into J1 and J2 of the DOM card. The test checks all EXC and Sense lines on a given device address. The test shoe is designed to connect each EXC output to a SENSE input and to reset another EXC according to the following table.

EXC output	Sense Line	EXC reset
00XX	03XX	06XX
02XX	07XX	00XX
04XX	05XX	02XX
01XX	06XX	04XX
03XX	04XX	01XX
05XX	02XX	03XX
07XX	00XX	05XX
06XX	01XX	07XX

Therefore, at each step in the table only one of the Sense lines should be true at a time. All Sense lines are polled after each step and errors are reported if detected and if sense switch 1 is reset.

When the test program is activated, it will print:

EXTERNAL CONTROL AND SENSE TEST

If no errors occur during the execution of the test, the program returns control to the supervisor after printing the following message:

TEST PASSED

If errors occur during the test, one or more of the following messages will be printed:

EXC 00XX OR SEN 03XX ERROR
EXC 02XX OR SEN 07XX ERROR
EXC 04XX OR SEN 05XX ERROR
EXC 01XX OR SEN 06XX ERROR
EXC 03XX OR SEN 04XX ERROR
EXC 05XX OR SEN 02XX ERROR
EXC 07XX OR SEN 00XX ERROR
EXC 06XX OR SEN 01XX ERROR

If the first error occurs, the problem may be in the address decoder logic on the master DOM.

Test 2 - Register and Gated Input Test

Each DOM card has two output registers and one 16-bit gated input channel. For purposes of these tests the registers and inputs at a particular device address are numbered as shown in Table 2-2.

The DOM test shoe is used to connect digital output registers to the gated inputs. The even-numbered output register is assigned to J2-1 through 16 for bits 0 to 15, respectively; the odd-numbered output register is assigned to J2-17 through 32 for bits 0 to 15, respectively; a single set of input gates is assigned to J1-29 through J1-44 for bits 0 to 15, respectively on each card. The test shoe feeds the even-

numbered output register directly back into the input gates with a wired-OR condition with the odd-numbered output register. The odd-numbered output registers are fed back in a scrambled form.

The program outputs a series of 16-bit numbers to the selected output register and reads them back in through the input gates and unscrambles them if the odd-numbered register is selected. All 65,536 different 16-bit numbers are output. The values are checked to see if the inputs match the original outputs.

When the test program is activated, it will print:

```
REGISTER TEST
ENTER OUTPUT REGISTER NO
```

The user should enter the appropriate number between 0 and 7 followed by a period. The test program compares the inputs to the outputs and prints any readings which do not match. If the input and output readings match, the program prints:

```
TEST PASSED
```

This test runs for about 15 seconds for even-numbered registers and about 22 seconds for odd-numbered registers. The odd-numbered register tests run longer because the input must be unscrambled before it can be compared to the output. This is not required on the even-numbered register tests.

BIC Interface Test

This test uses the even-numbered output register and input gates on each DOM under BIC control to test the BIC interface. The output register is tied directly back into the input gates by the test shoe.

EXC 0 is used to provide the trap-out request by wiring P1-74 to P1-79. EXC 1 is used to provide the trap-in request by wiring P1-75 to P1-80. Note that these connections should be made even if the BIC is not used.

When the test program is activated, it prints:

```
BIC INTERFACE TEST
ENTER OUTPUT REGISTER NO
```

The user must enter one of the following values: 0, 2, 4, or 6 followed by a period.

During the test, trap-in and trap-out requests are given alternately until 20 words have been passed out and then back into 40 sequential memory locations. They are checked to see that each pair of words matches; if not, both input and output are listed in octal. If all 20 pairs match, the program prints:

```
TEST PASSED
```

The 20 words passed during the test are as follows:

- All odd bits set (0125252_8)
- All even bits set (052525_8)
- Each single bit set (0100000_8)
  (0040000_8)
  :
  (001_8)
- All bits reset (0_8)
- All bits set (0177777_8)

3. I/O INTERFACE THEORY OF OPERATION

The Digital Output Modules coordinate four types of communication between the computer and peripheral devices: digital data out, digital data in, External Control signals out, and Sense signals in. The DOM logic responsible for providing these four interfaces is discussed in this section.

All communication between the DOM and the computer is conducted on the computer I/O bus. In the following discussion, mnemonics used to identify E-bus signals include the suffix "I". Signals transferred between the DOM and the BIC are carried on the B-bus; mnemonics for these signals include the suffix "B". Refer to a Varian 620 series or V73 system handbook and Buffer Interlace Controller Manual for details regarding communication conducted via the computer I/O bus.

The following discussions are keyed by letter designations to schematics and logic diagrams presented in Appendix D.

3.1 DATA TRANSFER

Program-Controlled Data Transfer

A data transfer operation occurs in two stages. First, the individual register or gated input is selected; then a data word is sent to the selected register.

DOM Selection Stage

The selection stage begins when the computer enters the desired device address and function code on E-bus lines EB00-I through EB05-I and EB06-I through EB08-I. A NAND gate on the addressed master DOM decodes the device address and generates a Device Select signal. This is combined with the control line pulse FRYX-I (Function Ready). The resulting signal Function Select combines with a true level on EB15-I to clock the contents of the function code into the EXC2 storage register.

The EXC2 Decode Logic selects one of eight output lines, EXC2-0 through EXC2-7, according to the contents of the function code. Each EXC2 line is connected via a wire wrap jumper in the backplane to the clock input gate of a different register or gated input. An active EXC2 line enables one of three inputs to the clock input gate in preparation for the data transfer stage of the operation.

Data Transfer Stage

The device address is again placed on the E-bus. A true level on EB14-I identifies the operation as a data transfer out and, together with Function-Select, sets the data transfer out (DTOS) latch. Output of the DTOS latch enables the second input to the clock input gate.

After the control pulse FRYX-I goes false, the computer removes the device address from the E-bus and places a data word on lines EB00-I through EB14-I, with a sign bit on EB15-I. This is followed by the control pulse DRYX-I. DRYX-I enables the clock input gate of the selected register or gated input, DRYX-I also resets the DTOS latch.

After DRYX-I goes false, the only true input to the clock input gate of the register is provided by the selected EXC2 line. This input remains true until a different EXC2 line at that device address is selected. Until that time, subsequent data transfer operations for that device address will be routed to the same register or gated input, without requiring another EXC2 instruction.

BIC-Controlled Data Transfer

When a data transfer is under BIC control, a different set of DOM logic is involved.

DOM Selection Stage

The DOM selection stage is the same for a BIC-controlled data transfer as for a program-controlled data transfer; the data transfer stage, however, is not.

Data Transfer Stage

The BIC can be used to control the transfer of data to or from the computer memory under the control of the TROX-B signal.

The DOM provides a flip-flop to allow the computer to determine the direction of data flow. EXC-0 is normally wired to the X-OUT terminal and EXC-1 is normally wired to the X-IN terminal. REX-0 and REX-1 are grounded so that their corresponding EXCs operate as pulses.

EXC-0 is then executed when the BIC is to transfer data out of memory and EXC-1 is executed when the BIC is to transfer data into memory.

XRDY is an input signal to the signal to the Digital Output Module which is used to control the rate at which the BIC transfers data. XRDY presents two logic loads and has a 1 K ohm resistor to +5 Vdc. A low true pulse received by XRDY initiates a BIC data transfer operation after the BIC is connected. The XRDY pulse should be less than 2 microseconds and greater than 50 nanoseconds in duration.

3.2 EXTERNAL CONTROL DECODE

Every master DOM makes available eight EXC outputs. An output goes true when its flip-flop is set by the EXC decode logic. A function code, provided by the computer as a result of an EXC program instruction, specifies which EXC output flip-flop is set.

EXC output flip-flops are not reset by program instructions alone; they may be reset through a variety of hardware or hardware/software techniques. Some examples of methods for resetting EXC output flip-flops are discussed in Section 2.5.

The EXC output driver is capable of switching signals at levels up to +30 volts, with current sinking of up to 250 mA.

3.3 SENSE DECODE

Every master DOM is capable of sampling, one at a time, up to eight Sense input lines and forwarding the logic level present on the selected line to the computer. A function code, provided by the computer as a result of a SEN program instruction, specifies which Sense input is to be sampled.

Sense input signals are considered lgoically true when they are at 0 Vdc and logically false at +4 Vdc. When sampled, a true input will cause a jump condition in the program. The DOM provides a 5.6 K pullup resistor to +5 volts on each Sense input. It is therefore not necessary to drive the Sense inputs high. The Sense inputs are normally connected to external logic (0 to +5 volts) or switch closures to ground.

> **NOTE**
>
> Sensed signals should not be allowed to go negative with respect to DOM logic ground and should not be allowed to go more positive than the DOM +5 volts.

3.4 LOGIC DESIGN

The basic design of the data output logic is represented in the block diagram of Figure 3-1. Each output register consists of four data output logic devices, each of which contains four TTL/DTL bistable 4-bit latches per device.

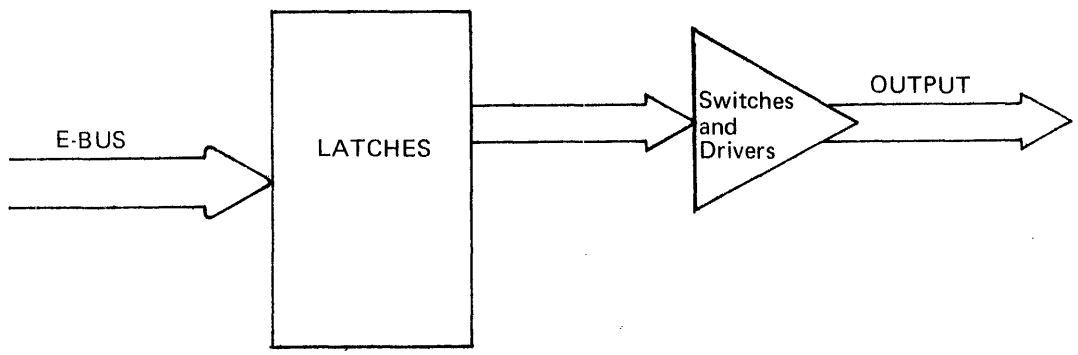


Figure 3-1. Digital Output Logic

Latches

Information present at a data (D) input (see Figure 3-2) is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

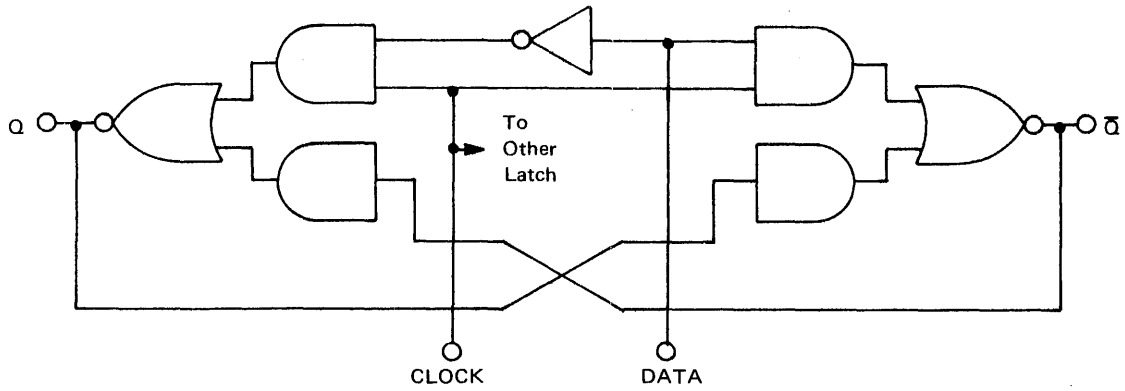


Figure 3-2. Latch - Functional Diagram

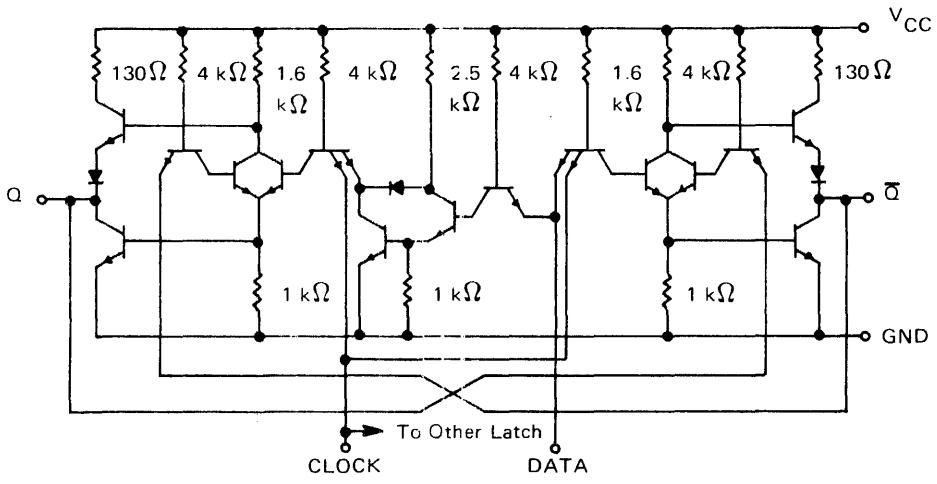


Figure 3-3. Latch - Schematic Diagram

Drivers

The dual peripheral drivers used in the DOM incorporate the following features:

- 300 - mA Output Current Capability
- High-Voltage Outputs
- High-Speed Switching

Typical applications of the drivers include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, and memory drivers. The drivers offer improved freedom from latch-up and diode-clamped inputs for simplified system design. They can drive lamps, relays, and memories to rated levels of voltage and current without external loading capacitors. A schematic diagram of a single driver is shown in Figure 3-4.

Note that although the above specifications and comments apply to the output driver used in the DOM, some caution must be exercised in driver usage. Within the DOM

there is no isolation of the driver grounds from the logic ground of the computer; it is, therefore, recommended that the DOM outputs not be used to switch high-current loads or other loads likely to couple noise into the computer's ground system.

If the DOM is used drive logic, it is recommended that pull-up resistors to +5V be included at the receiving end of the line; the value of the resistor should be 5.6 Kohms (optionally 1 K ohm) maximum, or equal to the characteristic impedance of the line. In this application, total load current should be limited 100 mA.

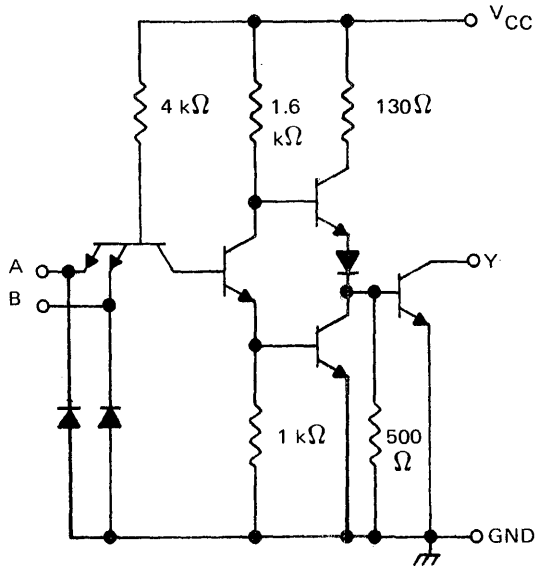


Figure 3-4. Driver - Schematic Diagram

4. INSTALLATION

4.1 PREREQUISITES

Each DOM or DOME requires one card slot in either the mainframe or Memory Expansion/Peripheral Controller frame. No special slots are reserved for use by DOMs; their location in the frame is determined solely by considerations of convenience in backplane wiring.

4.2 INSTALLATION AND INTERCONNECTION

A DOM is installed vertically with its component side to the left in 620/i and 620/L computers, and horizontally with its component side up in the 620/f computer. Figure 4-1 illustrates a typical installation.

The card is installed with the double pin edge pointing toward the installer. Proper orientation of the module is important since the cards are not keyed.

Connection to the computer I/O-bus and the BIC option B-bus is provided through backplane wiring. All pin assignments for the I/O-bus and B-bus are listed in Appendix A.

For each DOM, connections to external instruments include two output registers and one 16-bit gated input and may include up to eight External Control outputs and up to eight Sense inputs. Pin assignments for these connections are also listed in Appendix A. Recommended connector types for J1 and J2 are identified in the summary of key specifications in Appendix B.

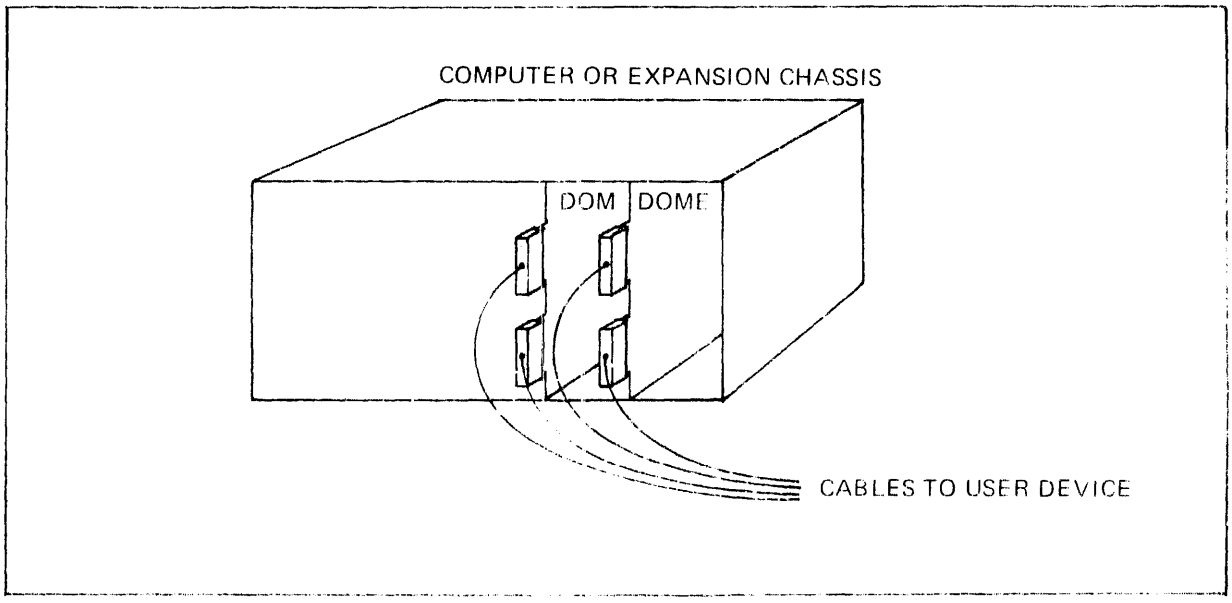


Figure 4-1. Typical Module Installation

Device Address Wiring

Table 4-1 lists the jumper connections required to wire a device address for a master DOM. Note that P1-76 (Enable) is not normally used. It is available, however, and may be used as an additional addressing condition. For example, if multiple master DOM modules have the same device address, the Enable input can be used to permit only one module to respond to that address at a given time.

Table 4-1. Device Address Wiring

Address	Wirewrap Jumpers		
050	P1-72 to P1-71	P1-69 to P1-68	P1-66 to P1-65
051	P1-72 to P1-71	P1-69 to P1-68	P1-66 to P1-64
052	P1-72 to P1-71	P1-69 to P1-67	P1-66 to P1-65
053	P1-72 to P1-71	P1-69 to P1-67	P1-66 to P1-64
054	P1-72 to P1-70	P1-69 to P1-68	P1-66 to P1-65
055	P1-72 to P1-70	P1-69 to P1-68	P1-66 to P1-64
056	P1-72 to P1-70	P1-69 to P1-67	P1-66 to P1-65
057	P1-72 to P1-70	P1-69 to P1-67	P1-66 to P1-64

EXC2 Output Wiring

Table 4-2 lists the jumper connections required to wire the eight EXC2 outputs to select individual registers on the DOM and DOMEs.

Table 4-2. Register Select Connections

SIGNAL	CONNECTION		REGISTER NUMBER
	FROM	TO	
XEXC-0	DOM #1 P1-110	DOM #1 P1-77	1
XEXC-1	DOM #1 P1-112	DOM #1 P1-78	2
XEXC-2	DOM #1 P1-114	DOME #2 P1-77	3
XEXC-3	DOM #1 P1-103	DOME #2 P1-78	4
XEXC-4	DOM #1 P1-104	DOME #3 P1-77	5
XEXC-5	DOM #1 P1-105	DOME #3 P1-78	6
XEXC-6	DOM #1 P1-106	DOME #4 P1-77	7
XEXC-7	DOM #1 P1-108	DOME #4 P1-78	8
DTI-X	DOM #1 P1-63	DOME #2 P1-63	INPUT 2
DTI-X	DOME #2 P1-63	DOME #3 P1-63	INPUT 3
DTI-X	DOME #3 P1-63	DOME #4 P1-63	INPUT 4
DTO-X	DOME #1 P1-102	DOME #2 P1-102	3 & 4
DTO-X	DOME #2 P1-102	DOME #3 P1-102	5 & 6
DTO-X	DOME #3 P1-102	DOME #4 P1-102	7 & 8

External Control Reset Wiring

Provision must be made for resetting External Control outputs. Basic information on techniques for resetting the outputs is presented in Section 2.5. One possible configuration is illustrated in Table 4-3.

Table 4-3. External Control Reset Wiring

Signals	DOM	DOM
EXC1/REX0	J1-6	J1-5
EXC3/REX2	J1-12	J1-11
EXC5/REX4	J1-18	J1-17
EXC7/REX6	J1-24	J1-23

XRDY And X-IN/X-OUT Wiring

DOMs used in conjunction with the BIC option require an externally-supplied signal, XRDY, which synchronizes the data transfer with external device operation. EXC0

and EXC1 are connected to X-OUT and X-IN respectively to select the DOM for connection to the BIC and to establish the direction of data transfer. Further discussion of these requirements can be found in Section 3.1 of this manual.

A wiring configuration for BIC operation under internal program control is shown in Table 4-4. This configuration is used when operating the DOM Test Program as described in Section 2.8 of this manual.

For BIC operation under external control (externally supplied timing for BIC-connected operations), the external pulse is provided through J1-19. The pulse is low true and less than 1.8 microseconds for the 620/L computer.

Table 4-4. DOM Wiring for Program-Controlled BIC Operation

BIC Connections	P1-74 to P1-79 to P1-89 P1-75 to P1-80 to P1-87 --- P1-85 to P1-73

Note that if the BIC is not used, P1-79 and P1-80 should be grounded or, alternatively, P1-79 should be connected to P1-74, and P1-80 should be connected to P1-75.

4.3 INSTALLATION EXAMPLE

A typical DOM could be installed with the following wiring:

Device Address 050

P1-71 wired to P1-72
P1-68 wired to P1-69
P1-65 wired to P1-66

Register Select Connections

P1-110 wired to P1-77
P1-112 wired to P1-78

BIC Control

P1-74 wired to P1-79
P1-75 wired to P1-80

Note: If BIC is not used P1-79 and P1-80 should be grounded.

EXC Reset (These connections will be inside J1 connector hood.)

J1-5 to J1-4
J1-8 to J1-7

APPENDIX A: DOM PIN ASSIGNMENTS

BACKPLANE WIRING

Pin No.	Name	Function
P1-1	Digital ground	
2	EB00	One bit of Device Address or data word
3	Digital ground	
4	EB01	One bit of Device Address or data word
5	Digital ground	
6	EB02	One bit of Device Address or data word
7	Digital ground	
8	EB03	One bit of Device Address or data word
9	Digital ground	
10	EB04	One bit of Device Address or data word
11	EB05	One bit of Device Address or data word
12	EB06	One bit of EXC, EXC2 or SEN code or data word
13	EB07	One bit of EXC, EXC2 or SEN code or data word
14	EB08	One bit of EXC, EXC2 or SEN code or data word
15	EB09	One bit of data word
16	EB10	One bit of data word
17	EB11	EXC tag line or one bit of data word
18	EB12	Sense tag line or one bit of data word
19	EB13	One bit of data word
20	EB14	Data tag line or one bit of data word
21	EB15	EXC2 tag line or one bit of data word
22	Digital ground	
23	Not used	
24	Digital ground	
25	Not used	
26	Digital ground	
27	FRYX	Function Ready
28	Digital ground	
29	DRYX	Data Ready
30	Digital ground	
31	SERX	Sense Response
32	Digital ground	
33	Not used	
34	Digital ground	
35	Not used	

BACKPLANE WIRING (Continued)

Pin No.	Name	Function
P1-36	Digital ground	
37	Not used	
38	Digital ground	
39	Not used	
40	Digital ground	
41	Not used	
42	Not used	
43	SYRT	Resets system logic
44	IUAX	Interrupt acknowledge from computer
45	Not used	
46	Not used	
47	Not used	
48	Digital ground	
49	TRQX	Transfer Request from DOM to BIC
50	TROX	Identifies direction of BIC-controlled data transfer
51	Digital ground	
52	Not used	
53	Digital ground	
54	CDCX	Notifies BIC that DOM is connected
55	Digital ground	
56	DCEX	Connect signal from BIC
57	Digital ground	
58	TAKX	Transfer Request acknowledge from BIC
59	Digital ground	
60	DESX	Disconnect from BIC
61	Not used	
62	Not used	
63	DTI-X	Jumper connection for DTI-X to DOMEs
64	EB00+	Jumper connection for wiring Device Address
65	EB00-	Jumper connection for wiring Device Address
66	EB0I	Jumper connection for wiring Device Address
67	EB01+	Jumper connection for wiring Device Address
68	EB01-	Jumper connection for wiring Device Address
69	EB1I	Jumper connection for wiring Device Address
70	EB02+	Jumper connection for wiring Device Address
71	EB02-	Jumper connection for wiring Device Address
72	EB2I	Jumper connection for wiring Device Address

Pin No.	Name	Function
P1-73	Device Ready	Externally-supplied timing for BIC-connected operations
74	Not used	
75	Not used	
76	Enable	Not used
77	EXC2-N	Jumper connection for EXC2 signal assigned to Register 1
78	EXC2-M	Jumper connection for EXC2 signal assigned to Register 2
79	EPO-N	DOM Select signal for BIC-connected operations
80	Not used	
81	Not used	
82	Not used	
83	Not used	
84	Not used	
85	DTOS	Data transfer request to computer
86	EXC7	Jumper connection for internal use of EXC7
87	EXC5	Jumper connection for internal use of EXC5
88	Not used	
89	Not used	
90	EXC6	Jumper connection for internal use of EXC6
91	EXC2	Jumper connection for internal use of EXC2
92	Not used	
93	EXC3	Jumper connection for internal use of EXC3
94	EXC4	Jumper connection for internal use of EXC4
95	Not used	
96	Not used	
97	Not used	
98	EXC1	Jumper connection for internal use of EXC1
99	Not used	
100	Digital ground	
101	EXC0	Jumper connection for internal use of EXC0
102	DTO-X	Jumper connection for DTO-X signal to DOMEs
103	EXC2-3	Jumper connection for register Select line 3
104	EXC2-4	Jumper connection for register Select line 4
105	EXC2-5	Jumper connection for register Select line 5
106	EXC2-6	Jumper connection for register Select line 6
107	Not used	

BACKPLANE WIRING (Continued)

Pin No.	Name	Function
P1-108	EXC2-7	Jumper connection for register Select line 7
109	Not used	
110	EXC2-0	Jumper connection for register Select line 0
111	Not used	
112	EXC2-1	Jumper connection for register Select line 1
113	Not used	
114	EXC2-2	Jumper connection for register Select line 2
115	Not used	
116	Not used	
117	Not used	
118	+5 Vdc	
119	Not used	
120	Not used	
121	+5 Vdc	
122	Digital ground	

TERMINAL EDGE CONNECTOR WIRING

Pin No.	Name	Function
J1-1	DTIN	Data Transfer In
2	+5 Vdc	
3	EXC0	Output connection for EXC0
4	Digital ground	
5	REX0	Jumper connection for EXC0 reset
6	EXC1	Output connection for EXC1
7	Digital ground	
8	REX1	Jumper connection for EXC1 reset
9	EXC2	Output connection for EXC2
10	Digital ground	
11	REX2	Jumper connection for EXC2 reset
12	EXC3	Output connection for EXC3
13	Digital ground	
14	REX3	Jumper connection for EXC3 reset
15	EXC4	Output connection for EXC4
16	Digital ground	
17	REX4	Jumper connection for EXC4 reset
18	EXC5	Output connection for EXC5
19	Device Ready	External connection for BIC operation
20	REX5	Jumper connection for EXC5 reset
21	EXC6	Output connection for EXC6
22	Digital ground	
23	REX6	Jumper connection for EXC6 reset

TERMINAL EDGE CONNECTOR WIRING (Continued)

Pin No.	Name	Function
J1-24	EXC7	Output connection for EXC7
25	REX7	Jumper connection for EXC7 reset
26	Sense 0	Input connection for Sense 0 line
27	Sense 1	Input connection for Sense 1 line
28	Sense 2	Input connection for Sense 2 line
29	DIN 00	Input word, bit 0, LSB
30	DIN 01	Input word, bit 1
31	DIN 02	Input word, bit 2
32	DIN 03	Input word, bit 3
33	DIN 04	Input word, bit 4
34	DIN 05	Input word, bit 5
35	DIN 06	Input word, bit 6
36	DIN 07	Input word, bit 7
37	DIN 08	Input word, bit 8
38	DIN 09	Input word, bit 9
39	DIN 10	Input word, bit 10
40	DIN 11	Input word, bit 11
41	DIN 12	Input word, bit 12
42	DIN 13	Input word, bit 13
43	DIN 14	Input word, bit 14
44	DIN 15	Input word, bit 15, MSB
J2-1	DOA 00	Register 1 output word, bit 0, LSB
2	DOA 01	Register 1 output word, bit 1
3	DOA 02	Register 1 output word, bit 2
4	DOA 03	Register 1 output word, bit 3
5	DOA 04	Register 1 output word, bit 4
6	DOA 05	Register 1 output word, bit 5
7	DOA 06	Register 1 output word, bit 6
8	DOA 07	Register 1 output word, bit 7
9	DOA 08	Register 1 output word, bit 8
10	DOA 09	Register 1 output word, bit 9
11	DOA 10	Register 1 output word, bit 10
12	DOA 11	Register 1 output word, bit 11
13	DOA 12	Register 1 output word, bit 12
14	DOA 13	Register 1 output word, bit 13
15	DOA 14	Register 1 output word, bit 14
16	DOA 15	Register 1 output word, bit 15, MSB
17	DOB 00	Register 2 output word, bit 0, LSB
18	DOB 01	Register 2 output word, bit 1

TERMINAL EDGE CONNECTOR WIRING (Continued)

Pin No.	Name	Function
J2-19	DOB 02	Register 2 output word, bit 2
20	DOB 03	Register 2 output word, bit 3
21	DOB 04	Register 2 output word, bit 4
22	DOB 05	Register 2 output word, bit 5
23	DOB 06	Register 2 output word, bit 6
24	DOB 07	Register 2 output word, bit 7
25	DOB 08	Register 2 output word, bit 8
26	DOB 09	Register 2 output word, bit 9
27	DOB 10	Register 2 output word, bit 10
28	DOB 11	Register 2 output word, bit 11
29	DOB 12	Register 2 output word, bit 12
30	DOB 13	Register 2 output word, bit 13
31	DOB 14	Register 2 output word, bit 14
32	DOB 15	Register 2 output word, bit 15, MSB
33	Sense 3	Input connection for Sense 3 line
34	Sense 4	Input connection for Sense 4 line
35	Sense 5	Input connection for Sense 5 line
36	Sense 6	Input connection for Sense 6 line
37	Sense 7	Input connection for Sense 7 line
38	DTOA	Data Transfer Out, Register 1
39	Digital ground	
40	Digital ground	
41	+5 Vdc	
42	Digital ground	
43	Digital ground	
44	DTOB	Data Transfer Out, Register 2

APPENDIX B: SPECIFICATIONS

DIGITAL OUTPUT

Number	Two 16-bit registers.
Type	Open collector transistor with 5.6 K ohms (1 K ohms, optional) to +5 Vdc. Sinks current when true. Capable of sinking 300 mA. Load pulses (DTOA and DTOB) are externally available; these pulses are 200 nanoseconds in duration, low true.
Available Fanout	30 logic loads.
Maximum Load Capacitance	100 pF.

DIGITAL INPUT

Number	16 lines gated.
Type	One logic load with 5.6 K ohms (1 K ohm, optional) to +5 Vdc. Low true. Enable Gate (DTIN) is externally available. This signal is 1.9 microseconds in duration, low true.
DTIN Available Fanout	16 logic loads.
DTIN Maximum Load Capacitance	1000 pF. This signal is true when input data is gated onto the computer E-bus.

DIGITAL CONTROL OUTPUTS

Number	Eight.
Type	TI SN7545IP Dual Peripheral Driver; sinks current when true. Each output will sink 300 mA and standsoff +30 V. Each EXC sets an R-S type flip-flop, which results in a dc logic low true output. Each flip-flop has an

DIGITAL CONTROL OUTPUTS (Continued)

Type	externally available reset input, 1 logic load, with 5.6 K ohms (1 K ohms, optional) to +5 Vdc. Reset input may be grounded for pulse operation or may be connected to an EXC for computer control of reset.

DIGITAL SENSE INPUTS

Number	Eight.
Type	TTL logic levels. Ground true, open circuit inputs are held to +5V supply through 5.6 K ohm resistors (1 K ohm, optional).

SPARE GATES

Number	Two.
Type	NOR gates are provided to accommodate special additional logic requirements.

POWER	+5 Vdc $\pm$1%, 1A.

TEMPERATURE RANGE

Operating	-10°C to 50°C
Storage	-55°C to 85°C

PHYSICAL CHARACTERISTICS

Dimensions	One printed circuit board 7-3/4 x 12 x 1/2 inches.
Connectors	One 122-terminal card edge connector. Two 44-terminal card edge connectors.

APPENDIX C: DRIVER PROGRAM EXAMPLES

```
PAGE    1 DASG  05/07/73

                      1 *       TEST DOM - PROGRAM CONTROL INPUT AND OUTPUT
001000                2         ORG       01000
        004012        3 PDOM    EQU       04012
                      4 *
                      5 *
                      6 *
001000 002000         7 PDRO    CALL      PDOM,DOMNR,OUT,NUM,OBUF,ERROR
001001 004012
001002 001030 R
001003 001031 R
001004 001033 R
001005 001200 R
001006 001025 R
001007 002000         8         CALL      PDOM,DOMNR,IN,NUM,IBUF,ERROR
001010 004012
001011 001030 R
001012 001032 R
001013 001033 R
001014 001034 R
001015 001025 R
001016 001100         9         JSS1      *+4
001017 001022 R
001020 001000        10         JMP       PDRO
001021 001000 R
001022 000001        11         HLT       01
001023 001000        12         JMP       PDRO
001024 001000 R
001025 000077        13 ERROR   HLT       077
001026 001000        14         JMP       PDRO
001027 001000 R
001030 000011        15 DOMNR   DATA      9           DOM  SELECT CODE
001031 000000        16 OUT     DATA      0
001032 000001        17 IN      DATA      1
001033 000001        18 NUM     DATA      1           NUMBER OF WORDS
001034               19 IBUF    BSS       100         INPUT BUFFER
001200               20 OBUF    BSS       100         OUTPUT BUFFER
        000000       21         END
```

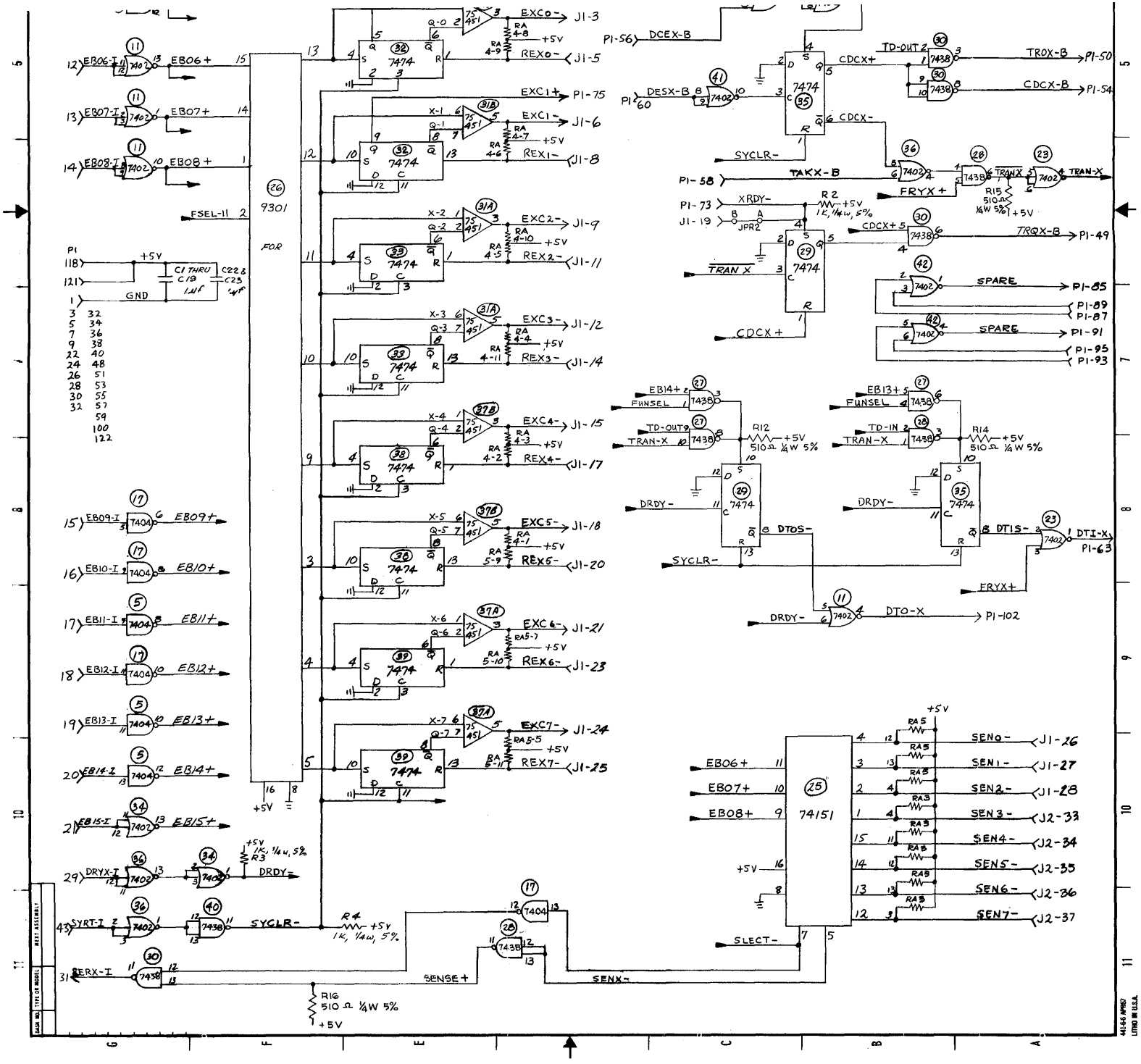
```
PAGE    1 DASG  05/07/73

                        1 *       TEST DDM - DIRECT ACCESS CONTROL (BIC) MODE
                        2 *
002000                  3         ORG     02000
        004144          4 DDDM    EQU     04144
        004367          5 SDDM    EQU     04367
002000 002000           6 DDRO    CALL    DDDM,BICNR,DOMNR,OUT,NUM,OBUF,ERROR
002001 004144
002002 002036 R
002003 002037 R
002004 002040 R
002005 002042 R
002006 002207 R
002007 002033 R
002010 002000           7         CALL    BICW          GO WAIT BIC COMPLETE
002011 002353 R
002012 002000           8         CALL    DDDM,BICNR,DOMNR,IN,NUM,IBUF,ERROR
002013 004144
002014 002036 R
002015 002037 R
002016 002041 R
002017 002042 R
002020 002043 R
002021 002033 R
002022 002000           9         CALL    BICW
002023 002353 R
002024 001100          10         JSR1    *+4
002025 002030 R
002026 001000          11         JMP     DDRO
002027 002000 R
002030 000003          12         HLT     3             HALT AFTER INPUT - OUTPUT
002031 001000          13         JMP     DDRO
002032 002000 R
002033 000001          14 ERROR   HLT     1
002034 001000          15         JMP     DDRO
002035 002000 R
002036 000001          16 BICNR   DATA    1
002037 000011          17 DOMNR   DATA    9             =051 SELECT
002040 000000          18 OUT     DATA    0
002041 000001          19 IN      DATA    1
002042 000001          20 NUM     DATA    1             NUMBER OF WORDS  TRANSFERED
002043                 21 IBUF    BSS     100           INPUT BUFFER
002207                 22 OBUF    BSS     100           OUTPUT BUFFER
                       23 *
```

```
                    24 *        BICW    BIC WAIT SUBROUTINE
                    25 *
002353 000000       26 BICW     ENTR    0
002354 002000       27          CALL    $DOM,BICS   GO WAIT BIC COMPLETE
002355 004367
002356 002376 R
002357 012376       28          LDA     BICS
002360 001010       29          JAZ     BICW+1      BIC STILL BUSY
002361 002354 R
002362 004341       30          LSRA    1
002363 001010       31          JAZ     *+4
002364 002367 R
002365 001000       32          JMP     ERROR       BIC ABNORMAL STOP
002366 002033 R
002367 001200       33          JSS2    *+4
002370 002373 R
002371 001000       34          JMP*    BICW
002372 102353 R
002373 000002       35          HLT     2           CONDITIONAL HALT
002374 001000       36          JMP     DDRO        RESTART
002375 002000 R
002376 000000       37 BICS     DATA    0
       000000       38          END
```

APPENDIX D: SCHEMATICS, ASSEMBLIES, AND PARTS LISTS

Digital I/O Module 03-950111


EB06+
EB07+
EB08+
EB09+
EB10+
EB11+
EB12+
EB13+
EB14+
EB15+
DRYX-I
SYRT-I
SERX-I
FSEL-11
9301
FOR
P1
+5V
GND
C1 THRU C19 1uf
C22 & C23 4uf
3 32
5 34
7 36
9 38
22 40
24 48
26 51
28 53
30 55
32 57
59
100
122
EXC0-
REX0-
EXC1+
EXC1-
REX1-
EXC2-
REX2-
EXC3-
REX3-
EXC4-
REX4-
EXC5-
REX5-
EXC6-
REX6-
EXC7-
REX7-
R3 1K, 1/4w, 5%
DRDY-
R4 1K, 1/4w, 5%
SYCLR-
SENSE+
SENX-
R16 510 Ω 1/4W 5%
DESX-B
DCEX-B
CDCX+
CDCX-
TD-OUT
TROX-B
CDCX-B
TAKX-B
FRYX+
TRANX
TRAN-X
XRDY-
R2 1K, 1/4w, 5%
JPR2
TRQX-B
SPARE
R15 510Ω 1/4W 5%
EB14+
EB13+
FUNSEL
TD-IN
R12 510Ω 1/4W 5%
R14 510Ω 1/4W 5%
DRDY-
DTOS-
DTIS-
DTI-X
DTO-X
SYCLR-
74151
SEN0-
SEN1-
SEN2-
SEN3-
SEN4-
SEN5-
SEN6-
SEN7-
SLECT-
RA5
RA3
RA4
RA1
RA2
+5V
GND
TRAN-X
DRDY-
SYCLR-
DTOS-
DTIS-
DTO-X
FRYX+
TRANX
TRAN-X
SPARE
SPARE
P1-56
P1-60
P1-58
P1-73
J1-19
P1-50
P1-54
P1-49
P1-85
P1-89
P1-87
P1-91
P1-95
P1-93
P1-63
P1-102
J1-3
J1-5
J1-6
J1-8
J1-9
J1-11
J1-12
J1-14
J1-15
J1-17
J1-18
J1-20
J1-21
J1-23
J1-24
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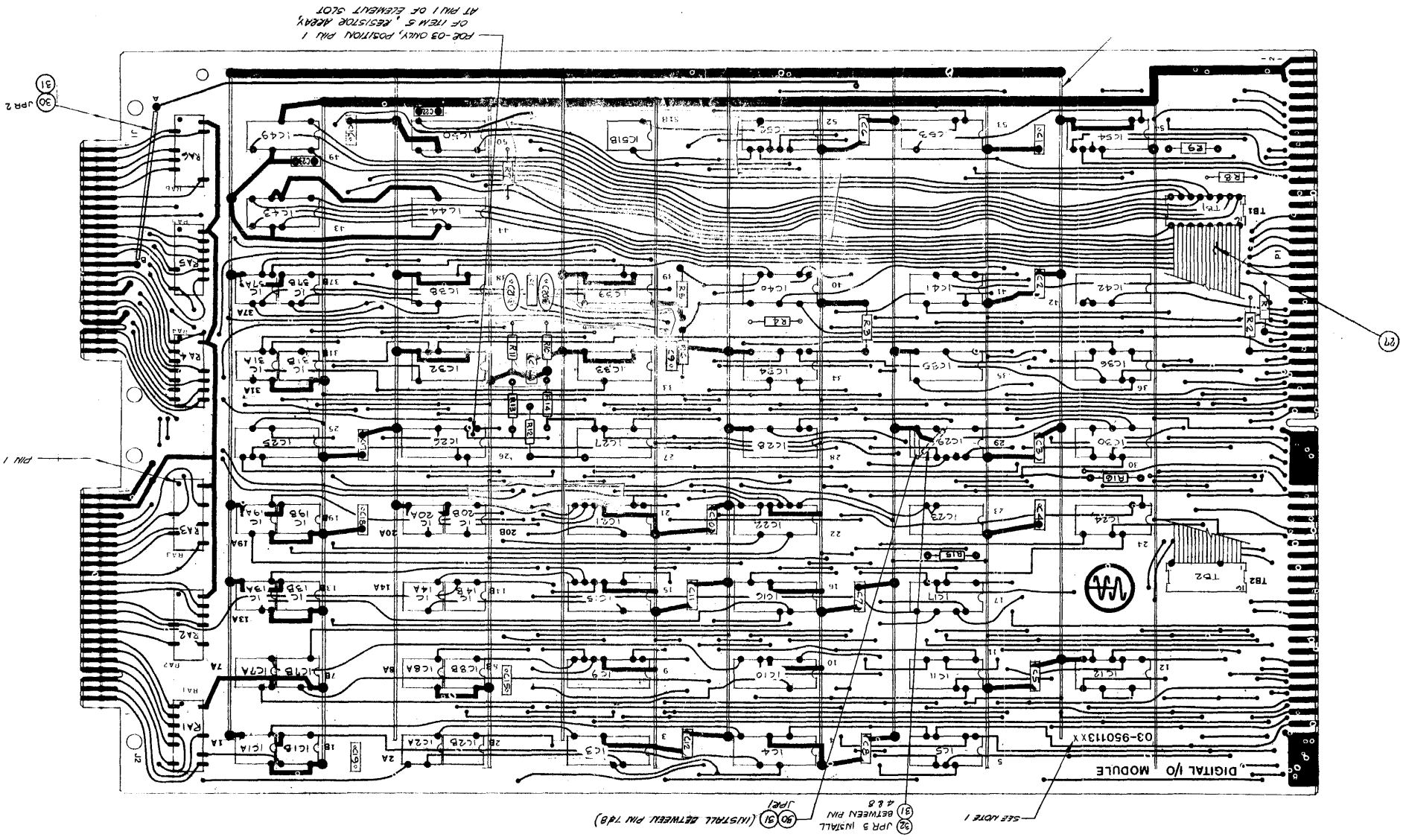
J2-33
J2-34
J2-35
J2-36
J2-37


FOR 03 ONLY, POSITION PIN 1 OF ITEM 5 , RESISTOR ARRAY, AT PIN 1 OF ELEMENT SLOT
PIN 1 (TYPICAL)
DIGITAL I/O MODULE
03-950113XX
SEE NOTE 1
JPR 3 INSTALL BETWEEN PIN 4 & 5
(INSTALL BETWEEN PIN 1&8 JPR1)
JPR 2

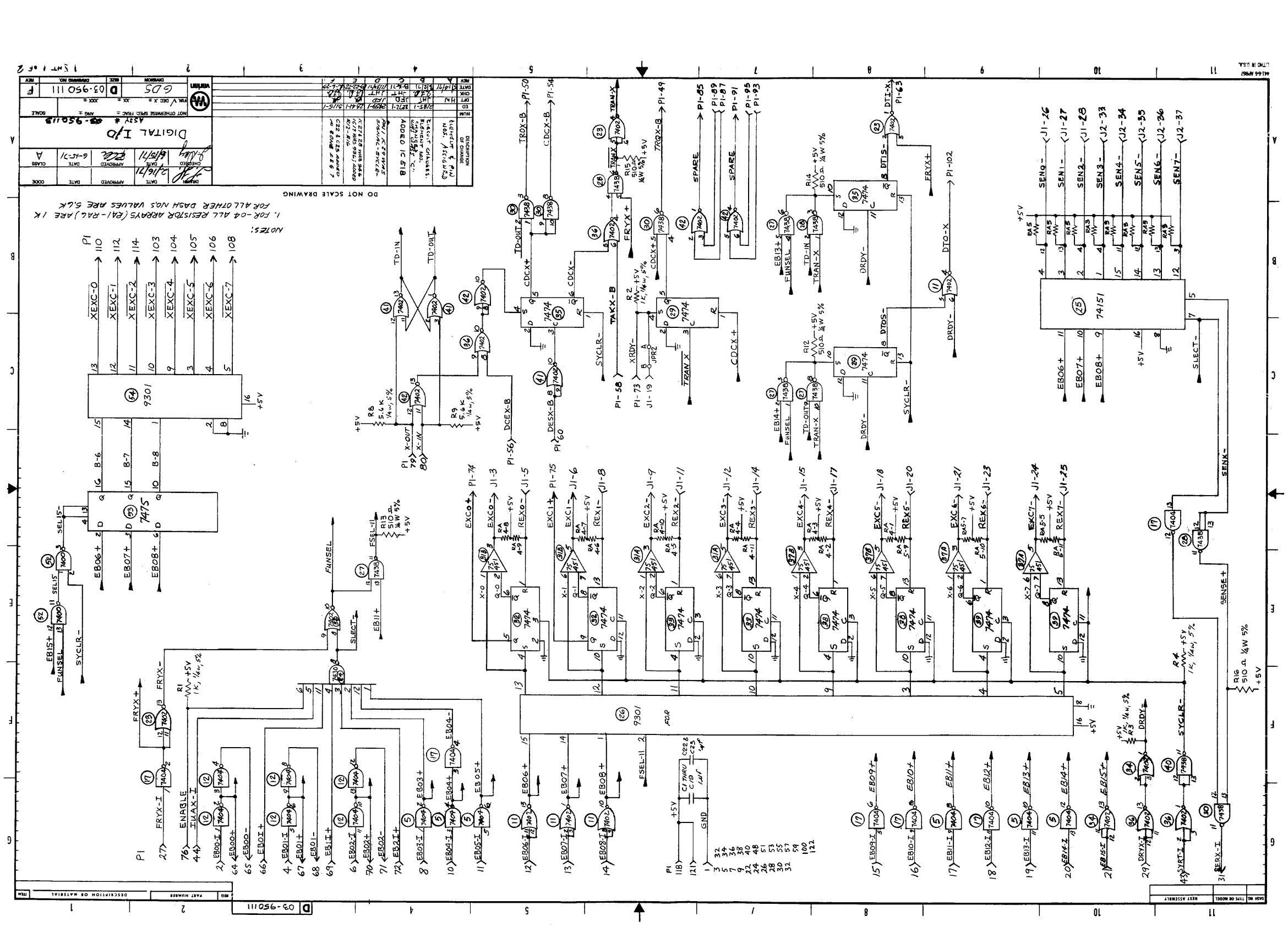
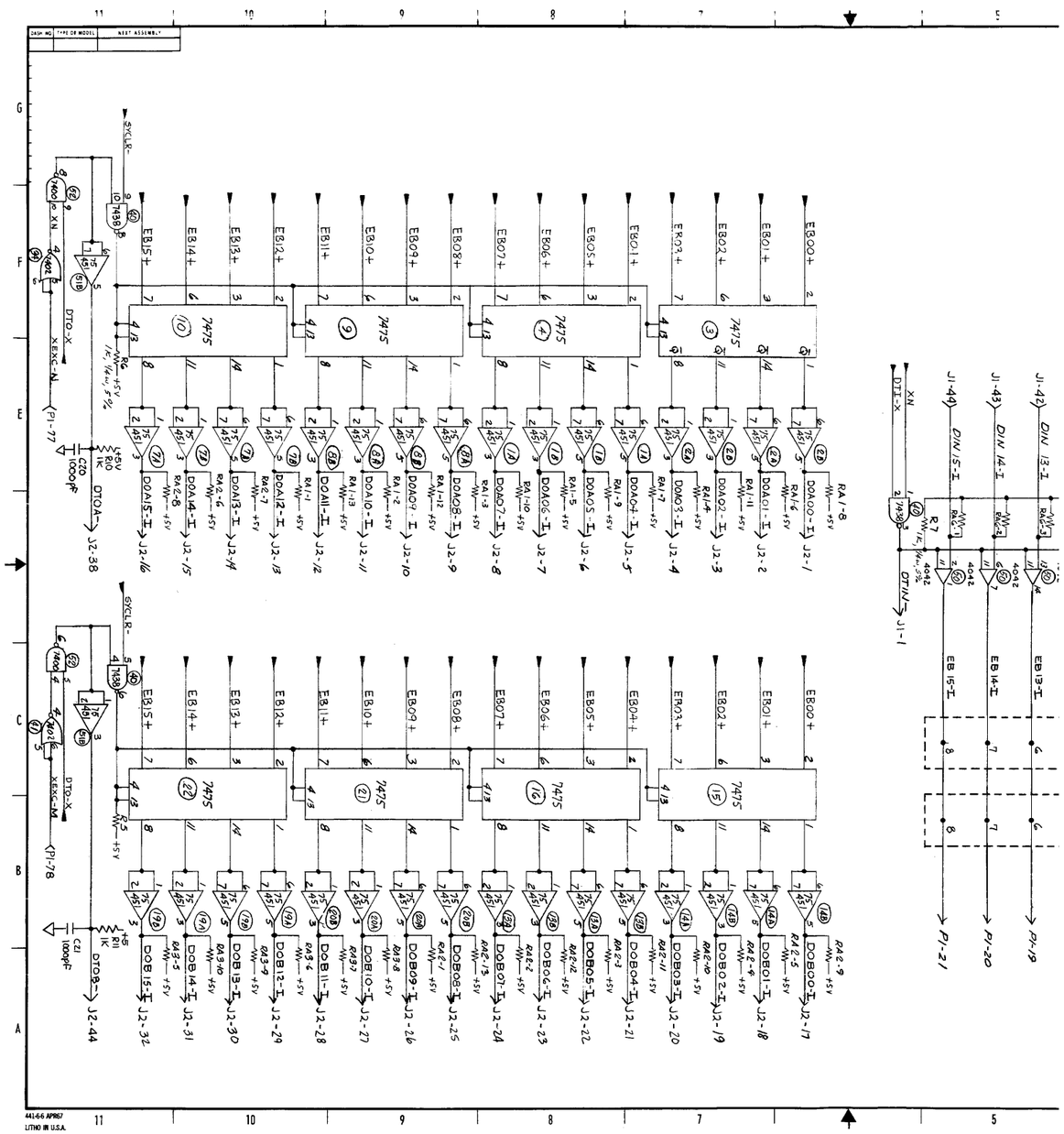

DIGITAL I/O
A5YY # 03-950111
D 03-950111
GDS
DO NOT SCALE DRAWING
1. FOR -04 ALL RESISTOR ARRAYS (RA1-RA6) ARE 1K
FOR ALL OTHER DASH NOS. VALUES ARE 5.1K
NOTES:
P1
TD-IN
TD-OUT
EXC0- EXC1- EXC2- EXC3- EXC4- EXC5- EXC6- EXC7-
9301
7475
7414
7474
7451
7438
7439
7404
7402
7400
74151
+5V
ENABLE
FRYX-I
FRYX+
TRAX-I
SYCLR-
SELECT-
FUNSEL
DRDY-
DRDY+
SYRT-I
SERX-I
SENSE+
SENSE-
EB00+ EB01+ EB02+ EB03+ EB04+ EB05+ EB06+ EB07+ EB08+
EB09+ EB10+ EB11+ EB12+ EB13+ EB14+ EB15+
SEN0- SEN1- SEN2- SEN3- SEN4- SEN5- SEN6- SEN7-
REX0- REX1- REX2- REX3- REX4- REX5- REX6- REX7-
EXC0+ EXC1+ EXC2+ EXC3+ EXC4+ EXC5+ EXC6+ EXC7+
TRDX-B
CDCX-B
DESX-B
TAXX-B
TRAX+
CDCX+
CDCX-
DESX-B
DCEX-B
TRAX-X
CDCX+
SPARE
FRYX+
DTO-X
DTI-X
DTOS-
DTIS-
EB13+
EB14+
TD-IN
TD-OUT
TRAN-X
FUNSEL
DRDY-
SYCLR-
XRDY-
JPR2
TRAN-X
X-OUT
X-IN
R1 1K, 1/4W, 5%
R2 1K, 1/4W, 5%
R4 1K, 1/4W, 5%
R5 4.7K, 1/4W, 5%
R8 5.1K 1/4W, 5%
R9 5.1K 1/4W, 5%
R10 910Ω 1/4W 5%
R12 510Ω 1/4W 5%
R14 510Ω 1/4W 5%
R15 510Ω 1/4W 5%
RA1 4.9K
RA2 4.8K
RA3 4.7K
RA4 4.6K
RA5 4.5K
RA6 4.4K
C1 MICRO FARAD 10V
C22,23 .1μF
GND
P1-50 P1-54 P1-49 P1-85 P1-89 P1-87 P1-91 P1-93 P1-95 P1-102 P1-74 P1-56 P1-58 P1-73 P1-60 P1-75
J1-26 J1-27 J1-28 J2-33 J2-34 J2-35 J2-36 J2-37
J1-3 J1-5 J1-6 J1-8 J1-9 J1-11 J1-12 J1-14 J1-15 J1-17 J1-18 J1-20 J1-21 J1-23 J1-24 J1-25
B-6 B-7 B-8

FIGURE NO. 1

Digital I/O Module Assembly, 03-950113

Schematic Reference	Description	Varian Part No.
RA1-RA6, RA4-RA6 RA1-RA3, 5, 6, & IC26	Resistor, Array, 5.6K	03-998011
IC1A, IB, 2A, 2B, 7A, 8A, 8B, 13A, 13B, 14A, 14B, 19A, 19B, 20A, 20B, 31A, 31B, 37A, 37B, 51B	IC Element 75451	62-600260
IC3, 4, 9, 10, 15, 16, 21, 22, 53	IC Element 7475N	62-600351
IC30, 40, 27, 28	IC Element 7438	62-600294
IC25	IC Element 74151	62-600270
IC26, IC54	IC Element 9301	62-600400
IC29, 32, 33, 35, 38, 39	IC Element 7474	62-600365
IC11, 23, 34, 36, 41, 42	IC Element 7402	62-600356
IC24	IC Element 7430	62-600359
IC5, 12, 17	IC Element 7404	62-600013
IC52	IC Element 7400	62-600355
IC43, 44, 49, 50	IC Element 4042	62-600316



50113

Varian Part No.

03-998011	
62-600260	
62-600351	
62-600294	
62-600270	
62-600400	
62-600365	
62-600356	
62-600359	
62-600013	
62-600355	
62-600316	

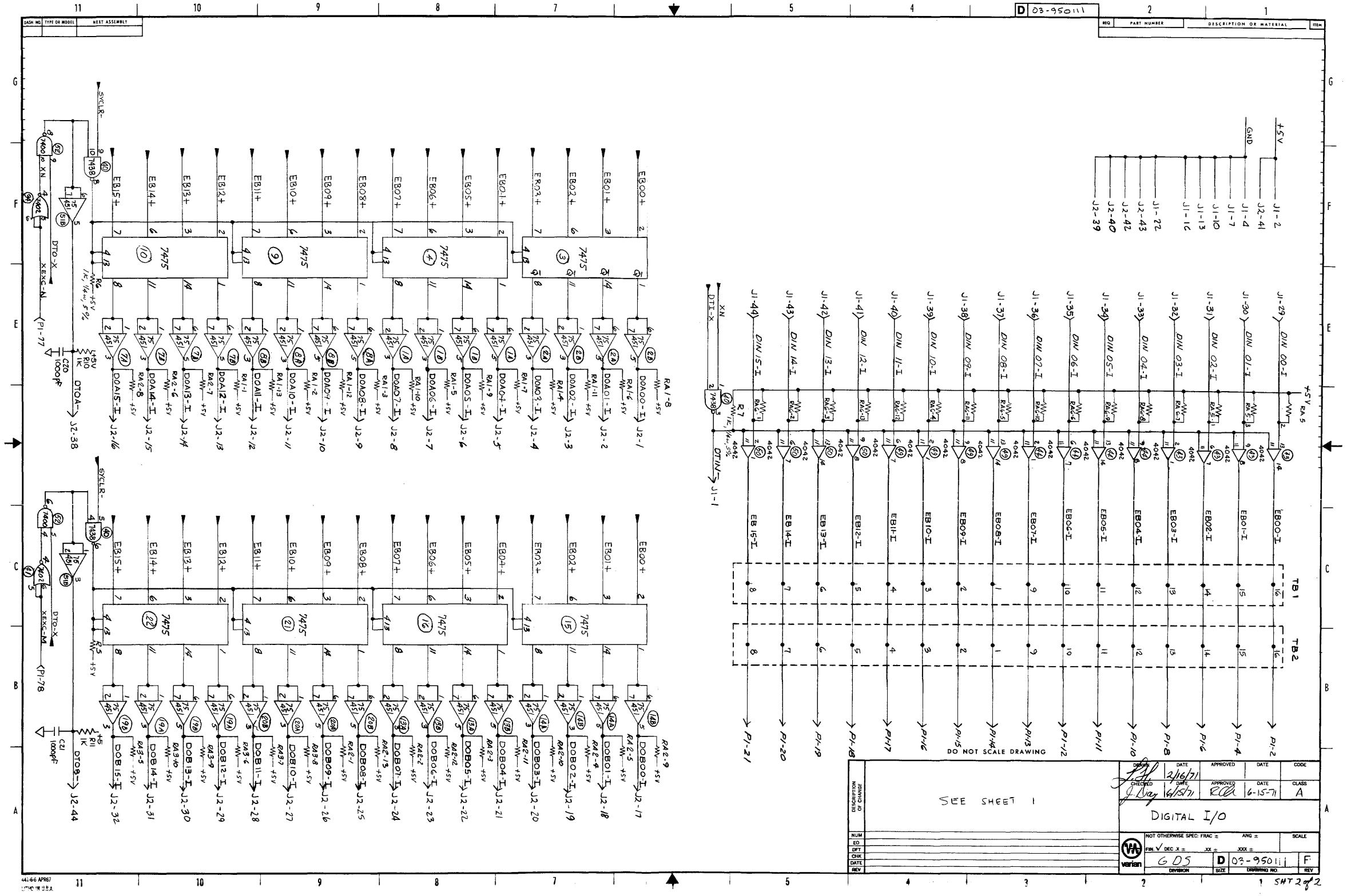


FIGURE NO. 2