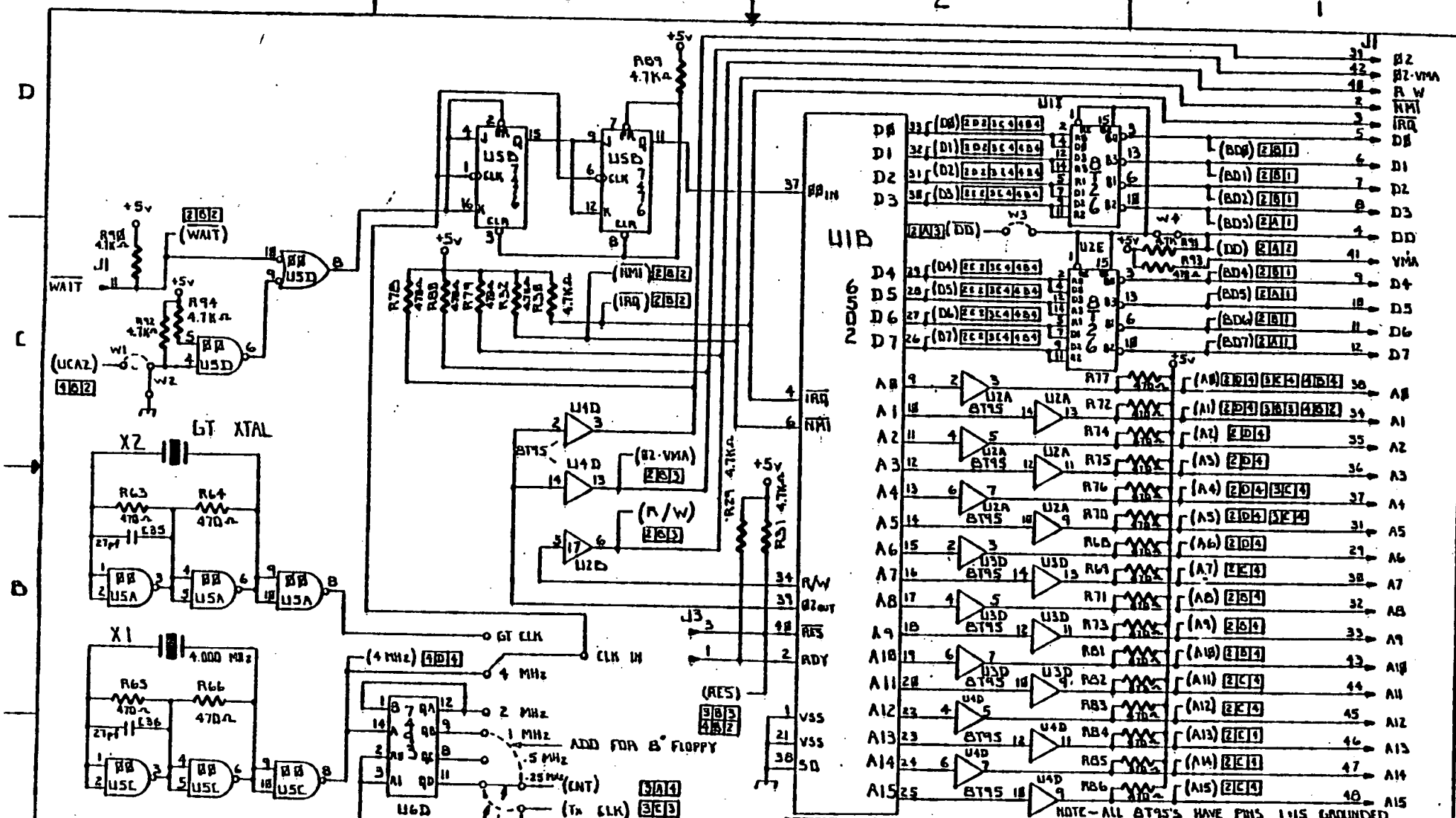
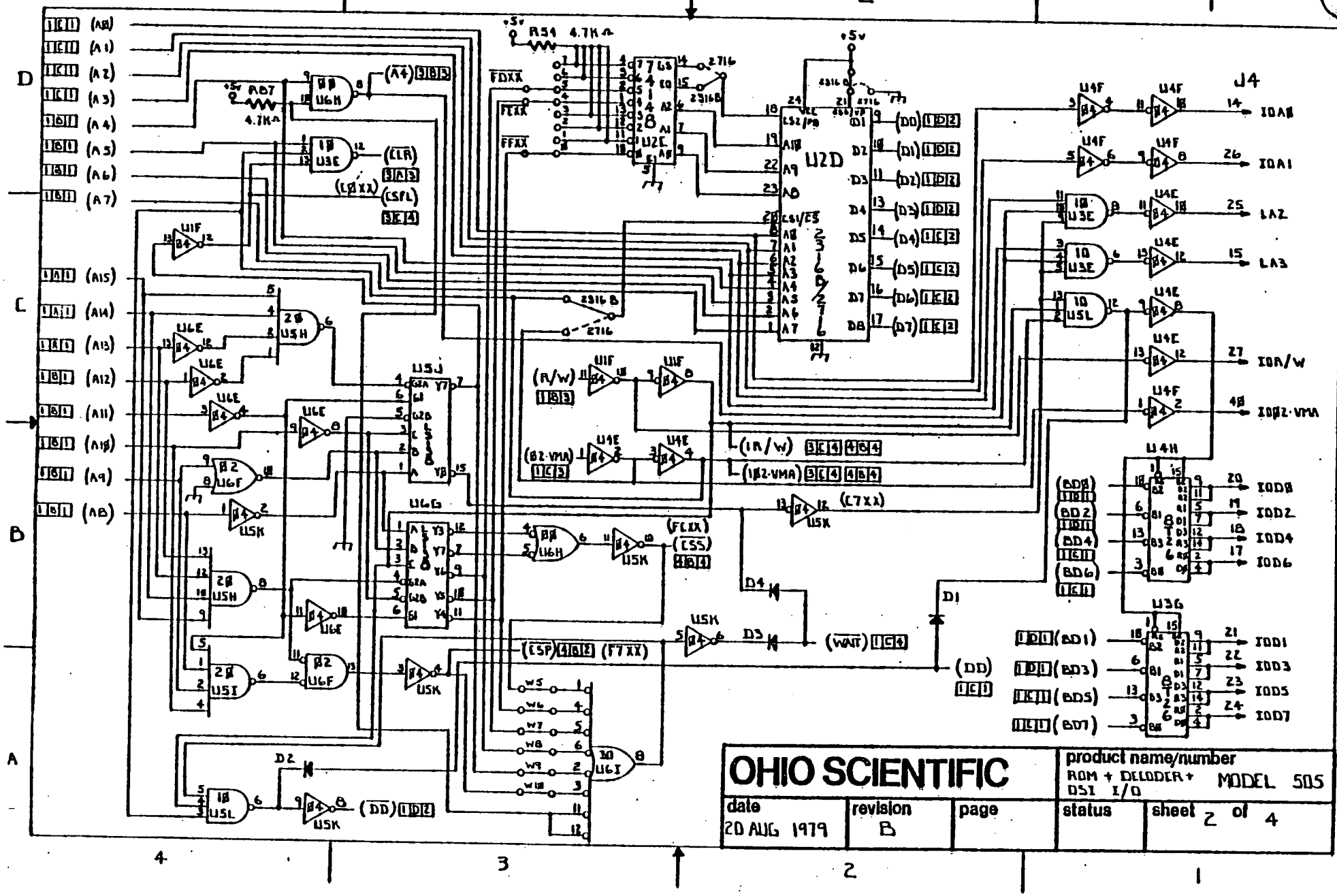
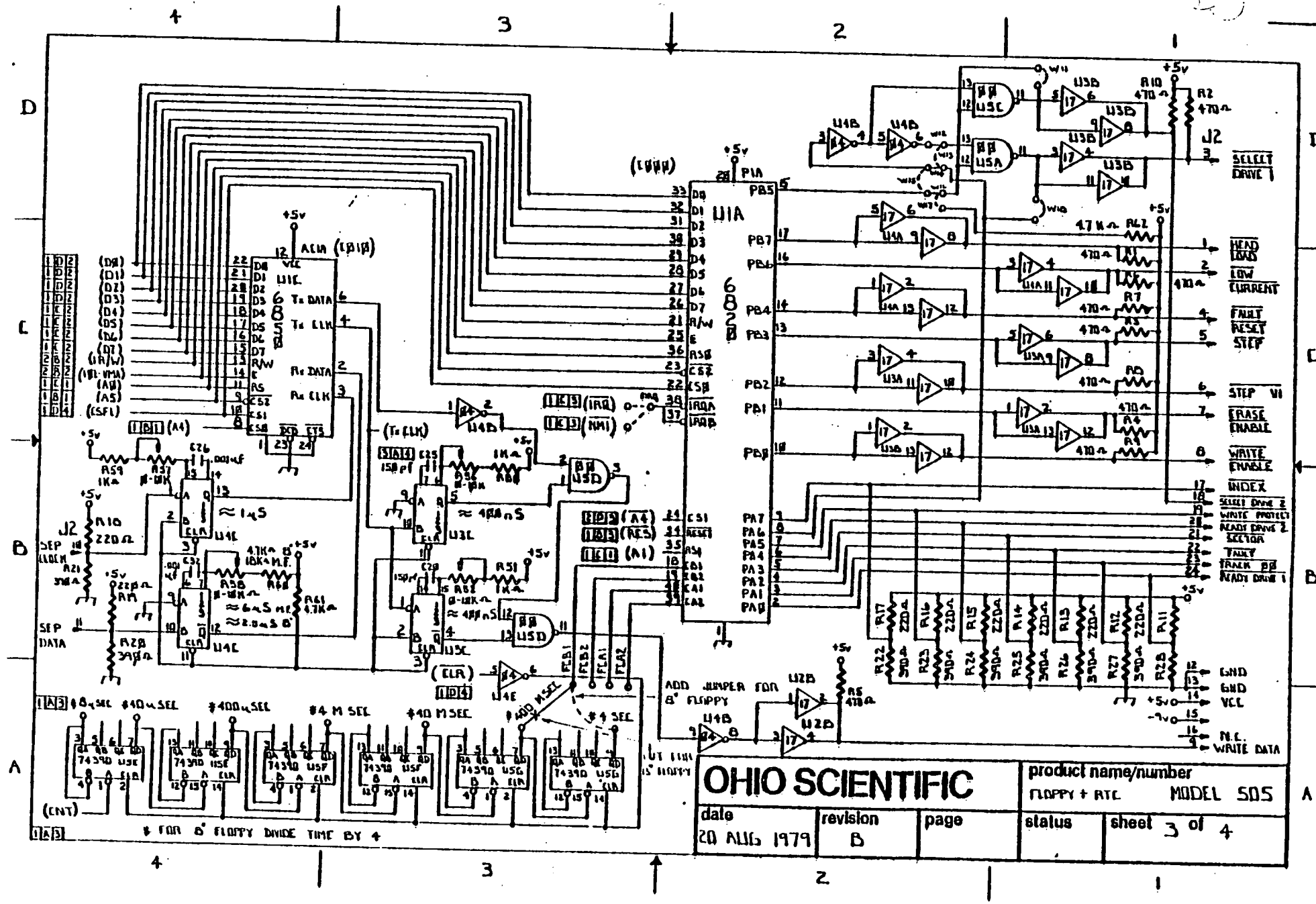


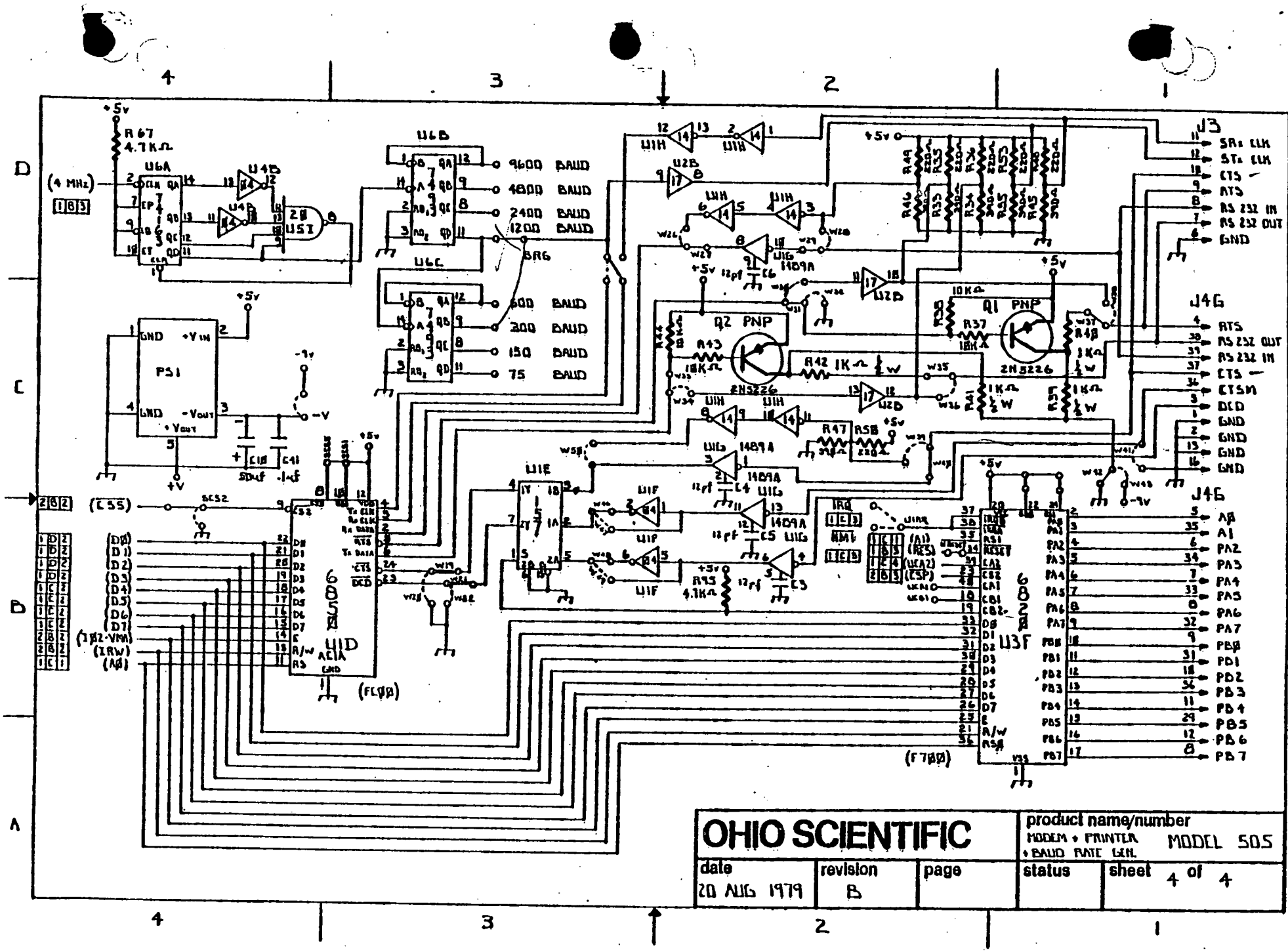
OHIO SCIENTIFIC			product name/number CPU AND DSC. MODEL 505	
date 20 AUG 1979	revision B	page	status	sheet 1 of 4



OHIO SCIENTIFIC			product name/number: ROM + DECODER + DSI I/O — MODEL 505	
date: 20 AUG 1979	revision: B	page:	status:	sheet 2 of 4



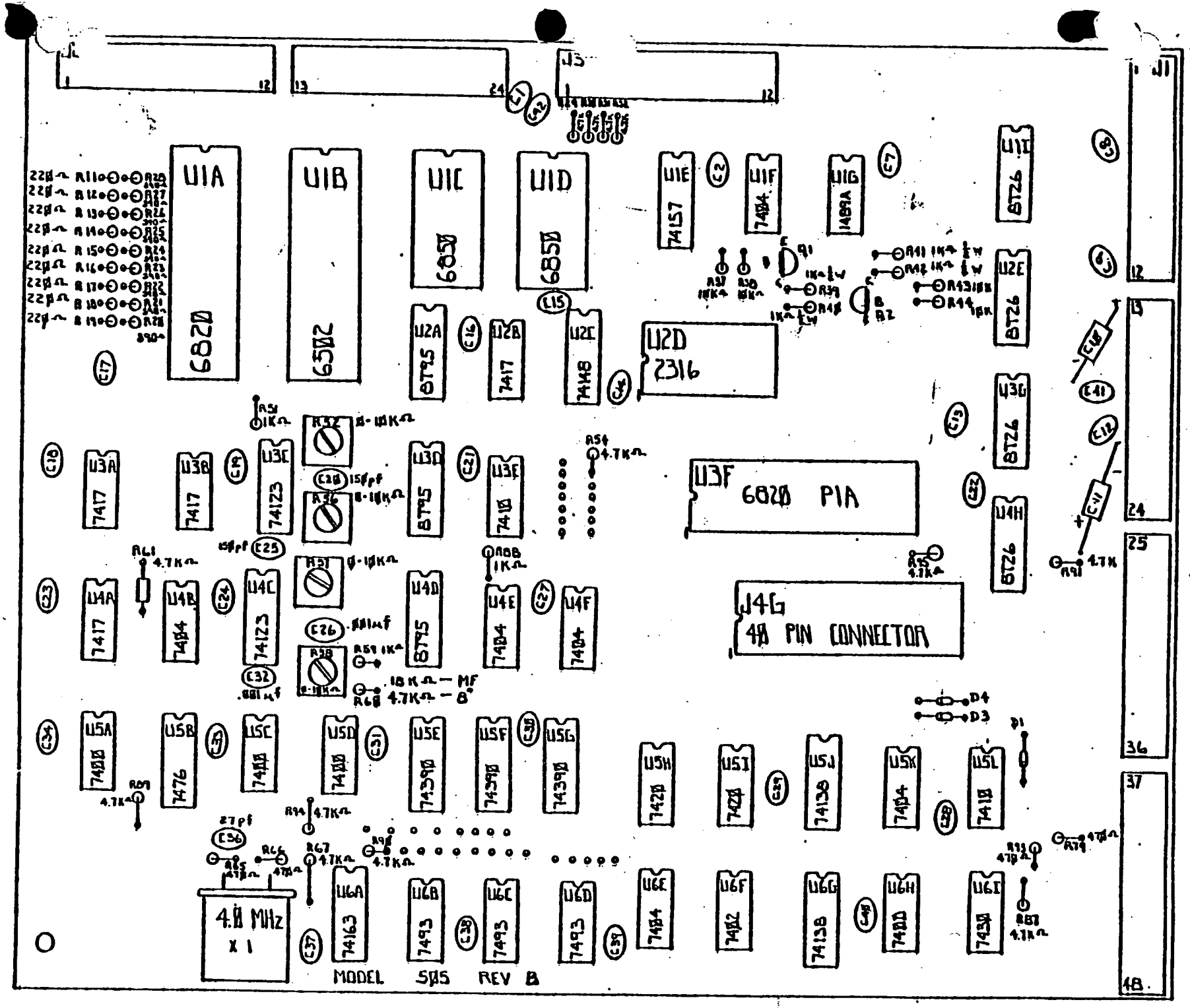
OHIO SCIENTIFIC
product name/number
FLOPPY + RTC
MODEL 505
date
20 AUG 1979
revision
B
page
status
sheet 3 of 4
SELECT DRIVE 1
HEAD LOAD
LOW CURRENT
FAULT RESET
STEP
STEP V1
ERASE ENABLE
WRITE ENABLE
INDEX
SELECT DRIVE 2
WRITE PROTECT
READY DRIVE 2
SECTOR
FAULT
TRACK 00
READY DRIVE 1
GND
GND
VCC
N.C.
WRITE DATA
ADD JUMPER FOR 8" FLOPPY
* FOR 8" FLOPPY DIVIDE TIME BY 4
SEP CLOCK
SEP DATA

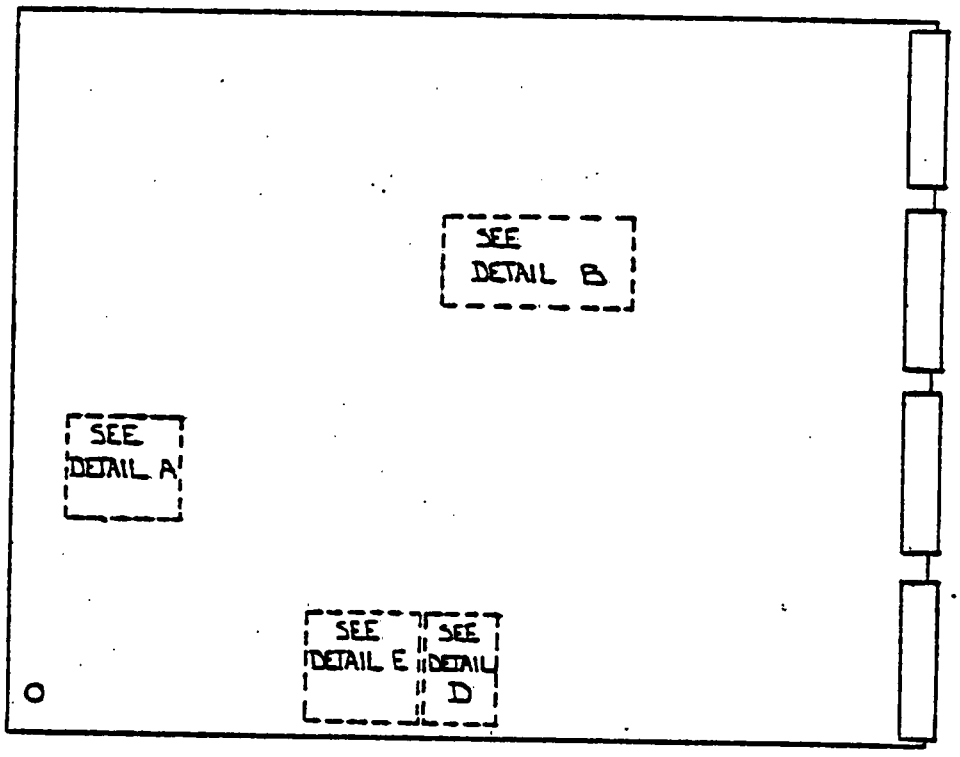


OHIO SCIENTIFIC			product name/number MODEM + PRINTER + BAUD RATE GEN. MODEL 505	
date 20 AUG 1979	revision B	page	status	sheet 4 of 4

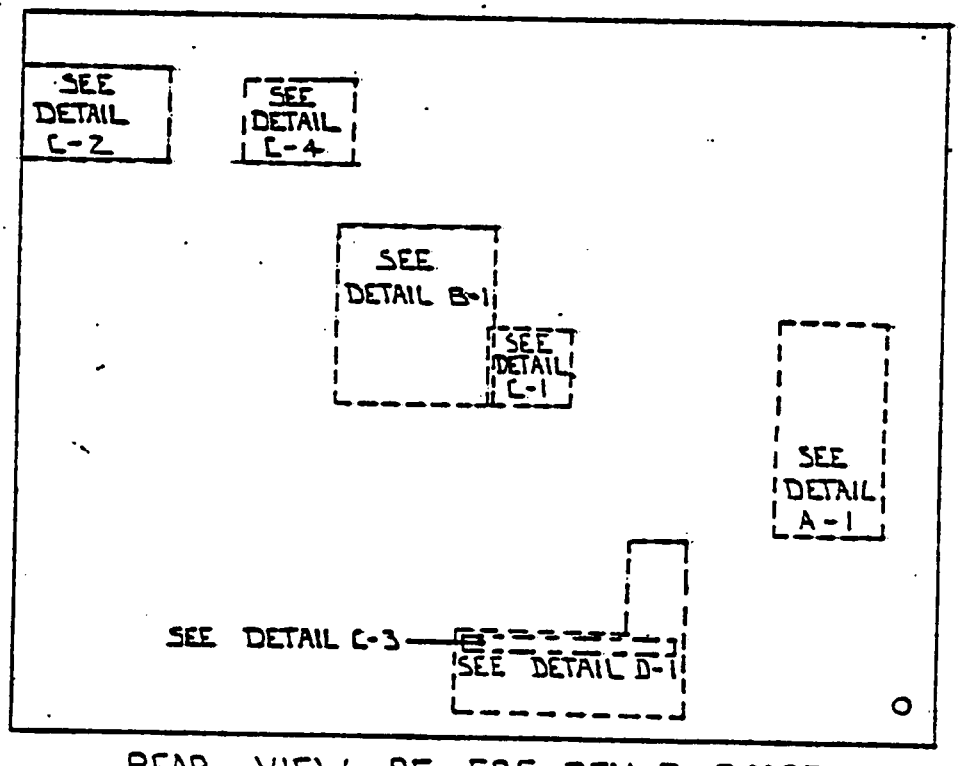
Signal Names Used on 505 Board

Signal Name	Description
A0-A15	Address lines 0 through 15
$\overline{A4}$	Inverted address bit 4 from BUS (low true)
#BAUD	All baud rates shown will be the actual values output from the ACIA in the ÷ 16 mode (actual signal (HZ)= 16 X #BAUD shown.) (ex. 1200 baud line = 19.2 KHz)
BD0-BD7	Buffered data lines 0 through 7 on the BUS.
BRG	Baud rate input to ACIA (U1D)
CLKIN	Input for CPU clock circuit. The CPU (6502) will run at 1/2 or 1/4 of the frequency connected to "CLKIN" dependent on state of WAIT signal.
$\overline{CLR}$	Clear real time clock divider (Address = C020) (low true)
CNT	Input signal for real time clock
CSFL	Chip select to floppy interface (Address = C0XX)
$\overline{CSP}$	Chip select (Address F7XX) for user PIA (low true)
$\overline{CSS}$	Chip select (Address FCXX) for printer (low true)
DD	Data direction
$\overline{DD}$	Not data direction. To be used only when the 505 board is being used only as an I/O board
D0-D7	Data lines 0 through 7
I02VMA	Buffered internal 02VMA signal
$\overline{IRQ}$	Interrupt request (low true)
IRW	Buffered internal Read/Write signal
#MHZ	Actual frequency of the signal
$\overline{NMI}$	Non-maskable interrupt (low true)
02VMA	02
$\overline{RES}$	Reset for CPU and PIA's (low true)
R/W	Read/Write signal on the BUS
TXCLK	Transmit clock for floppy interface
UCA2	CA2 pin on user PIA, U3F, (6820) (Address - F700). This signal is used to force WAIT state in "GT" machines. Low enables "GT" speed.
V-	Negative DC voltage from DC to DC converter
V+	Positive DC voltage from DC to DC converter
$\overline{WAIT}$	Wait for BUS line. A low signal enables slow speed.
125KHZ	125 KHZ from real time clock divider. Used for mini-floppy.


J1
J2
J3
U1A
6820
U1B
6502
U1C
6850
U1D
6850
U1E
74157
U1F
7404
U1G
1489A
U1H
8T26
U2A
8T95
U2B
7417
U2C
74148
U2D
2316
U2E
8T26
U3A
7417
U3B
7417
U3C
74123
U3D
8T95
U3E
7410
U3F
6820 PIA
U3G
8T26
U3H
8T26
U4A
7417
U4B
7404
U4C
74123
U4D
8T95
U4E
7404
U4F
7404
U4G
48 PIN CONNECTOR
U5A
7410
U5B
7426
U5C
7410
U5D
7410
U5E
74390
U5F
74390
U5G
74390
U5H
7420
U5I
7420
U5J
74138
U5K
7404
U5L
7410
U6A
74163
U6B
7493
U6C
7493
U6D
7493
U6E
7404
U6F
7402
U6G
74138
U6H
7400
U6I
7430
4.0 MHz
X 1
MODEL 505 REV B



FRONT VIEW OF 505 REV B BOARD



REAR VIEW OF 505 REV B BOARD