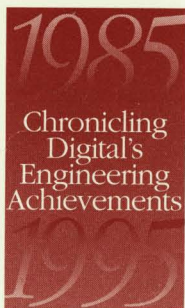


# Digital Technical Journal

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## Cumulative Index

1985-1994



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# Digital Technical Journal

## Cumulative Index

1985-1994

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# Preface

This cumulative index is provided as a convenient means for readers to locate subjects referenced in the *Digital Technical Journal* from 1985 through 1994. Since the *Journal* was first published in 1985, it has offered engineers and educators insights into the design of Digital's innovative engineering in such areas as software, systems, peripherals, semiconductors, and networking. With this index, readers can now more easily access that information.

The editors welcome comments on the utility of the index. Usefulness to readers will determine the frequency with which future indexes are published and enhancements made to the search capabilities of the *Journal's* electronic files on the World Wide Web. Comments may be sent to the attention of the Managing Editor, Digital Technical Journal, Digital Equipment Corporation, 30 Porter Road LJO2/D10, Littleton, Massachusetts 01460 U.S.A., or through the Internet to dtj@digital.com.

## How to Use the *Digital Technical Journal* Cumulative Index

This cumulative index has been designed as a guide to the content and location of papers in the *Digital Technical Journal* 1985–1994. The four sections are Subject Index, Volume Listing, Author Listing, and Acronym Glossary.

**Subject Index** headings are arranged alphabetically. Subheadings are indented under main headings, and secondary subheadings are indented under subheadings. All entries are then arranged chronologically and refer to volume, number, date (year), and page numbers.

*Example:*

Alpha AXP, 4/4 (1992) 19–205

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software simulators, 4/4 (1992) 181–192

Cross-references serve as guides from one heading to another and are of two types:

- *See* references guide the reader to the preferred form of a subject (e.g., LSE *see* Language Sensitive Editor)

- *See also* references guide the reader from one heading to other headings where there is relevant material (e.g., DEC Rdb *See also* VAX Rdb/VMS).

The **Volume Listing** presents the titles and authors of papers for all issues that make up the six volumes referenced in this index.

In the **Author Listing**, author names are arranged alphabetically. A chronological listing of an author's papers follows his or her name.

Because of the extensive number of acronyms used throughout the literature, an **Acronym Glossary** is provided for readers' quick referral.

## Acknowledgments

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- Adiletta, Matthew J.**, "Semiconductor Technology in a High-performance VAX System," Vol. 2, No. 4 (1990)
- Allison, Brian R.**, "An Overview of the VAX 6200 Family of Systems," Vol. 1, No. 7 (1988); "The Architectural Definition Process of the VAX 6200 Family," Vol. 1, No. 7 (1988); "Technical Description of the DEC 7000 and DEC 10000 AXP Family," Vol. 4, No. 4 (1992)
- Allmon, Randy**, "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Alonso, Carlos**, "Verification of the First Fault-tolerant VAX System," Vol. 3, No. 1 (1991)
- Anderson, Walker**, "Logical Verification of the NVAX CPU Chip Design," Vol. 4, No. 3 (1992); "Development of Digital's PCI Chip Sets and Evaluation Kit for the DECchip 21064 Microprocessor," Vol. 6, No. 2 (1994)
- Angebrannt, Susan**, "The Sample X11 Server Architecture," Vol. 2, No. 3 (1990)
- Anglin, Robert**, "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Appel, Neal B.**, "CDA in Science and Engineering," Vol. 2, No. 1 (1990)
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- Axtell, Brian A.**, "Programmer Productivity Aspects of the VAX GKS and VAX PHIGS Products," Vol. 1, No. 6 (1988)
- Baba, Hiroyoshi**, "Japanese Input Method Independent of Applications," Vol. 5, No. 3 (1993)
- Bahaa-El-Din, Wael H.**, "Performance Evaluation of Transaction Processing Systems," Vol. 3, No. 1 (1991)
- Bak, Dennis T.**, "The Impact of VAX 8800 Design Methodology on CAD Development," Vol. 1, No. 4 (1987)
- Baldwin, Christopher**, "Development of the FDDI Physical Layer," Vol. 3, No. 2 (1991)
- Balkovich, Edward E.**, "VAXcluster Availability Modeling," Vol. 1, No. 5 (1987)
- Barnard, Karen E.**, "Hierarchical Fault Detection and Isolation Strategy for the VAX 9000 System," Vol. 2, No. 4 (1990)
- Bartoszek, John T.**, "VAX 6000 Model 400 Physical Technology," Vol. 2, No. 2 (1990)
- Basmaji, Jean H.**, "The Role of Computer-aided Engineering in the Design of the VAX 6200 System," Vol. 1, No. 7 (1988)
- Bates, Kenneth H.**, "Performance Aspects of the HSC Controller," Vol. 1, No. 8 (1989)
- Bean, Robert G.**, "The Hierarchical Storage Controller, A Tightly Coupled Multiprocessor as Storage Server," Vol. 1, No. 8 (1989)
- Beander, Bert**, "VAX/VMS Software Development Environment," Vol. 1, No. 6 (1988)
- Beck, Paul R.**, "The DECnet-VAX Product—An Integrated Approach to Networking," Vol. 1, No. 3 (1986)
- Bell, David A.**, "Transistor Hot Carrier Reliability Assurance in CMOS Technologies," Vol. 4, No. 2 (1992)
- Benoit, Paul**, "DECnet for OpenVMS AXP: A Case History," Vol. 4, No. 4 (1992)
- Benson, David**, "An Overview of the Common Node Software," Vol. 3, No. 2 (1991)
- Benson, Linda E.**, "VTX and VALU—Software Productivity Tools for Distributed Applications Development," Vol. 1, No. 6 (1988)
- Benson, Thomas R.**, "Porting OpenVMS from VAX to Alpha AXP," Vol. 4, No. 4 (1992)
- Bernstein, Debra**, "The NVAX and NVAX+ High-performance VAX Microprocessors," Vol. 4, No. 3 (1992)
- Bernstein, Philip A.**, "DECdta—Digital's Distributed Transaction Processing Architecture," Vol. 3, No. 1 (1991)
- Berti, Antonio C.**, "CMOS-4 Technology for Fast Logic and Dense On-chip Memory," Vol. 4, No. 2 (1992)
- Bertucci, David**, "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Bettels, Jürgen**, "Unicode: A Universal Character Code," Vol. 5, No. 3 (1993); "The X/Open Internationalization Model," Vol. 5, No. 3 (1993)
- Bhabhalia, Prashant**, "VAXcluster Availability Modeling," Vol. 1, No. 5 (1987)

- Bhaiwala, Masooma, "Digital's DECchip 21066: The First Cost-focused Alpha AXP Chip," Vol. 6, No. 1 (1994)
- Bhandarkar, Dileep P., "Vector Processing on the VAX 9000 System," Vol. 2, No. 4 (1990)
- Bidermann, William R., "The MicroVAX 78132 Floating Point Chip," Vol. 1, No. 2 (1986)
- Biro, Larry L., "The NVAX and NVAX+ High-performance VAX Microprocessors," Vol. 4, No. 3 (1992)
- Bischoff, Gabriel P., "A Parallel Implementation of the Circuit Simulator SPICE on the VAX 8800 System," Vol. 1, No. 4 (1987)
- Bishop, F. Avery, "Unicode: A Universal Character Code," Vol. 5, No. 3 (1993)
- Biswas, Prabuddha, "Ethernet Performance of Remote DECwindows Applications," Vol. 2, No. 3 (1990)
- Blaha, Virginia C., "The F Box, Floating Point in the VAX 8600 System," Vol. 1, No. 1 (1985)
- Blickstein, David S., "The GEM Optimizing Compiler System," Vol. 4, No. 4 (1992)
- Bloem, John E., "The VAX 8600 I Box, A Pipelined Implementation of the VAX Architecture," Vol. 1, No. 1 (1985)
- Boone, Steven E., "The TK50 Cartridge Tape Drive," Vol. 1, No. 2 (1986)
- Bouchard, Gregg A., "The VAX 6000 Model 600 Processor," Vol. 4, No. 3 (1992)
- Bowhill, William J., "An Overview of the VAX 6000 Model 400 Chip Set," Vol. 2, No. 2 (1990); "The VAX 6000 Model 400 Scalar Processor Module," Vol. 2, No. 2 (1990)
- Brand, Gerald J., "A Logical Grounding Scheme for the VAX 8800 Processor," Vol. 1, No. 4 (1987)
- Brash, David L.A., "The DECNIS 500/600 Multiprotocol Bridge/Router and Gateway," Vol. 5, No. 1 (1993)
- Brender, Ronald F., "Pragmatics in the Development of VAX Ada," Vol. 1, No. 6 (1988); "Using Simulation to Develop and Port Software," Vol. 4, No. 4 (1992)
- Bresnahan, Edward W., "PATHWORKS for VMS File Server," Vol. 4, No. 1 (1992)
- Brett, Bevin R., "Pragmatics in the Development of VAX Ada," Vol. 1, No. 6 (1988)
- Brewer, Elizabeth A., "Design of the PATHWORKS for ULTRIX File Server," Vol. 4, No. 1 (1992)
- Britton, Sharon, "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Brown, Barry G., "The Unique Features of the VAX 9000 Power System Design," Vol. 2, No. 4 (1990)
- Brown, John F., "An Overview of the VAX 6000 Model 400 Chip Set," Vol. 2, No. 2 (1990); "The NVAX and NVAX+ High-performance VAX Microprocessors," Vol. 4, No. 3 (1992)
- Bruckert, William F., "Designing Reliability into the VAX 8600 System," No. 1 (1985); "Verification of the First Fault-tolerant VAX System," Vol. 3, No. 1 (1991)
- Brunner, Richard A., "Vector Processing on the VAX 9000 System," Vol. 2, No. 4 (1990)
- Bryant, Stewart F., "The DECNIS 500/600 Multiprotocol Bridge/Router and Gateway," Vol. 5, No. 1 (1993)
- BuBler, Christoph J., "Policy Resolution in Workflow Management Systems," Vol. 6, No. 4 (1994)
- Bulger, Joseph M., "CMOS-4 Back-end Process Development for a VLSI 0.75  $\mu\text{m}$  Triple-level Interconnection Technology," Vol. 4, No. 2 (1992)
- Burlèy, Robert M., "An Overview of the Four Systems in the VAX 8800 Family," Vol. 1, No. 4 (1987)
- Butala, Charles F., "The Unique Features of the VAX 9000 Power System Design," Vol. 2, No. 4 (1990)
- Buxton, Kim A., "The ULTRIX Implementation of DECnet/OSI," Vol. 5, No. 1 (1993)
- Calcagni, Richard E., "VAX 6000 Model 400 CPU Chip Set Functional Design Verification," Vol. 2, No. 2 (1990)
- Callander, Michael A., Sr., "The VAX 6000 Model 400 Scalar Processor Module," Vol. 2, No. 2 (1990); "The VAXstation 4000 Model 90," Vol. 4, No. 3 (1992)
- Callon, Ross W., "Routing Architecture," Vol. 5, No. 1 (1993)
- Camilli, Larry T., "Test and Qualification of the VAX 6000 Model 400 System," Vol. 2, No. 2 (1990)
- Cao, Xi-ren, "CI Bus Arbitration Performance in a VAXcluster System," Vol. 1, No. 5 (1987)
- Cardoza, Wayne M., "Porting OpenVMS from VAX to Alpha AXP," Vol. 4, No. 4 (1992)
- Carlson, Lauren M., "The VAXstation 4000 Model 90," Vol. 4, No. 3 (1992); "Development of Digital's PCI Chip Sets and Evaluation Kit for the DECchip 21064 Microprocessor," Vol. 6, No. 2 (1994)
- Chandler, Martha A., "Design of the PATHWORKS for ULTRIX File Server," Vol. 4, No. 1 (1992)
- Chang, Chran-Ham, "ULTRIX Fiber Distributed Data Interface Networking Subsystem Implementation," Vol. 3, No. 2 (1991); "High-performance TCP/IP and UDP/IP Networking in DEC OSF/1 for Alpha AXP," Vol. 5, No. 1 (1993)
- Chang, Luke L., "The Unique Features of the VAX 9000 Power System Design," Vol. 2, No. 4 (1990)
- Chao, Linda, "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Chenet, Steven J., "The Unique Features of the VAX 9000 Power System Design," Vol. 2, No. 4 (1990)
- Cheng, Siu Yin, "PATHWORKS for VMS File Server," Vol. 4, No. 1 (1992)
- Chernoff, Anton, "Binary Translation," Vol. 4, No. 4 (1992)
- Cheung, Baldwin K., "Interapplication Access and Integration," Vol. 2, No. 1 (1990)
- Chin, Derrick J., "The Unique Features of the VAX 9000 Power System Design," Vol. 2, No. 4 (1990)

- Ching, S. Stephen, "The VAX 8600 I Box, A Pipelined Implementation of the VAX Architecture," Vol. 1, No. 1 (1985)
- Chisvin, Lawrence, "The VAX 6000 Model 600 Processor," Vol. 4, No. 3 (1992)
- Chui, Kwong-Tak A., "Design of the VAX 4000 Model 400, 500, and 600 Systems," Vol. 4, No. 3 (1992); "Digital's DECchip 21066: The First Cost-focused Alpha AXP Chip," Vol. 6, No. 1 (1994)
- Cianciolo, Christopher J., "Hardware Accelerators for Bitonal Image Processing," Vol. 3, No. 4 (1991)
- Ciarfella, Paul W., "An Overview of the Common Node Software," Vol. 3, No. 2 (1991)
- Clark, Thomas E., "CMOS-4 Back-end Process Development for a VLSI 0.75  $\mu$ m Triple-level Interconnection Technology," Vol. 4, No. 2 (1992)
- Clement, J. Joseph, "Electromigration Reliability of VLSI Interconnect," Vol. 4, No. 2 (1992)
- Clifford, William H., Jr., "Programmer Productivity Aspects of the VAX GKS and VAX PHIGS Products," Vol. 1, No. 6 (1988)
- Cobb, Graham R., "Digital's Multiprotocol Routing Software Design," Vol. 5, No. 1 (1993)
- Coffler, Jeffrey, "Porting Digital's Database Management Products to the Alpha AXP Platform," Vol. 4, No. 4 (1992)
- Cohen, Seth S., "The Relationship between the DECwrite Editor and the Digital Document Interchange Format," Vol. 2, No. 1 (1990)
- Collica, Randall S., "A Yield Enhancement Methodology for Custom VLSI Manufacturing," Vol. 4, No. 2 (1992)
- Collins, Michael D., "Development of the XUI Toolkit," Vol. 2, No. 3 (1990)
- Colombo, James V., "DECnet for OpenVMS AXP: A Case History," Vol. 4, No. 4 (1992)
- Colon Osorio, Fernando C., "The VAX 8600 I Box, A Pipelined Implementation of the VAX Architecture," Vol. 1, No. 1 (1985); "CI Bus Arbitration Performance in a VAXcluster System," Vol. 1, No. 5 (1987)
- Conklin, Peter F., "Enrollment Management, Managing the Alpha AXP Program," Vol. 4, No. 4 (1992)
- Conrad, Robert A., "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Conroy, David G., "The Alpha Demonstration Unit: A High-performance Multiprocessor for Software and Chip Development," Vol. 4, No. 4 (1992); "The Evolution of the Alpha AXP PC," Vol. 6, No. 1 (1994)
- Conti, Robert A., "Software Productivity Features Provided by the Ada Language and the VAX Ada Compiler," Vol. 1, No. 6 (1988)
- Cotter, Gerald E., "The Unique Features of the VAX 9000 Power System Design," Vol. 2, No. 4 (1990)
- Couranz, Robert, "The E<sup>2</sup>COTS System and Alpha AXP Technology: The New Computer Standard for Military Use," Vol. 6, No. 2 (1994)
- Craig, Peter W., "The GEM Optimizing Compiler System," Vol. 4, No. 4 (1992)
- Crane, Barbara, "Disk Drive Technology Improvements in the RA90," Vol. 1, No. 8 (1989)
- Cressman, David C., "Analysis of Data Compression in the DLT2000 Tape Drive," Vol. 6, No. 2 (1994)
- Croll, John W., "Test and Qualification of the VAX 6000 Model 400 System," Vol. 2, No. 2 (1990)
- Crouse, Robert N., "Hardware Accelerators for Bitonal Image Processing," Vol. 3, No. 4 (1991)
- Crowell, Jonathan C., "Design of the VAX 4000 Model 400, 500, and 600 Systems," Vol. 4, No. 3 (1992); "The Design of the VAX 4000 Model 100 and MicroVAX 3100 Model 90 Desktop Systems," Vol. 4, No. 3 (1992)
- Curless, Jeffrey R., "DECnet Transport Architecture," Vol. 4, No. 1 (1992)
- D'Silva, Vijay G., "Measurement and Analysis Techniques for DECnet Products," Vol. 1, No. 9 (1989)
- Darcy, George A., III, "Using Simulation to Develop and Port Software," Vol. 4, No. 4 (1992)
- Davidson, Caroline S., "The GEM Optimizing Compiler System," Vol. 4, No. 4 (1992)
- Davies, Neil L. M., "SEI-based Process Improvement Efforts at Digital," Vol. 5, No. 4 (1993)
- Davis, Scott H., "Design of VMS Volume Shadowing Phase II—Host-based Shadowing," Vol. 3, No. 3 (1991)
- DeGregory, Karen T., "Performance Evaluation of the VAX 6200 Systems," Vol. 1, No. 7 (1988)
- DeVane, Charles J., "Design of the MicroVAX 3500/3600 Second-level Cache," Vol. 1, No. 7 (1988)
- Denham, Jeffrey M., "DEC OSF/1 Version 3.0 Symmetric Multiprocessing Implementation," Vol. 6, No. 3 (1994)
- Dever, Daniel E., "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Dickau, Martin, "Project Management of the VAX DEC/Test Manager Software Version 2.0," Vol. 1, No. 6 (1988)
- Dietrich, X. Joseph, "A Yield Enhancement Methodology for Custom VLSI Manufacturing," Vol. 4, No. 2 (1992)
- Dimino, Lucien A., "Performance of DEC Rdb Version 6.0 on AXP Systems," Vol. 6, No. 1 (1994)
- Dischler, Richard J., "The MicroVAX 78032 Chip; A 32-Bit Microprocessor," Vol. 1, No. 2 (1986); "HDSC and Multichip Unit Design and Manufacture," Vol. 2, No. 4 (1990); "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Dolan, Francis, "Network Management," Vol. 5, No. 1 (1993)
- Donchin, Dale R., "The NVAX CPU Chip: Design Challenges, Methods and CAD Tools," Vol. 4, No. 3 (1992)
- Dormitzer, Paul H., "The VAX 9000 Service Processor Unit," Vol. 2, No. 4 (1990)
- Doucette, Richard L., "Semiconductor Technology in a High-performance VAX System," Vol. 2, No. 4 (1990)



- Doyle, Brian S., "Transistor Hot Carrier Reliability Assurance in CMOS Technologies," Vol. 4, No. 2 (1992)
- Dubash, Jamshed H., "CMOS-4 Back-end Process Development for a VLSI 0.75  $\mu\text{m}$  Triple-level Interconnection Technology," Vol. 4, No. 2 (1992)
- Duffy, Darrell J., "The System Communication Architecture," Vol. 1, No. 5 (1987)
- Dumont, Margaret M., "SEI-based Process Improvement Efforts at Digital," Vol. 5, No. 4 (1993)
- Dunbeck, Peter B., "HDSC and Multichip Unit Design and Manufacture," Vol. 2, No. 4 (1990)
- Duncan, Anne Smith, "Software Productivity Measurements," Vol. 1, No. 6 (1988)
- Dunnington, William R., "VAXcluster Availability Modeling," Vol. 1, No. 5 (1987)
- Durdan, W. Hugh, "An Overview of the VAX 6000 Model 400 Chip Set," Vol. 2, No. 2 (1990)
- Dutton, Todd A., "The Design of the DEC 3000 AXP Systems, Two High-performance Workstations," Vol. 4, No. 4 (1992)
- Eck, John C., "Synthesis in the CAD System Used to Design the VAX 9000 System," Vol. 2, No. 4 (1990)
- Edmondson, John H., "The NVAX and NVAX+ High-performance VAX Microprocessors," Vol. 4, No. 3 (1992)
- Eiref, Daniel, "The Design of the DEC 3000 AXP Systems, Two High-performance Workstations," Vol. 4, No. 4 (1992)
- Emberton, William T., "DECdta—Digital's Distributed Transaction Processing Architecture," Vol. 3, No. 1 (1991)
- Emer, Joel S., "Design and Implementation of the VAX Distributed File Service," Vol. 1, No. 9 (1989)
- Emlich, Larry W., "VAXsimPLUS, A Fault Manager Implementation," Vol. 1, No. 8 (1989)
- Engberg, Björn, "X Window Terminals," Vol. 3, No. 4 (1991)
- English, William, "An Overview of the VAX 8600 System," Vol. 1, No. 1 (1985); "Cooling the VAX 8600 Processor," Vol. 1, No. 1 (1985)
- Faiman, R. Neil, Jr., "The GEM Optimizing Compiler System," Vol. 4, No. 4 (1992)
- Falcone, Joseph R., "The Evolution of the Alpha AXP PC," Vol. 6, No. 1 (1994)
- Faricelli, John V., "Numerical Device and Process Simulation Tools in Transistor Design," Vol. 4, No. 2 (1992)
- Farnham, Stuart J., "VMS Multiprocessing on the VAX 8800 System," Vol. 1, No. 4 (1987)
- Farrell, James A., "Microprocessor Performance and Process Complexity in CMOS Technologies," Vol. 4, No. 2 (1992)
- Feenan, James J., Jr., "The Design of Multimedia Object Support in DEC Rdb," Vol. 5, No. 2 (1993)
- Fenwick, David M., "Vector Processing on the VAXvector 6000 Model 400," Vol. 2, No. 2 (1990)
- Ferris, Edward J., "The ULTRIX Implementation of DECnet/OSI," Vol. 5, No. 1 (1993)
- Finkelstein, Eugene, "Performance Evaluation of Distributed Applications and Services in the DECnet Environment," Vol. 1, No. 9 (1989)
- Fischer, Timothy C., "The NVAX CPU Chip: Design Challenges, Methods and CAD Tools," Vol. 4, No. 3 (1992)
- Fishbein, Bruce J., "Transistor Hot Carrier Reliability Assurance in CMOS Technologies," Vol. 4, No. 2 (1992)
- Fisher, Amnon, "The MicroVAX 78132 Floating Point Chip," Vol. 1, No. 2 (1986)
- Fite, David B., Jr., "Design Strategy for the VAX 9000 System," Vol. 2, No. 4 (1990)
- Flower, Richard, "High-performance TCP/IP and UDP/IP Networking in DEC OSF/1 for Alpha AXP," Vol. 5, No. 1 (1993)
- Forecast, John, "The DECnet-ULTRIX Software, Vol. 1, No. 3 (1986); "High-performance TCP/IP and UDP/IP Networking in DEC OSF/1 for Alpha AXP," Vol. 5, No. 1 (1993)
- Fossum, Tryggve, "An Overview of the VAX 8600 System," Vol. 1, No. 1 (1985); "The F Box, Floating Point in the VAX 8600 System," Vol. 1, No. 1 (1985); "Design Strategy for the VAX 9000 System," Vol. 2, No. 4 (1990)
- Fox, Michael S., "Local Area VAXcluster Systems," Vol. 1, No. 5 (1987)
- Fox, Thomas F., "The CVAX 78034 Chip, a 32-bit Second-generation VAX Microprocessor," Vol. 1, No. 7 (1988); "Microprocessor Performance and Process Complexity in CMOS Technologies," Vol. 4, No. 2 (1992); "The NVAX CPU Chip: Design Challenges, Methods and CAD Tools," Vol. 4, No. 3 (1992)
- Friedberg, Jeffrey D., "PEX: A Network-transparent Three-dimensional Graphics System," Vol. 2, No. 3 (1990)
- Friedman, Lawrence N., "An Implementation of the OSI Upper Layers and Applications," Vol. 5, No. 1 (1993)
- Fu, John, "Aspects of the VAX 8800 C Box Design," Vol. 1, No. 4 (1987)
- Furlong, Thomas C., "Development of the DECstation 3100," Vol. 2, No. 2 (1990)
- Furtney, Mark, "A Shared Memory MPP from Cray Research," Vol. 6, No. 2 (1994)
- Gagnon, Michael, "DB Integrator: Open Middleware for Data Access," Vol. 7, No. 1 (1995)
- Gamache, Rodney N., "VMS Symmetric Multiprocessing," Vol. 1, No. 7 (1988)
- Garver, Marion M., "CMOS-4 Back-end Process Development for a VLSI 0.75  $\mu\text{m}$  Triple-level Interconnection Technology," Vol. 4, No. 2 (1992)
- Garvey, Glenn P., "The Role of Computer-aided Engineering in the Design of the VAX 6200 System," Vol. 1, No. 7 (1988)
- George, Peter, "The Making of a MicroVAX Workstation," Vol. 1, No. 2 (1986)

- Gerberg, Elliot C., "Digital's Multiprotocol Routing Software Design," Vol. 5, No. 1 (1993)
- Gianatassio, Michael, Jr., "VTX and VALU—Software Productivity Tools for Distributed Applications Development," Vol. 1, No. 6 (1988)
- Gieseke, Bruce, "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Gilbert, Peter D., "Development of the VAX NOTES System," Vol. 1, No. 6 (1988)
- Gillett, Richard B., Jr., "Interfacing a VAX Microprocessor to a High-speed Multiprocessing Bus," Vol. 1, No. 7 (1988)
- Giokas, Dennis G., "eXcursion for Windows: Integrating Two Windowing Systems," Vol. 4, No. 1 (1992); "The Design of ManageWORKS: A User Interface Framework," Vol. 6, No. 4 (1994)
- Glossop, Kent D., "The GEM Optimizing Compiler System," Vol. 4, No. 4 (1992)
- Goldman, Matthew S., "The VAX 9000 Service Processor Unit," Vol. 2, No. 4 (1990)
- Goldstein, Andrew C., "The Design and Implementation of a Distributed File System," Vol. 1, No. 5 (1987)
- Goleman, William L., "Improving Process to Increase Productivity While Assuring Quality: A Case Study of the Volume Shadowing Port to OpenVMS AXP," Vol. 6, No. 1 (1994)
- Good, Michael D., "Software Usability Engineering," Vol. 1, No. 6 (1988)
- Graham, Richard, "Fiber Distributed Data Interface Overview," Vol. 3, No. 2 (1991)
- Grass, Steven J., "Development of a Graphical Program Generator," Vol. 1, No. 6 (1988)
- Grawin, Richard A., "Performance Evaluation of Distributed Applications and Services in the DECnet Environment," Vol. 1, No. 9 (1989)
- Gray, Heather, "High-performance TCP/IP and UDP/IP Networking in DEC OSF/1 for Alpha AXP," Vol. 5, No. 1 (1993)
- Greenberg, Steven S., "A Parallel Implementation of the Circuit Simulator SPICE on the VAX 8800 System," Vol. 1, No. 4 (1987)
- Greenwood, Stephen R., "VAX SCAN: Rule-based Text Processing Software," Vol. 1, No. 6 (1988); "The DECwindows User Interface Language," Vol. 2, No. 3 (1990); "International Cultural Differences in Software," Vol. 5, No. 3 (1993)
- Griffin, David M., "Remote System Management in Network Environments," Vol. 1, No. 9 (1989)
- Gronowski, Paul E., "The CVAX 78034 Chip, a 32-bit Second-generation VAX Microprocessor," Vol. 1, No. 7 (1988)
- Grove, Richard B., "The GEM Optimizing Compiler System," Vol. 4, No. 4 (1992)
- Gruha, Gregory J., "CMOS-4 Technology for Fast Logic and Dense On-chip Memory," Vol. 4, No. 2 (1992)
- Grundmann, William R., "The F Box, Floating Point in the VAX 8600 System," Vol. 1, No. 1 (1985)
- Guenther, Alan, "Design of the DECprint Common Printer Supervisor for VMS Systems," Vol. 3, No. 4 (1991)
- Guerrieri, Ernesto, "DEC TP WORKcenter: A Software Process Case Study," Vol. 5, No. 4 (1993)
- Gumbel, Richard T., "Development of the CDA Toolkit," Vol. 2, No. 1 (1990)
- Habib, Frances A., "Tools and Techniques for Preliminary Sizing of Transaction Processing Applications," Vol. 3, No. 1 (1991)
- Hackenberg, John H., "Signal Integrity in the VAX 8600 System," Vol. 1, No. 1 (1985); "Semiconductor Technology in a High-performance VAX System," Vol. 2, No. 4 (1990)
- Haduch, Kenneth J., "Aspects of the VAX 8800 C Box Design," Vol. 1, No. 4 (1987)
- Haentjens, René, "The Ordering of Universal Character Strings," Vol. 5, No. 3 (1993)
- Hannemann, Robert J., "VAX 6000 Model 400 Physical Technology," Vol. 2, No. 2 (1990)
- Hansen, Stephen P., "VAX 6000 Model 400 Physical Technology," Vol. 2, No. 2 (1990)
- Harokopus, Robert P., "Hierarchical Fault Detection and Isolation Strategy for the VAX 9000 System," Vol. 2, No. 4 (1990)
- Harper, John, "Overview of Digital's Open Networking," Vol. 5, No. 1 (1993)
- Harris, Thomas J., "Software Productivity Measurements," Vol. 1, No. 6 (1988)
- Harvey, Michael S., "VMS Multiprocessing on the VAX 8800 System," Vol. 1, No. 4 (1987)
- Hasenaar, Robert, "The Megadoc Image Document Management System," Vol. 5, No. 2 (1993)
- Hassoun, Soha M. N., "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Hawe, William R., "Performance Analysis and Modeling of Digital's Networking Architecture," Vol. 1, No. 3 (1986); "The Extended Local Area Network Architecture and LANBridge 100," Vol. 1, No. 3 (1986); "Fiber Distributed Data Interface Overview," Vol. 3, No. 2 (1991); "High-performance TCP/IP and UDP/IP Networking in DEC OSF/1 for Alpha AXP," Vol. 5, No. 1 (1993)
- Hayden, Peter C., "Fiber Distributed Data Interface Overview," Vol. 3, No. 2 (1991); "LAN Addressing for Digital Video Data," Vol. 5, No. 2 (1993)
- Hayes, Fidelma M., "Design of the AlphaServer Multiprocessor Server Systems," Vol. 6, No. 3 (1994)
- Herrick, William V., "An Overview of the VAX 6000 Model 400 Chip Set," Vol. 2, No. 2 (1990)
- Hetherington, Ricky C., "VAX Instructions That Illustrate the Architectural Features of the VAX 9000 CPU," Vol. 2, No. 4 (1990)

- Heydari, Masood, "The Role of Computer-aided Engineering in the Design of the VAX 6200 System," Vol. 1, No. 7 (1988)
- Hiscock, James S., "Development of the DECbridge 500 Product," Vol. 3, No. 2 (1991)
- Ho, Roy, "DXML: A High-performance Scientific Subroutine Library," Vol. 6, No. 3 (1994)
- Hobbs, Steven O., "The GEM Optimizing Compiler System," Vol. 4, No. 4 (1992)
- Hoepfner, Gregory W., "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Honma, Takahide, "Japanese Input Method Independent of Applications," Vol. 5, No. 3 (1993)
- Hooper, Donald F., "Synthesis in the CAD System Used to Design the VAX 9000 System," Vol. 2, No. 4 (1990)
- Hoover, Stewart V., "The Design of DECmodel for Windows," Vol. 6, No. 4 (1994)
- Houghton, Christopher L., "Digital's DECchip 21066: The First Cost-focused Alpha AXP Chip," Vol. 6, No. 1 (1994)
- Houlihan, Paul J., "Improving Process to Increase Productivity While Assuring Quality: A Case Study of the Volume Shadowing Port to OpenVMS AXP," Vol. 6, No. 1 (1994)
- Hrones, John A., Jr., "Defining Global Requirements with Distributed QFD," Vol. 5, No. 4 (1993)
- Hsiao, Ruei-Hsin, "Measurement and Analysis Techniques for DECnet Products," Vol. 1, No. 9 (1989)
- Hsu, Yun-Ping, "Performance Evaluation of Transaction Processing Systems," Vol. 3, No. 1 (1991)
- Huntwork, Paul K., "Changing the Rules: A Pragmatic Approach to Product Development," Vol. 5, No. 4 (1993)
- Hutchings, Anthony F., "The Evolution of the Custom CAD Suite Used on the MicroVAX II System," Vol. 1, No. 2 (1986)
- Hutchison, Jerry D., "Development of the FDDI Physical Layer," Vol. 3, No. 2 (1991)
- Iles, Michael V., "Using Simulation to Develop and Port Software," Vol. 4, No. 4 (1992)
- Jack, Martin L., "Development of the CDA Toolkit," Vol. 2, No. 1 (1990)
- Jackson, Daniel B., "Transistor Hot Carrier Reliability Assurance in CMOS Technologies," Vol. 4, No. 2 (1992)
- Jackson, James L., "The DECnet-ULTRIX Software," Vol. 1, No. 3 (1986)
- Jacobson, Neal F., "The Digital Table Interchange Format," Vol. 2, No. 1 (1990); "Interapplication Access and Integration," Vol. 2, No. 1 (1990); "The Design and Development of the DECdecision Product," Vol. 2, No. 1 (1990)
- Jagannathan, Ravindran, "Porting OpenVMS from VAX to Alpha AXP," Vol. 4, No. 4 (1992)
- Jain, Anil K., "The CVAX 78034 Chip, a 32-bit Second-generation VAX Microprocessor," Vol. 1, No. 7 (1988)
- Jain, Raj, "Performance Analysis and Modeling of Digital's Networking Architecture," Vol. 1, No. 3 (1986)
- Janetos, James P., "The VAX 8800 Input/Output System," Vol. 1, No. 4 (1987)
- Janosik, John L., Jr., "The Design of Multimedia Object Support in DEC Rdb," Vol. 5, No. 2 (1993)
- Jedrey, Benjamin C., Jr., "Defining Global Requirements with Distributed QFD," Vol. 5, No. 4 (1993)
- Jesuraj, Ramasamy, "Modeling and Analysis of the DECnet/SNA Gateway," Vol. 1, No. 9 (1989)
- Johnson, Brad C., "Remote System Management in Network Environments," Vol. 1, No. 9 (1989)
- Johnson, James E., "Transaction Management Support in the VMS Operating System Kernel," Vol. 3, No. 1 (1991); "The Structure of the OpenVMS Management Station," Vol. 6, No. 4 (1994)
- Jones, James D., "The Common Printer Access Protocol," Vol. 3, No. 4 (1991)
- Jones, Richard D., "CMOS-4 Technology for Fast Logic and Dense On-chip Memory," Vol. 4, No. 2 (1992)
- Jones, Tracey L., "Floating Point in the VAX 8800 Family," Vol. 1, No. 4 (1987)
- Josephson, Ronald E., "Designing Reliability into the VAX 8600 System," Vol. 1, No. 1 (1985)
- Joshi, Ashok M., "A Relational Database Management System for Production Applications," Vol. 1, No. 8 (1989); "Designing an Optimized Transaction Commit Protocol," Vol. 3, No. 1 (1991)
- Kachrani, Ajay P., "The Common Printer Access Protocol," Vol. 3, No. 4 (1991)
- Kalita, E. Brian, "Cooling the VAX 8600 Processor," Vol. 1, No. 1 (1985)
- Kalkunte, Ramsesh S., "Performance Analysis of a High-speed FDDI Adapter," Vol. 3, No. 3 (1991)
- Kamath, Chandrika, "DXML: A High-performance Scientific Subroutine Library," Vol. 6, No. 3 (1994)
- Keller, James B., "Aspects of the VAX 8800 C Box Design," Vol. 1, No. 4 (1987)
- Kement, Michael W., "A Logical Grounding Scheme for the VAX 8800 Processor," Vol. 1, No. 4 (1987)
- Kempf, Mark F., "The Extended Local Area Network Architecture and LANBridge 100," Vol. 1, No. 3 (1986); "Terminal Servers on Ethernet Local Area Networks," Vol. 1, No. 3 (1986)
- Kenah, Lawrence J., "The Evolution of Instruction Emulation for the MicroVAX Systems," Vol. 1, No. 2 (1986)
- Kent, Christopher A., "XDPS: A Display PostScript System Extension for DECwindows," Vol. 2, No. 3 (1990)
- Khalil, Nadim A., "Numerical Device and Process Simulation Tools in Transistor Design," Vol. 4, No. 2 (1992)
- Kirby, Alan J., "The Extended Local Area Network Architecture and LANBridge 100," Vol. 1, No. 3 (1986)
- Kirk, Matthew B., "Binary Translation," Vol. 4, No. 4 (1992)

- Knox, Stephen T., "Modeling the Cost of Software Quality," Vol. 5, No. 4 (1993)
- Kochem, Robert C., "Development of the DECbridge 500 Product," Vol. 3, No. 2 (1991)
- Koeninger, R. Kent, "A Shared Memory MPP from Cray Research," Vol. 6, No. 2 (1994)
- Kohler, Walter H., "Performance Evaluation of Transaction Processing Systems," Vol. 3, No. 1 (1991)
- Koning, G. Paul, "The DECconcentrator 500 Product," Vol. 3, No. 2 (1991)
- Kopec, Thomas E., "Design of the VAX 4000 Model 400, 500, and 600 Systems," Vol. 4, No. 3 (1992); "The Evolution of the Alpha AXP PC," Vol. 6, No. 1 (1994)
- Krakauer, David B., "Transistor Hot Carrier Reliability Assurance in CMOS Technologies," Vol. 4, No. 2 (1992)
- Kratkiewicz, Gary L., "The Design of DECmodel for Windows," Vol. 6, No. 4 (1994)
- Kravitz, David, "Development of Digital's PCI Chip Sets and Evaluation Kit for the DECchip 21064 Microprocessor," Vol. 6, No. 2 (1994)
- Kretschmer, Reinhard, "Margin Analysis on Magnetic Disk Recording Channels," Vol. 1, No. 8 (1989)
- Krishnakumar, P. G., "GIGAswitch System: A High-performance Packet-switching Platform," Vol. 6, No. 1 (1994)
- Kronenberg, Nancy P., "The VAXcluster Concept: An Overview of a Distributed System," Vol. 1, No. 5 (1987); "Porting OpenVMS from VAX to Alpha AXP," Vol. 4, No. 4 (1992)
- Krycka, James A., "The DECnet-VAX Product—An Integrated Approach to Networking," Vol. 1, No. 3 (1986)
- Kuchler, Kathryn, "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Kuenzel, James E., "The DECconcentrator 500 Product," Vol. 3, No. 2 (1991)
- Kuhn, Robert H., "The KAP Parallelizer for DEC Fortran and DEC C Programs," Vol. 6, No. 3 (1994)
- Kurth, Hugh R., "The Design of the DEC 3000 AXP Systems, Two High-performance Workstations," Vol. 4, No. 4 (1992)
- Kwong, Ambrose C., "Modeling and Analysis of the DECnet/SNA Gateway," Vol. 1, No. 9 (1989)
- La Pelle, Nancy R., "The Evolution of Network Management Products," Vol. 1, No. 3 (1986)
- Ladd, Andrew R., "The VAXstation 4000 Model 90," Vol. 4, No. 3 (1992)
- Ladd, Maureen, "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Laing, William A., "Transaction Management Support in the VMS Operating System Kernel," Vol. 3, No. 1 (1991)
- Lambracht, Rudolph, Jr., "A Yield Enhancement Methodology for Custom VLSI Manufacturing," Vol. 4, No. 2 (1992)
- Landau, Richard, "Design of the DECprint Common Printer Supervisor for VMS Systems," Vol. 3, No. 4 (1991)
- Landau, Robert V., "Transaction Management Support in the VMS Operating System Kernel," Vol. 3, No. 1 (1991)
- Lanza, Raymond, "Porting ULTRIX Software to the MicroVAX System," Vol. 1, No. 2 (1986)
- Lary, Richard F., "The Hierarchical Storage Controller, A Tightly Coupled Multiprocessor as Storage Server," Vol. 1, No. 8 (1989)
- Lasher, Lewis, "The VAX RALLY System—A Relational Fourth-Generation Language," Vol. 1, No. 6 (1988)
- Lau, David G., "A Yield Enhancement Methodology for Custom VLSI Manufacturing," Vol. 4, No. 2 (1992)
- Lauck, Anthony G., "Digital Network Architecture Overview," Vol. 1, No. 3 (1986)
- Laurune, William R., "The Digital Document Interchange Format," Vol. 2, No. 1 (1990)
- Lawson, John R., Jr., "Automatic, Network-directed Operating System Software Upgrades: A Platform-independent Approach," Vol. 6, No. 4 (1994)
- Leahy, Lee, "New Availability Features of Local Area VAXcluster Systems," Vol. 3, No. 3 (1991)
- Leary, Burton M., "The MicroVAX 78132 Floating Point Chip," Vol. 1, No. 2 (1986); "The CVAX 78034 Chip, a 32-bit Second-generation VAX Microprocessor," Vol. 1, No. 7 (1988); "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Leasure, Bruce, "The KAP Parallelizer for DEC Fortran and DEC C Programs," Vol. 6, No. 3 (1994)
- Leibholz, Daniel L., "Digital's DECchip 21066: The First Cost-focused Alpha AXP Chip," Vol. 6, No. 1 (1994)
- Lemmon, Paul J., "The Design and Verification of the AlphaStation 600 5-series Workstation," Vol. 7, No. 1 (1995)
- Leskowitz, Andrew T., "eXcursion for Windows: Integrating Two Windowing Systems," Vol. 4, No. 1 (1992)
- Leuthold, Dale H., "Semiconductor Technology in a High-performance VAX System," Vol. 2, No. 4 (1990)
- Leveille, Paul A., "The VAX 9000 Service Processor Unit," Vol. 2, No. 4 (1990)
- Levine, Ronald D., "Volume Rendering with the Kubota 3D Imaging and Graphics Accelerator," Vol. 6, No. 2 (1994)
- Levy, Henry M., "The VAXcluster Concept: An Overview of a Distributed System," Vol. 1, No. 5 (1987)
- Lichtenberg, Mitchell P., "DECnet Transport Architecture," Vol. 4, No. 1 (1992)
- Lidington, Gary P., "Overview of the MicroVAX 3500/3600 Processor Module," Vol. 1, No. 7 (1988)
- Litwinetz, Dennis M., "Semiconductor Technology in a High-performance VAX System," Vol. 2, No. 4 (1990)
- Lloyd, James R., "Electromigration Reliability of VLSI Interconnect," Vol. 4, No. 2 (1992)

- Long, Paula, "DEC OSF/1 Version 3.0 Symmetric Multiprocessing Implementation," Vol. 6, No. 3 (1994)
- Low, David A., "An Overview of the PATHWORKS Product Family," Vol. 4, No. 1 (1992)
- Lundberg, James R., "The VAX 6000 Model 400 Scalar Processor Module," Vol. 2, No. 2 (1990)
- Lupton, Glenn, "Language-Sensitive Editor," Vol. 1, No. 6 (1988)
- Lynch, Brian T., "The Unique Features of the VAX 9000 Power System Design," Vol. 2, No. 4 (1990)
- Madden, Liam, "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Mager, Ellen J., "DECnet Transport Architecture," Vol. 4, No. 1 (1992)
- Manley, Dwight P., "Design Strategy for the VAX 9000 System," Vol. 2, No. 4 (1990); "DXML: A High-performance Scientific Subroutine Library," Vol. 6, No. 3 (1994);
- Mann, Bruce E., "Terminal Servers on Ethernet Local Area Networks," Vol. 1, No. 3 (1986)
- Marcello, Richard C., "An Overview of the VAX 6000 Model 400 Chip Set," Vol. 2, No. 2 (1990)
- Marks, Maurice P., "Binary Translation," Vol. 4, No. 4 (1992)
- Martin, Sally J., "Development of the VAX Distributed Name Service," Vol. 1, No. 9 (1989)
- Maruska, David W., "The Design of the VAX 4000 Model 100 and MicroVAX 3100 Model 90 Desktop Systems," Vol. 4, No. 3 (1992)
- Maskay, Barry A., "Developing the MicroVAX II CPU Board," Vol. 1, No. 2 (1986); "Development of the CVAX Q22-bus Interface Chip," Vol. 1, No. 7 (1988); "Design and Performance of the DEC 4000 AXP Departmental Server Computing Systems," Vol. 4, No. 4 (1992)
- Matthews, Andrew J., "On-line Manufacturing Data Access on the VAX 8800 Project," Vol. 1, No. 4 (1987)
- Mayo, Brian T., "Development of the DECbridge 500 Product," Vol. 3, No. 2 (1991)
- McCann, Janet M., "Development of the VAX Distributed Name Service," Vol. 1, No. 9 (1989)
- McCarty, Robert J., "VAX 6000 Model 400 Physical Technology," Vol. 2, No. 2 (1990)
- McElroy, James B., "An Overview of the VAX 8600 System," Vol. 1, No. 1 (1985); "Packaging the VAX 8600 Processor," Vol. 1, No. 1 (1985); "HDSC and Multichip Unit Design and Manufacture," Vol. 2, No. 4 (1990)
- McGregor, Scott A., "An Overview of the DECwindows Architecture," Vol. 2, No. 3 (1990)
- McKeen, Francis X., "Vector Processing on the VAX 9000 System," Vol. 2, No. 4 (1990)
- McKeen, Karen L., "VTX and VALU—Software Productivity Tools for Distributed Applications Development," Vol. 1, No. 6 (1988)
- McKinney, Dina L., "Digital's DECchip 21066: The First Cost-focused Alpha AXP Chip," Vol. 6, No. 1 (1994)
- McLellan, Edward J., "Development of the CVAX Floating Point Chip," Vol. 1, No. 7 (1988); "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Mediouni, Rabah, "Performance of DEC Rdb Version 6.0 on AXP Systems," Vol. 6, No. 1 (1994)
- Melton, Jim, "Character Internationalization in Databases: A Case Study," Vol. 5, No. 3 (1993)
- Melvin, James M., "Verification of the First Fault-tolerant VAX System," Vol. 3, No. 1 (1991)
- Merewood, Richard J., "The VAXcluster Concept: An Overview of a Distributed System," Vol. 1, No. 5 (1987)
- Methot, Christopher E., "Capacity Modeling of PATHWORKS Client-Server Workloads," Vol. 4, No. 1 (1992)
- Metzger, Jeffrey A., "Design of the Turbo PrintServer 20 Controller," Vol. 3, No. 4 (1991)
- Mevis, Joop W., "The Megadoc Image Document Management System," Vol. 5, No. 2 (1993)
- Meyer, Derrick R., "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Meyer, Jeanne E., "Internal Organization of the Alpha 21164, a 300-MHz 64-bit Quad-issue CMOS RISC Microprocessor," Vol. 7, No. 1 (1995)
- Mierswa, Peter O., "The DECnet-DOS System," Vol. 1, No. 3 (1986); "The Evolution of the Mailbus," Vol. 1, No. 9 (1989)
- Millbrandt, Dorothy Noren, "The DECnet/OSI for OpenVMS Version 5.5 Implementation," Vol. 5, No. 1 (1993)
- Miner, Daniel G., "The CVAX 78034 Chip, a 32-bit Second-generation VAX Microprocessor," Vol. 1, No. 7 (1988)
- Mirchandani, Dinesh, "Ethernet Performance of Remote DECwindows Applications," Vol. 2, No. 3 (1990)
- Mishra, Sudhindra N., "The VAX 8800 Microarchitecture," Vol. 1, No. 4 (1987)
- Mitchell, Charles Z., "Pragmatics in the Development of VAX Ada," Vol. 1, No. 6 (1988)
- Mitton, David J., "The DECnet-DOS System," Vol. 1, No. 3 (1986)
- Mohamed, Zia, "Porting Digital's Database Management Products to the Alpha AXP Platform," Vol. 4, No. 4 (1992)
- Montanaro, James, "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Morency, John P., "The DECnet/SNA Gateway Product—A Case Study in Cross Vendor Networking," Vol. 1, No. 3 (1986); "Modeling and Analysis of the DECnet/SNA Gateway," Vol. 1, No. 9 (1989)
- Morgan, David K., "The CVAX CMCTL—A CMOS Memory Controller Chip," Vol. 1, No. 7 (1988)

- Morgan, Wm. Eugene**, "The Relationship between the DECwrite Editor and the Digital Document Interchange Format," Vol. 2, No. 1 (1990)
- Morris, Stephen J.**, "Using Simulation to Develop and Port Software," Vol. 4, No. 4 (1992)
- Morse, Kathleen D.**, "The Evolution of Instruction Emulation for the MicroVAX Systems," Vol. 1, No. 2 (1986); "VMS Multiprocessing on the VAX 8800 System," No. 4 (1987); "VMS Symmetric Multiprocessing," Vol. 1, No. 7 (1988)
- Moses, Bhagyam**, "Performance Evaluation of the VAX 6200 Systems," Vol. 1, No. 7 (1988)
- Mullens, James R.**, "Digital's DECchip 21066: The First Cost-focused Alpha AXP Chip," Vol. 6, No. 1 (1994)
- Murray, John E.**, "VAX Instructions That Illustrate the Architectural Features of the VAX 9000 CPU," Vol. 2, No. 4 (1990)
- Muzzey, Douglas W.**, "Changing the Rules: A Pragmatic Approach to Product Development," Vol. 5, No. 4 (1993)
- Nadkarni, Ashok P.**, "High-performance TCP/IP and UDP/IP Networking in DEC OSF/1 for Alpha AXP," Vol. 5, No. 1 (1993)
- Nadkarni, Samyojita A.**, "Design of the VAX 4000 Model 400, 500, and 600 Systems," Vol. 4, No. 3 (1992); "Development of Digital's PCI Chip Sets and Evaluation Kit for the DECchip 21064 Microprocessor," Vol. 6, No. 2 (1994)
- Nanz, Gerd**, "Numerical Device and Process Simulation Tools in Transistor Design," Vol. 4, No. 2 (1992)
- Nash, Andrew K.**, "The ULTRIX Implementation of DECnet/OSI," Vol. 5, No. 1 (1993)
- Nasr, Andre I.**, "CMOS-4 Technology for Fast Logic and Dense On-chip Memory," Vol. 4, No. 2 (1992)
- Nasr, Mary Beth**, "DECnet Transport Architecture," Vol. 4, No. 1 (1992)
- Natarajan, Thiagarajan**, "The Unique Features of the VAX 9000 Power System Design," Vol. 2, No. 4 (1990)
- Natusch, Paul J.**, "The Memory System in the VAX 8800 Family," Vol. 1, No. 4 (1987)
- Neidecker-Lutz, Burkhard K.**, "Software Motion Pictures," Vol. 5, No. 2 (1993)
- Newman, Todd D.**, "The Sample X11 Server Architecture," Vol. 2, No. 3 (1990)
- Nichols, William G.**, "Design and Implementation of the VAX Distributed File Service," Vol. 1, No. 9 (1989)
- Nielsen, Michael J. K.**, "Development of the DECstation 3100," Vol. 2, No. 2 (1990)
- Nishimoto, Peter L.**, "PEX: A Network-transparent Three-dimensional Graphics System," Vol. 2, No. 3 (1990)
- Norcross, Mitchell O.**, "The VAXstation 4000 Model 90," Vol. 4, No. 3 (1992); "Development of Digital's PCI Chip Sets and Evaluation Kit for the DECchip 21064 Microprocessor," Vol. 6, No. 2 (1994)
- Nourse, Andrew W.**, "Microsoft Windows Network Virtual Device Drivers in PATHWORKS for DOS," Vol. 4, No. 1 (1992)
- Noyce, William B.**, "The GEM Optimizing Compiler System," Vol. 4, No. 4 (1992)
- Olson, Ronald M.**, "CDA in Science and Engineering," Vol. 2, No. 1 (1990)
- Omahen, Kenneth J.**, "Tools and Techniques for Preliminary Sizing of Transaction Processing Applications," Vol. 3, No. 1 (1991)
- Oran, David R.**, "Digital Network Architecture Overview," Vol. 1, No. 3 (1986); "The DECnet/SNA Gateway Product—A Case Study in Cross Vendor Networking," Vol. 1, No. 3 (1986)
- Oran, David R.**, "Development of the VAX Distributed Name Service," Vol. 1, No. 9 (1989)
- Özveren, Cüneyt M.**, "GIGAswitch System: A High-performance Packet-switching Platform," Vol. 6, No. 1 (1994)
- Palmer, Lawrence B.**, "DECspin: A Networked Desktop Videoconferencing Application," Vol. 5, No. 2 (1993)
- Palmer, Lawrence G.**, "ULTRIX Fiber Distributed Data Interface Networking Subsystem Implementation," Vol. 3, No. 2 (1991)
- Palmer, Ricky S.**, "DECspin: A Networked Desktop Videoconferencing Application," Vol. 5, No. 2 (1993)
- Pan, Davis Yen**, "Digital Audio Compression," Vol. 5, No. 2 (1993)
- Park, Daeil**, "System Level Performance of VAX 8974 and 8978 Systems," Vol. 1, No. 5 (1987)
- Patel, Bimal**, "Vector Processing on the VAX 9000 System," Vol. 2, No. 4 (1990)
- Patel, Sanjay J.**, "Digital's DECchip 21066: The First Cost-focused Alpha AXP Chip," Vol. 6, No. 1 (1994)
- Patrick, Paul B., Sr.**, "CASE Integration Using ACA Services," Vol. 5, No. 2 (1993)
- Payson, Christopher J.**, "Hardware Accelerators for Bitonal Image Processing," Vol. 3, No. 4 (1991)
- Peng, Victor**, "The NVAX CPU Chip: Design Challenges, Methods and CAD Tools," Vol. 4, No. 3 (1992)
- Perlman, Radia J.**, "Digital Network Architecture Overview," Vol. 1, No. 3 (1986); "Routing Architecture," Vol. 5, No. 1 (1993)
- Pickholtz, Jeffrey D.**, "The NVAX and NVAX+ High-performance VAX Microprocessors," Vol. 4, No. 3 (1992)
- Pietras, Christine M.**, "Changing the Rules: A Pragmatic Approach to Product Development," Vol. 5, No. 4 (1993)
- Pitkin, Richard P.**, "The DECnet/SNA Gateway Product—A Case Study in Cross Vendor Networking," Vol. 1, No. 3 (1986); "Modeling and Analysis of the DECnet/SNA Gateway," Vol. 1, No. 9 (1989)
- Polich, Herman D.**, "VAXsimPLUS, A Fault Manager Implementation," Vol. 1, No. 8 (1989)
- Porcher, Thomas**, "X Window Terminals," Vol. 3, No. 4 (1991)
- Porter, Brian**, "VAX 6000 Error Handling: A Pragmatic Approach," Vol. 4, No. 3 (1992)

- Porter, David, "The DECnet/SNA Gateway Product—A Case Study in Cross Vendor Networking," Vol. 1, No. 3 (1986)
- Pouffary, Yanick, "The DECnet/OSI for OpenVMS Version 5.5 Implementation," Vol. 5, No. 1 (1993)
- Powers, Thomas E., "The Common Printer Access Protocol," Vol. 3, No. 4 (1991)
- Pratt, Kathleen L., "Floating Point in the VAX 8800 Family," Vol. 1, No. 4 (1987)
- Preston, Ronald P., "The NVAX CPU Chip: Design Challenges, Methods and CAD Tools," Vol. 4, No. 3 (1992)
- Priore, Donald A., "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Quaynor, Nii N., "The VAX 8600 I Box, A Pipelined Implementation of the VAX Architecture," Vol. 1, No. 1 (1985); "System Level Performance of VAX 8974 and 8978 Systems," Vol. 1, No. 5 (1987); "CI Bus Arbitration Performance in a VAXcluster System," Vol. 1, No. 5 (1987)
- Raghavan, Ananth, "Database Availability for Transaction Processing," Vol. 3, No. 1 (1991)
- Raj, Jain, "Performance Analysis of FDDI," Vol. 3, No. 3 (1991)
- Rajagopalan, Vidya, "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Ramakrishnan, K. K., "High-performance TCP/IP and UDP/IP Networking in DEC OSF/1 for Alpha AXP," Vol. 5, No. 1 (1993)
- Ramey, Delvan A., "Digital's DECchip 21066: The First Cost-focused Alpha AXP Chip," Vol. 6, No. 1 (1994)
- Rannenbergh, Wendy, "The X/Open Internationalization Model," Vol. 5, No. 3 (1993)
- Rege, Satish L., "The Architecture and Implementation of a High-performance FDDI Adapter," Vol. 3, No. 3 (1991)
- Reisert, James J., "The Design of the DEC 3000 AXP Systems, Two High-performance Workstations," Vol. 4, No. 4 (1992)
- Rengarajan, T. K., "High Availability Mechanisms of VAX DBMS Software," Vol. 1, No. 8 (1989); "Database Availability for Transaction Processing," Vol. 3, No. 1 (1991); "Designing an Optimized Transaction Commit Protocol," Vol. 3, No. 1 (1991); "The Design of Multimedia Object Support in DEC Rdb," Vol. 5, No. 2 (1993); "Performance of DEC Rdb Version 6.0 on AXP Systems," Vol. 6, No. 1 (1994)
- Richardson, Llanda M., "Numerical Device and Process Simulation Tools in Transistor Design," Vol. 4, No. 2 (1992)
- Rickard, Pamela J., "DECnet for OpenVMS AXP: A Case History," Vol. 4, No. 4 (1992)
- Riley, Mark F., "The Design of Multimedia Object Support in DEC Rdb," Vol. 5, No. 2 (1993)
- Rizzolo, Anthony J., "Design of the PATHWORKS for ULTRIX File Server," Vol. 4, No. 1 (1992)
- Robinson, David C., "An Implementation of the OSI Upper Layers and Applications," Vol. 5, No. 1 (1993)
- Robinson, Scott G., "Binary Translation," Vol. 4, No. 4 (1992)
- Roden, Robert J., "Frame Relay Networks," Vol. 5, No. 1 (1993)
- Rodwell, Karen E., "A Relational Database Management System for Production Applications," Vol. 1, No. 8 (1989)
- Rogers, Thomas K., "Performance Evaluation of Transaction Processing Systems," Vol. 3, No. 1 (1991)
- Rogers, William J., Jr., "Vector Processing on the VAX 9000 System," Vol. 2, No. 4 (1990)
- Rokicki, John C., "The Design of ManageWORKS: A User Interface Framework," Vol. 6, No. 4 (1994)
- Rosenbluth, Mark B., "Digital's DECchip 21066: The First Cost-focused Alpha AXP Chip," Vol. 6, No. 1 (1994)
- Ross, Lorain M., "CMOS-4 Back-end Process Development for a VLSI 0.75  $\mu$ m Triple-level Interconnection Technology," Vol. 4, No. 2 (1992)
- Rost, Randi J., "PEX: A Network-transparent Three-dimensional Graphics System," Vol. 2, No. 3 (1990)
- Rubino, Michael S., "Performance of DEC Rdb Version 6.0 on AXP Systems," Vol. 6, No. 1 (1994)
- Russo, Andrew P., "The AlphaServer 2100 I/O Subsystem," Vol. 6, No. 3 (1994)
- Ryan, Daniel J., Jr., "The DECnet/OSI for OpenVMS Version 5.5 Implementation," Vol. 5, No. 1 (1993)
- Ryan, Michael R., "The Development of DECwindows VMS Mail," Vol. 2, No. 3 (1990)
- Sadowski, Siegbert, "Margin Analysis on Magnetic Disk Recording Channels," Vol. 1, No. 8 (1989)
- Salafia, Leonard J., "The Unique Features of the VAX 9000 Power System Design," Vol. 2, No. 4 (1990)
- Salet, Ronald M., "VAX Instructions That Illustrate the Architectural Features of the VAX 9000 CPU," Vol. 2, No. 4 (1990)
- Saltz, Jeffrey S., "Programmer Productivity Aspects of the VAX GKS and VAX PHIGS Products," Vol. 1, No. 6 (1988)
- Samaras, William A., "The CPU Clock System in the VAX 8800 Family," Vol. 1, No. 4 (1987)
- Samudrala, Sridhar, "An Overview of the VAX 6000 Model 400 Chip Set," Vol. 2, No. 2 (1990); "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Santhanam, Sribalan, "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Sawyer, David S., "An Overview of the Common Node Software," Vol. 3, No. 2 (1991)
- Schiebl, Christian O., "Numerical Device and Process Simulation Tools in Transistor Design," Vol. 4, No. 2 (1992)
- Schneider, Guenter E., "The TK50 Cartridge Tape Drive," Vol. 1, No. 2 (1986)
- Schriesheim, Jeffrey A., "The DECnet-ULTRIX Software," Vol. 1, No. 3 (1986)



- Seavey, Marden H., "Numerical Device and Process Simulation Tools in Transistor Design," Vol. 4, No. 2 (1992)
- Seger, Mark J., "The Evolution of Network Management Products," Vol. 1, No. 3 (1986)
- Senerchia, David C., "The Memory System in the VAX 8800 Family," Vol. 1, No. 4 (1987)
- Shah, Sanjiv M., "The KAP Parallelizer for DEC Fortran and DEC C Programs," Vol. 6, No. 3 (1994)
- Shand, I. Michael C., "Routing Architecture," Vol. 5, No. 1 (1993)
- Sherwood, Will, "VAX 6000 Model 400 CPU Chip Set Functional Design Verification," Vol. 2, No. 2 (1990)
- Shikarpur, Uttam N., "High-performance TCP/IP and UDP/IP Networking in DEC OSF/1 for Alpha AXP," Vol. 5, No. 1 (1993)
- Shirron, Stephen F., "The RQDX3 Design Project," Vol. 1, No. 2 (1986); "Design and Performance of the DEC 4000 AXP Departmental Server Computing Systems," Vol. 4, No. 4 (1992)
- Shurtleff, David G., "Network Management," Vol. 5, No. 1 (1993)
- Sichel, Peter A., "ACCESS.bus, an Open Desktop Bus," Vol. 3, No. 4 (1991)
- Sicola, Stephen J., "The Architecture and Design of HS-series StorageWorks Array Controllers," Vol. 6, No. 4 (1994)
- Sidman, Michael D., "Control Systems Technology in Digital's Disk Drives," Vol. 1, No. 8 (1989)
- Simcoe, Robert J., "The MicroVAX 78132 Floating Point Chip," Vol. 1, No. 2 (1986); "GIGAswitch System: A High-performance Packet-switching Platform," Vol. 6, No. 1 (1994)
- Simone, Guido, "Design of the Turbo PrintServer 20 Controller," Vol. 3, No. 4 (1991)
- Singer, Arthur L., "The Role of Computer-aided Engineering in the Design of the VAX 6200 System," Vol. 1, No. 7 (1988)
- Sinkewicz, Ursula, "ULTRIX Fiber Distributed Data Interface Networking Subsystem Implementation," Vol. 3, No. 2 (1991)
- Sites, Richard L., "Alpha AXP Architecture," Vol. 4, No. 4 (1992); "Binary Translation," Vol. 4, No. 4 (1992)
- Skakshober, D. John, "Vector Processing on the VAXvector 6000 Model 400," Vol. 2, No. 2 (1990)
- Slater, Debra L., "Vector Processing on the VAXvector 6000 Model 400," Vol. 2, No. 2 (1990)
- Smelser, Craig, "ULTRIX Fiber Distributed Data Interface Networking Subsystem Implementation," Vol. 3, No. 2 (1991)
- Smith, Alan B., "Magnetic Domain Observations in Thin-film Heads Using Kerr Microscopy," Vol. 1, No. 8 (1989)
- Snaman, William E., Jr., "The VAX/VMS Distributed Lock Manager," Vol. 1, No. 5 (1987); "Application Design in a VAXcluster System," Vol. 3, No. 3 (1991)
- Soleimani, Hamid R., "Numerical Device and Process Simulation Tools in Transistor Design," Vol. 4, No. 2 (1992)
- Souza, Robert J., "GIGAswitch System: A High-performance Packet-switching Platform," Vol. 6, No. 1 (1994)
- Sovie, Dean A., "Design of the VAX 4000 Model 400, 500, and 600 Systems," Vol. 4, No. 3 (1992)
- Speer, Thomas G., "Digital's Transaction Processing Monitors," Vol. 3, No. 1 (1991)
- Spence, Martha L., "The DECnet-DOS System," Vol. 1, No. 3 (1986)
- Spine, Thomas M., "The Evolution of the X User Interface Style," Vol. 2, No. 3 (1990)
- Spinney, Barry A., "FDDI Data Link Development," Vol. 3, No. 2 (1991); "GIGAswitch System: A High-performance Packet-switching Platform," Vol. 6, No. 1 (1994)
- Spiro, Peter M., "High Availability Mechanisms of VAX DBMS Software," Vol. 1, No. 8 (1989); "Designing an Optimized Transaction Commit Protocol," Vol. 3, No. 1 (1991); "Porting Digital's Database Management Products to the Alpha AXP Platform," Vol. 4, No. 4 (1992); "Performance of DEC Rdb Version 6.0 on AXP Systems," Vol. 6, No. 1 (1994)
- Spitz, Rick, "The Making of a MicroVAX Workstation," Vol. 1, No. 2 (1986)
- Stamm, Rebecca L., "The VAX 6000 Model 400 Scalar Processor Module," Vol. 2, No. 2 (1990); "The NVAX and NVAX+ High-performance VAX Microprocessors," Vol. 4, No. 3 (1992)
- Stewart, Lawrence C., "The Alpha Demonstration Unit: A High-performance Multiprocessor for Software and Chip Development," Vol. 4, No. 4 (1992)
- Stewart, Robin L., "The Design of the DEC 3000 AXP Systems, Two High-performance Workstations," Vol. 4, No. 4 (1992)
- Stockdale, Richard E., "Design of the DEC LANcontroller 400 Adapter," Vol. 3, No. 3 (1991)
- Storm, Mark W., "Digital's Transaction Processing Monitors," Vol. 3, No. 1 (1991)
- Strecker, William D., "The VAXcluster Concept: An Overview of a Distributed System," Vol. 1, No. 5 (1987)
- Strutt, Colin, "Terminal Servers on Ethernet Local Area Networks," No. 3 (1986); "Design of the DECmcc Management Director," Vol. 5, No. 1 (1993)
- Sullivan, David J., "The DECnet/OSI for OpenVMS Version 5.5 Implementation," Vol. 5, No. 1 (1993)
- Sullivan, Patrick, "The VAX 6000 Model 400 Scalar Processor Module," Vol. 2, No. 2 (1990)
- Sung, Alan, "The Design and Development of the DECdecision Product," Vol. 2, No. 1 (1990)
- Supnik, Robert M., "The MicroVAX 78032 Chip, A 32-Bit Microprocessor," Vol. 1, No. 2 (1986)
- Sweeney, John C., "VAX 6000 Model 400 Physical Technology," Vol. 2, No. 2 (1990)

- Sweet, Bruce E., "DECelms—Managing Digital's FDDI and Ethernet Extended Local Area Networks," Vol. 3, No. 2 (1991)
- Swiatowiec, Frank J., "HDSC and Multichip Unit Design and Manufacture," Vol. 2, No. 4 (1990)
- Swist, James A., "Design of the DECMCC Management Director," Vol. 5, No. 1 (1993)
- Sylor, Mark W., "The Evolution of Network Management Products," Vol. 1, No. 3 (1986); "The NMCC/DECnet Monitor Design," Vol. 1, No. 3 (1986); "Network Management," Vol. 5, No. 1 (1993)
- Takizawa, Kuniaki, "Japanese Input Method Independent of Applications," Vol. 5, No. 3 (1993)
- Taylor, Deborah, "Frame Relay Networks," Vol. 5, No. 1 (1993) Vol. 5, No. 4 (1993)
- Taylor, Bruce J., "DEC TP WORKcenter: A Software Process Case Study," Vol. 5, No. 4 (1993)
- te Kieft, Jan B., "The Megadoc Image Document Management System," Vol. 5, No. 2 (1993)
- Templin, Fred L., "ULTRIX Fiber Distributed Data Interface Networking Subsystem Implementation," Vol. 3, No. 2 (1991)
- Thacker, Charles P., "The Alpha Demonstration Unit: A High-performance Multiprocessor for Software and Chip Development," Vol. 4, No. 4 (1992)
- Thiel, David W., "The VAX/VMS Distributed Lock Manager," Vol. 1, No. 5 (1987)
- Thierauf, Stephen C., "Circuit Implementation of a 300-MHz 64-bit Second-generation CMOS Alpha CPU," Vol. 7, No. 1 (1995)
- Thomas, Benjamin J., III, "Porting OpenVMS from VAX to Alpha AXP," Vol. 4, No. 4 (1992)
- Thomas, Robert E., "GIGAswitch System: A High-performance Packet-switching Platform," Vol. 6, No. 1 (1994)
- Thompson, Bruce W., "Development of the FDDI Physical Layer," Vol. 3, No. 2 (1991)
- Thomson, Robert G., "Assessing the Quality of OpenVMS AXP: Software Measurement Using Subjective Data," Vol. 5, No. 4 (1993); "Improving Process to Increase Productivity While Assuring Quality: A Case Study of the Volume Shadowing Port to OpenVMS AXP," Vol. 6, No. 1 (1994)
- Turner, Martin, "Numerical Device and Process Simulation Tools in Transistor Design," Vol. 4, No. 2 (1992)
- Tiffany, William J., "The DECconcentrator 500 Product," Vol. 3, No. 2 (1991)
- Towning, Stephen, "FDDI Data Link Development," Vol. 3, No. 2 (1991)
- Travis, Robert L., Jr., "CDA Overview," Vol. 2, No. 1 (1990); "The Digital Document Interchange Format," Vol. 2, No. 1 (1990)
- Treggiari, Leo P., "Development of the XUI Toolkit," Vol. 2, No. 3 (1990)
- Trehan, Vijay, "DECdta—Digital's Distributed Transaction Processing Architecture," Vol. 3, No. 1 (1991)
- Troiani, Mario, "The VAX 8600 I Box, A Pipelined Implementation of the VAX Architecture," Vol. 1, No. 1 (1985)
- Uhler, G. Michael, "An Overview of the VAX 6000 Model 400 Chip Set," Vol. 2, No. 2 (1990); "The NVAX and NVAX+ High-performance VAX Microprocessors," Vol. 4, No. 3 (1992)
- Ulichney, Robert, "Video Rendering," Vol. 5, No. 2 (1993); "Software Motion Pictures," Vol. 5, No. 2 (1993)
- Vaccaro, Anthony J., "Test and Qualification of the VAX 6000 Model 400 System," Vol. 2, No. 2 (1990)
- Vaillette, Gary, "Design of the Turbo PrintServer 20 Controller," Vol. 3, No. 4 (1991)
- VanGilder, James H., "The Development of DECwindows VMS Mail," Vol. 2, No. 3 (1990)
- van Hunnik, Theo H., "The Megadoc Image Document Management System," Vol. 5, No. 2 (1993)
- van Ingen, Catharine, "Technical Description of the DEC 7000 and DEC 10000 AXP Family," Vol. 4, No. 4 (1992)
- VanNoy, Jacob L., "The Evolution of the X User Interface Style," Vol. 2, No. 3 (1990)
- Viscarola, Peter G., "The WAVE Tools Base for Protocol Testing," Vol. 1, No. 9 (1989)
- Von Ehren, Rekha D., "System Level Performance of VAX 8974 and 8978 Systems," Vol. 1, No. 5 (1987)
- Wade, Nicholas, "An Overview of the VAX 6000 Model 400 Chip Set," Vol. 2, No. 2 (1990)
- Wade, Paul C., "The VAXBI Bus—A Randomly Configurable Design," Vol. 1, No. 4 (1987)
- Walker, Martin, "A Shared Memory MPP from Cray Research," Vol. 6, No. 2 (1994)
- Walsh, Robert J., "GIGAswitch System: A High-performance Packet-switching Platform," Vol. 6, No. 1 (1994)
- Wang, Tzyh-Jong, "System Level Performance of VAX 8974 and 8978 Systems," Vol. 1, No. 5 (1987)
- Warchol, Nicholas A., "The RQDX3 Design Project," Vol. 1, No. 2 (1986); "Design and Performance of the DEC 4000 AXP Departmental Server Computing Systems," Vol. 4, No. 4 (1992)
- Watkins, Jeffrey E., "The WAVE Tools Base for Protocol Testing," Vol. 1, No. 9 (1989)
- Wattum, Scott A., "An Implementation of the OSI Upper Layers and Applications," Vol. 5, No. 1 (1993)
- Weber, Larry B., "Compiler Optimization in RISC Systems," Vol. 2, No. 2 (1990)
- Weiss, Judy B., "Design of the DEC LANcontroller 400 Adapter," Vol. 3, No. 3 (1991)
- Welch, Daniel J., "CMOS-4 Back-end Process Development for a VLSI 0.75  $\mu\text{m}$  Triple-level Interconnection Technology," Vol. 4, No. 2 (1992)
- Wells, Philip J., "The Development of an Optimized PATHWORKS Transport Interface," Vol. 4, No. 1 (1992)

- Wenners, Thomas M., "The VAX 6000 Model 600 Processor," Vol. 4, No. 3 (1992); "Development of Digital's PCI Chip Sets and Evaluation Kit for the DECchip 21064 Microprocessor," Vol. 6, No. 2 (1994)
- Weyant, Thomas F., "VAXcluster Availability Modeling," Vol. 1, No. 5 (1987)
- Wheeler, William R., "The MicroVAX 78132 Floating Point Chip," Vol. 1, No. 2 (1986); "The NVAX CPU Chip: Design Challenges, Methods and CAD Tools," Vol. 4, No. 3 (1992)
- Wiecek, Cheryl A., "The Simulation of Processor Performance for the VAX 8800 Family," Vol. 1, No. 4 (1987)
- Wilde, Kathleen M., "High-performance TCP/IP and UDP/IP Networking in DEC OSF/1 for Alpha AXP," Vol. 5, No. 1 (1993)
- Wilhelm, Neil C., "Development of the DECstation 3100," Vol. 2, No. 2 (1990)
- Williams, Douglas D., "Vector Processing on the VAXvector 6000 Model 400," Vol. 2, No. 2 (1990)
- Winsor, Catherine F., "Hardware Accelerators for Bitonal Image Processing," Vol. 3, No. 4 (1991)
- Winston, Jeff, "The System Support Chip, a Multi-function Chip for CVAX Systems," Vol. 1, No. 7 (1988)
- Winters, Gayn B., "International Distributed Systems—Architectural and Practical Issues," Vol. 5, No. 3 (1993)
- Witek, Richard T., "The MicroVAX 78032 Chip, A 32-Bit Microprocessor," Vol. 1, No. 2 (1986); "A 200-MHz 64-bit Dual-issue CMOS Microprocessor," Vol. 4, No. 4 (1992)
- Wixon, Dennis R., "Changing the Rules: A Pragmatic Approach to Product Development," Vol. 5, No. 4 (1993)
- Wolrich, Gilbert M., "Development of the CVAX Floating Point Chip," Vol. 1, No. 7 (1988)
- Woodward, James A., "DEC OSF/1 Version 3.0 Symmetric Multiprocessing Implementation," Vol. 6, No. 3 (1994)
- Woog, Alexandra, "An Open, Distributable, Three-tier, Client-Server Architecture with Transaction Semantics," Vol. 7, No. 1 (1995)
- Wright, William A., "High Availability Mechanisms of VAX DBMS Software," Vol. 1, No. 8 (1989)
- Yang, Henry S., "FDDI Data Link Development," Vol. 3, No. 2 (1991)
- Yau, Michael M. T., "Supporting the Chinese, Japanese, and Korean Languages in the OpenVMS Operating System," Vol. 5, No. 3 (1993)
- Yetto, Lawrence, "The DECnet/OSI for OpenVMS Version 5.5 Implementation," Vol. 5, No. 1 (1993)
- Yoder, Gregory L., "Vector Processing on the VAX 9000 System," Vol. 2, No. 4 (1990)
- Yodlowski, Robert AJ, "Development of the CVAX Floating Point Chip," Vol. 1, No. 7 (1988)
- Yoshioka, Hiroataka, "Character Internationalization in Databases: A Case Study," Vol. 5, No. 3 (1993)
- Young, Carol A., "The Digital Table Interchange Format," Vol. 2, No. 1 (1990); "The Design and Development of the DECdecision Product," Vol. 2, No. 1 (1990)
- Yu, Eugene L., "The Memory System in the VAX 8800 Family," Vol. 1, No. 4 (1987)
- Ywoskus, John A., "Local Area VAXcluster Systems," Vol. 1, No. 5 (1987)
- Zaaf, Driss, "Defining Global Requirements with Distributed QFD," Vol. 5, No. 4 (1993)
- Zahavi, William Z., "Tools and Techniques for Preliminary Sizing of Transaction Processing Applications," Vol. 3, No. 1 (1991)
- Zalewski, Stephen, "The Making of a MicroVAX Workstation," Vol. 1, No. 2 (1986)
- Zetterlund, Bjorn, "Microprocessor Performance and Process Complexity in CMOS Technologies," Vol. 4, No. 2 (1992)
- Ziman, Linda, "Project Management of the VAX DEC/Test Manager Software Version 2.0," Vol. 1, No. 6 (1988)
- Zurawski, John H. P., "Floating Point in the VAX 8800 Family," Vol. 1, No. 4 (1987)

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