

DTE20 TEN-ELEVEN INTERFACE UNIT DESCRIPTION

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PREFACE

This manual contains three levels of DTE theory descriptions. The three levels are:

1. Overview – The overview introduces and identifies, in a simplified fashion, the basic hardware organization of the DTE Console Processor Interface. The major elements are presented without extensive details in order to provide a capsule view of the DTE structure.
2. Functional Description – This section describes the primary DTE function, which is to interface “front end” PDP-11 processors to the KL10 Central Processor. In such a system, several front end functions are thus provided, some of which are:
 - a. Handling unit record equipment
 - b. Handling communications equipment
 - c. Diagnosing the KL10 Central Processor
 - d. Bootstrapping the KL10 system.

In addition to front end functions, the DTE features other capabilities. Some of these capabilities are:

- a. Examine and Deposit console functions
- b. Doorbell function, where the PDP-11 can interrupt the KL10 and vice versa
- c. High speed simultaneous two-way variable byte data transfer between the PDP-11 and KL10 memory.

The functional description is the most comprehensive part of the DTE theory. Here, the basic elements of the DTE are described in the context of how they implement the primary DTE operations.

3. Logic Description – This section provides a detailed logic description of the DTE. The text is written to support the functional description. The logic description section is the most detailed part of the manual. This material is presented to expand the functional description so that the information provided in the functional description may be directly related to the engineering logic diagrams.

SECTION 1 OVERVIEW

1.1 INTRODUCTION

Each central processor in a KL10 system may have from one to four PDP-11 processors attached, each serving as a "front end" processor. Each PDP-11 is connected to the KL10 by a separate interface called the DTE20 Console Processor Interface, or simply the 10-11 Interface. The following are some of the possible front end functions:

1. Handling unit record equipment
2. Handling asynchronous communications equipment
3. Handling synchronous communications equipment
4. Providing a long term power line frequency clock
5. Diagnosing the KL10 Central Processor and other functional components in the system
6. Running a dedicated real-time data acquisition system
7. Bootstrapping the KL10 system.

In terms of basic features, the DTE20 generates parity for Deposit data and detects parity errors for both Examine data and byte transfers over the EBus. The DTE20 connects to the PDP-11 as a standard Unibus peripheral and communicates via interrupt or device address. Up to four DTE20s may be connected to a PDP-11. In a system consisting of four KL10 Central Processors, there may be four PDP-11/40 processors, where each processor can communicate with all KL10s in the system. It is possible to have up to four DTE20s on each PDP-11 in the KL10 system, and each KL10 processor may have 1, 2, 3, or 4 DTE20s connected to it via the EBus.

The DTE20 uses the NPR (Direct Memory Access) and BR (Vector Interrupt) features of the PDP-11. In addition, the DTE20 contains logic to detect PDP-11 core memory parity errors during NPR transfers, provided that the memory being accessed contains the parity option (MFU11 UP).

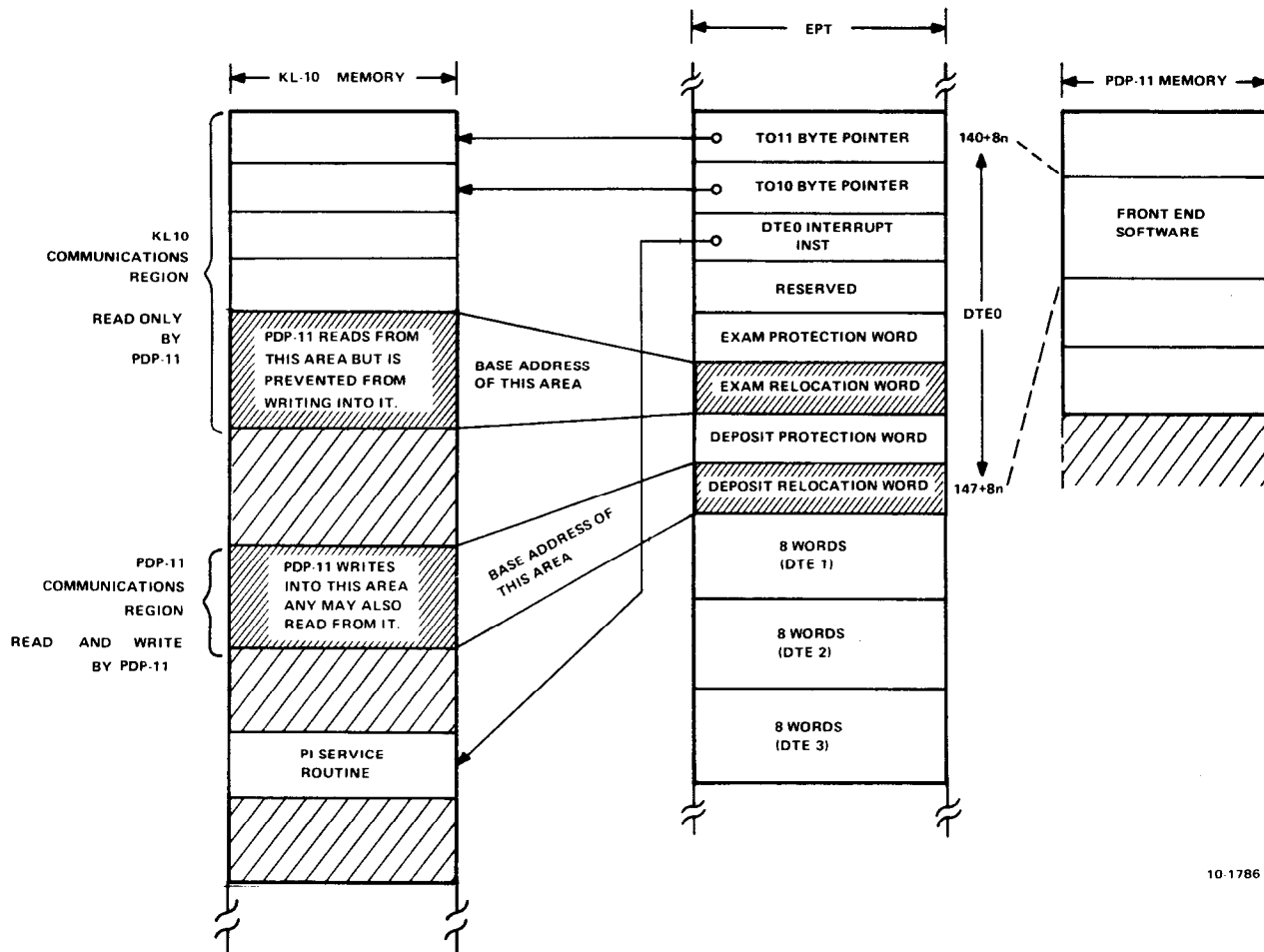
The DTE20 provides the following capabilities:

1. Console functions at Examine and Deposit, restricted or unrestricted.
2. Doorbell function, where the PDP-11 can interrupt the KL10 Central Processor and vice versa.
3. High speed simultaneous two-way transfer of variable byte data between the PDP-11 and KL10 memory.
4. Diagnostic bus for the PDP-11 to diagnose the KL10.
5. KL10-initiated bootstrap startup of the PDP-11 mechanism (diagnostic bus) to load the microcode into the CRAM, execute PDP-10 instructions, and start or stop the KL10 Central Processor.

The following terminology will give some perspective on the front end and its relationship to the DTE20.

PDP-11 Communication Region – This region consists of an area of KL10 core memory defined by the deposit relocation and protection word in the Executive Process Table (EPT). This area is written by the PDP-11 using protected deposits, and read by the KL10. It is used for coordination of status, preparing for byte transfer operations, and passing limited amounts of data. Each PDP-11 in the system has a separate communication region in the KL10 memory, which it alone can modify.

KL10 Communication Region – This region is defined solely by the KL10 software and is separate from the PDP-11 communication region. It can be written by the KL10, but may be read by the PDP-11 using protected Examines. This area is used to coordinate status, prepare byte transfer operations, and pass limited amounts of data (Figure 1-1).



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Figure 1-1 Overview Communications Region

Restricted Front End – A restricted front end is a PDP-11 system with a DTE20 that does not have diagnostic privileges. A restricted front end is prevented from using the diagnostic bus. A restricted front end can only access KL10 memory after the KL10 has performed a CONO (Conditions Out) to allow use of DTE PI0. After this has been done, the restricted front end can only examine or transfer bytes from the KL10 communication region and only deposit or transfer bytes to its own PDP-11 communication region.

Privileged Front End – A privileged front end is a PDP-11 attached to a KL10 via a DTE20 that can use the diagnostic bus and perform unrestricted Deposits.

Protected Examine or Deposit – A protected Examine or Deposit is an Examine or Deposit that is relocated and range checked by the KL10. The relocation and protection for Examine is separate from that of Deposit. A privileged front end can override the Examine and Deposit protection checks. A restricted front end cannot override these checks.

For addressing purposes, each controller is permanently assigned a unique device, or Controller Select (CS) code. A total of four Controller Select codes has been assigned because up to four controllers (interfaces) can be implemented in a KL10 system. Each interface is also assigned a physical number according to the physical slots in which the interface module will reside. These are indicated below. Both of these are hard-wired on the KL10 backplane. The specific Controller Select (CS) codes and physical number (n) assignments are as follows:

Interface	Controller Select (CS) Codes	Physical Number n_{10}
0	200	8
1	204	9
2	210	10
3	214	11

The device code is used to address the interface and the physical number is used to identify the interrupting interface.

Eight locations are assigned to each DTE20 in the KL10 Executive Process Table as follows:

Location	Name
$140 + 8*n$	To 11 Byte Pointer
$141 + 8*n$	To 10 Byte Pointer
$142 + 8*n$	DTE20 Interrupt Instruction
$143 + 8*n$	Reserved for DEC Hardware
$144 + 8*n$	Examine Protect Word
$145 + 8*n$	Examine Relocation Word
$146 + 8*n$	Deposit Protect Word
$147 + 8*n$	Deposit Relocation Word

NOTE: $n = 0, 1, 2$ or 3

Figure 1-2, API Word Format, illustrates the basic format of this word. The DTE20 allows the software to set the following fields of this 36-bit word:

Address Space Field 0-2
 Unused bits 11-12
 Address Field 13-35.

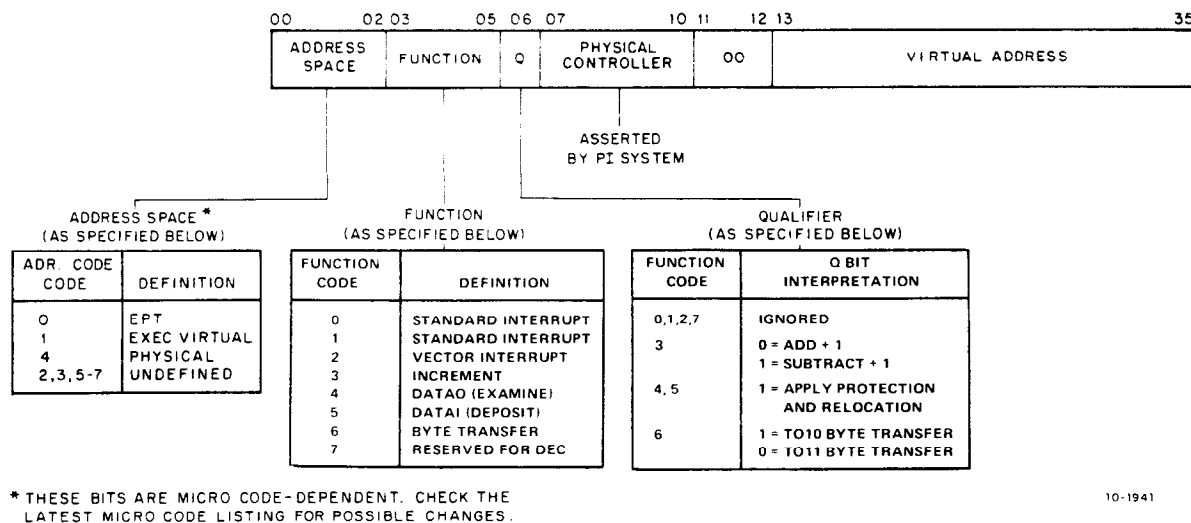


Figure 1-2 API Word Format

The Priority Interrupt (PI) board in the EBox supplies the physical controller number field [7-10]. The DTE20 asserts Qualifier (Q) bit 6, for all Examine and Deposits by a restricted front end, whether protected or not.

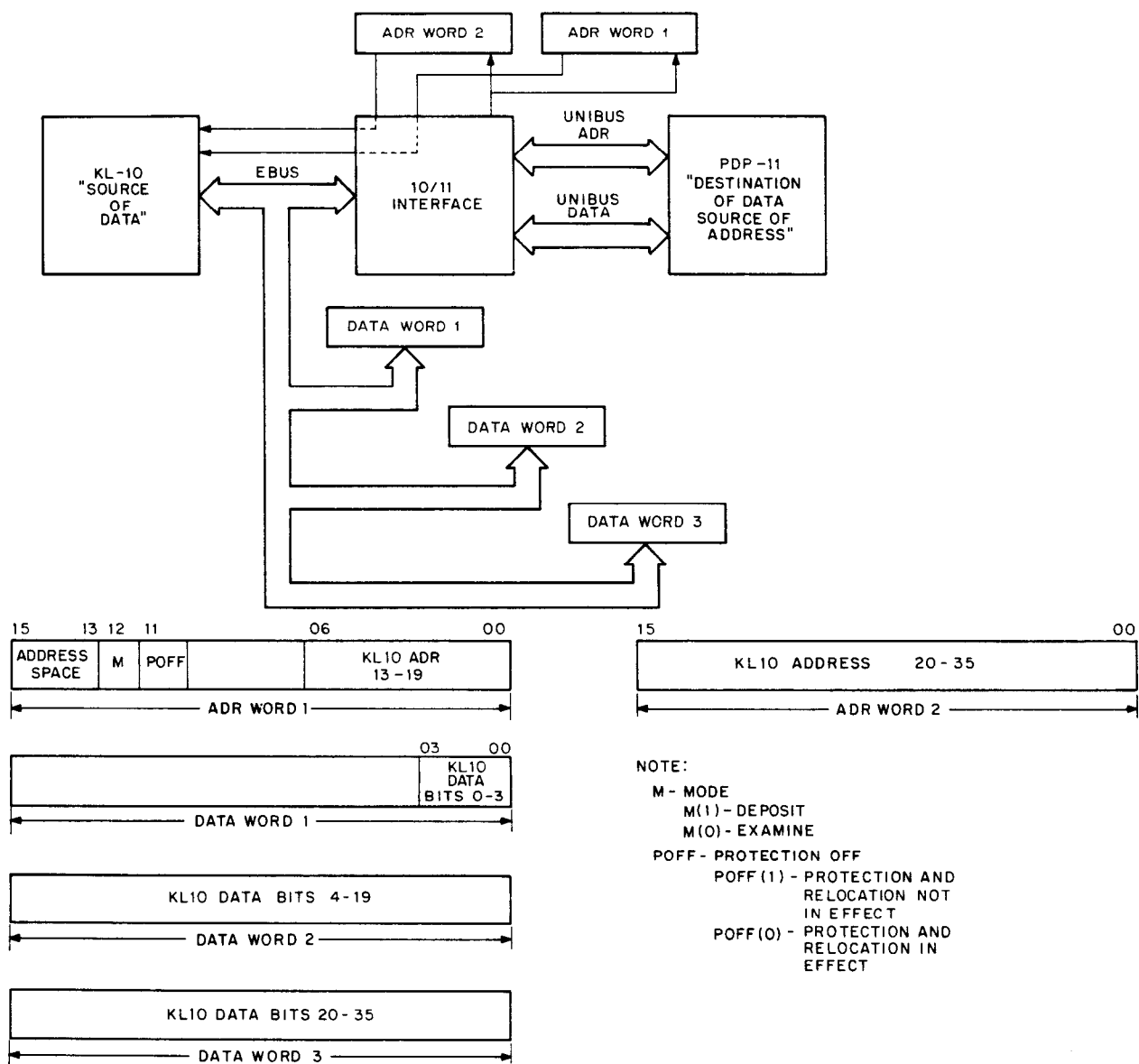
The DTE20 asserts Qualifier for all protected Examine and Deposits by a privileged front end and does not assert it if the privileged front end makes an unprotected Examine or Deposit.

1.2 BASIC PROGRAMMING OVERVIEW

To specify a 36-bit PDP-10 data word, three PDP-11 words are used. They are Deposit/Examine Data Word 1, Deposit/Examine Data Word 2, and Deposit/Examine Data Word 3.

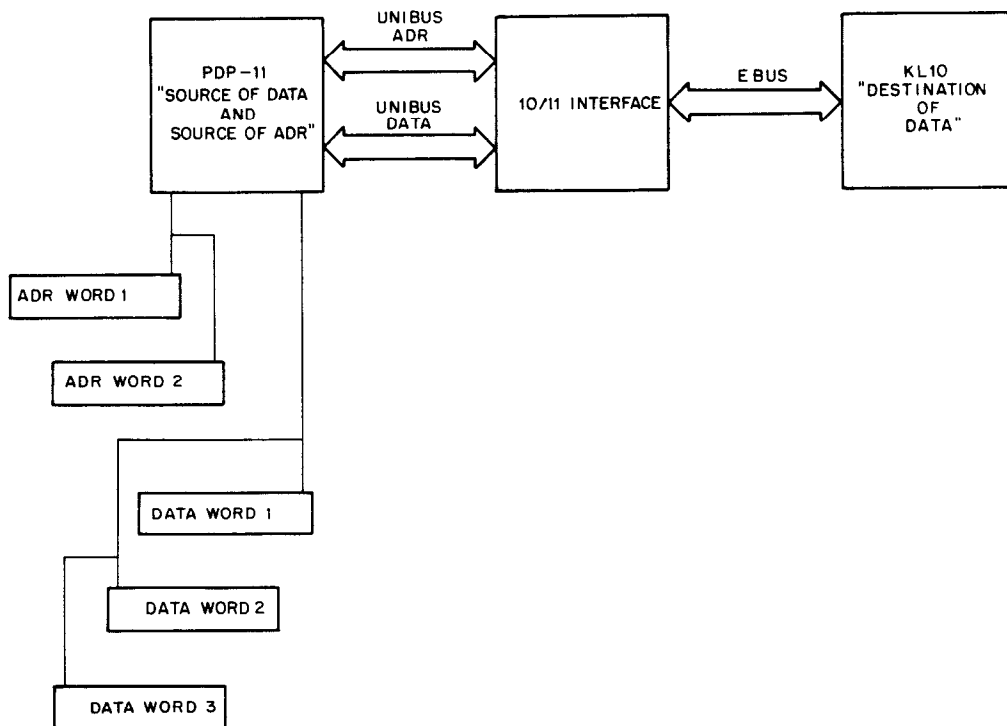
To specify a 23-bit PDP-10 address, two PDP-11 words are used. They are Ten Address Word 1 and Ten Address Word 2. The high order part of Ten Address Word 1 is used for control. Ten Address Word 1 specifies whether an Examine or Deposit is to be done. For a privileged front end, the protect off bit in the Ten Address Word 1 can be set by the software to allow an unprotected Examine or Deposit. On unprotected operations, the space field specifies the type of address: Executive Process Table (EPT), Exec Virtual, or Physical Address, which may refer to core memory or ACs.

The Examine or Deposit function is started when the PDP-11 program writes the Ten Address Word. No program interrupts are generated on the KL10 or the PDP-11 side to signal completion of the Examine or Deposit. Therefore, the PDP-11 program must check for completion by looking at the status DEXDONE bit. The DTE20 clears DEXDONE when the PDP-11 writes Ten Address Word 2, so the software never needs to. Data in TENAD1, TENAD2, DEXWD1, DEXWD2, DEXWD3 remain intact after an operation. Therefore, the PDP-11 may perform repeated protected Examine or Deposits merely by writing the TENAD2 word each time. An Examine followed by a Deposit (changing only TENAD1 and TENAD2) will result in moving data from one KL10 core location to another. For unprotected operations, the PDP-11 must reload the protect off bit (PRTOFF) between each operation (Figures 1-3 and 1-4).



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Figure 1-3 Examine Overview



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Figure 1-4 Deposit Overview

1.3 DOORBELL FUNCTION

The doorbell function allows each KL10 to interrupt each PDP-11 connected by a DTE20 and vice versa.

The doorbell consists of a programmable interrupt and a status bit. In order for the PDP-11 to interrupt the KL10, the PDP-11 sets the request 10 interrupt flip-flop (bit 08) in the PDP-11 status word. When this bit is set, the DTE20 generates an interrupt in the KL10 with a status bit set in the CONI word (bit 26) indicating that the PDP-11 CPU has programmed an interrupt of the KL10 (Figure 1-5).

This procedure works in a reversed but identical manner for the KL10 interrupting the PDP-11. The KL10 sets the 10 requesting 11 interrupt by doing a CONO to the DTE20. The PDP-11 discovers the cause for the interrupt by looking at bit TO10DB (bit 11) in status. Communication is done via a word (or words) in the communication region in KL10 memory. A word (or words) is chosen and Deposit and Examine features are used by the PDP-11 to gain access to these words (Figure 1-6).

This mechanism is used by either processor to indicate to the other processor that it is powering down. For example, if the KL10 determines that its power is disappearing, it will set a bit in a word that is assigned for power failure notification. The KL10 then interrupts the PDP-11. The PDP-11, as part of its standard routine, will always check for the KL10 power fail bit in the communication region. In this way, the PDP-11 is notified that the KL10 power is disappearing. In a similar way the PDP-11 could interrupt the KL10 on every tick of the power line clock (50 or 60 Hz).

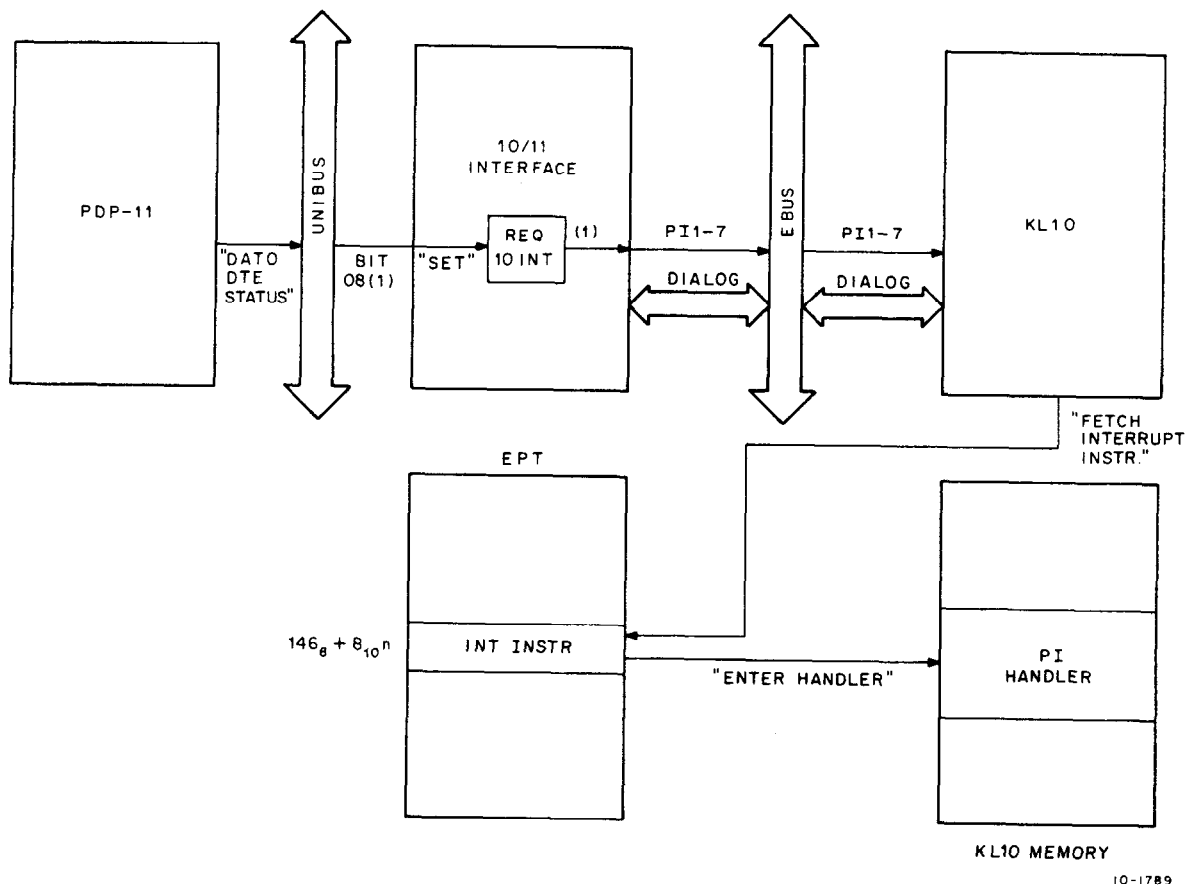


Figure 1-5 PDP-11 Rings KL10 Doorbell

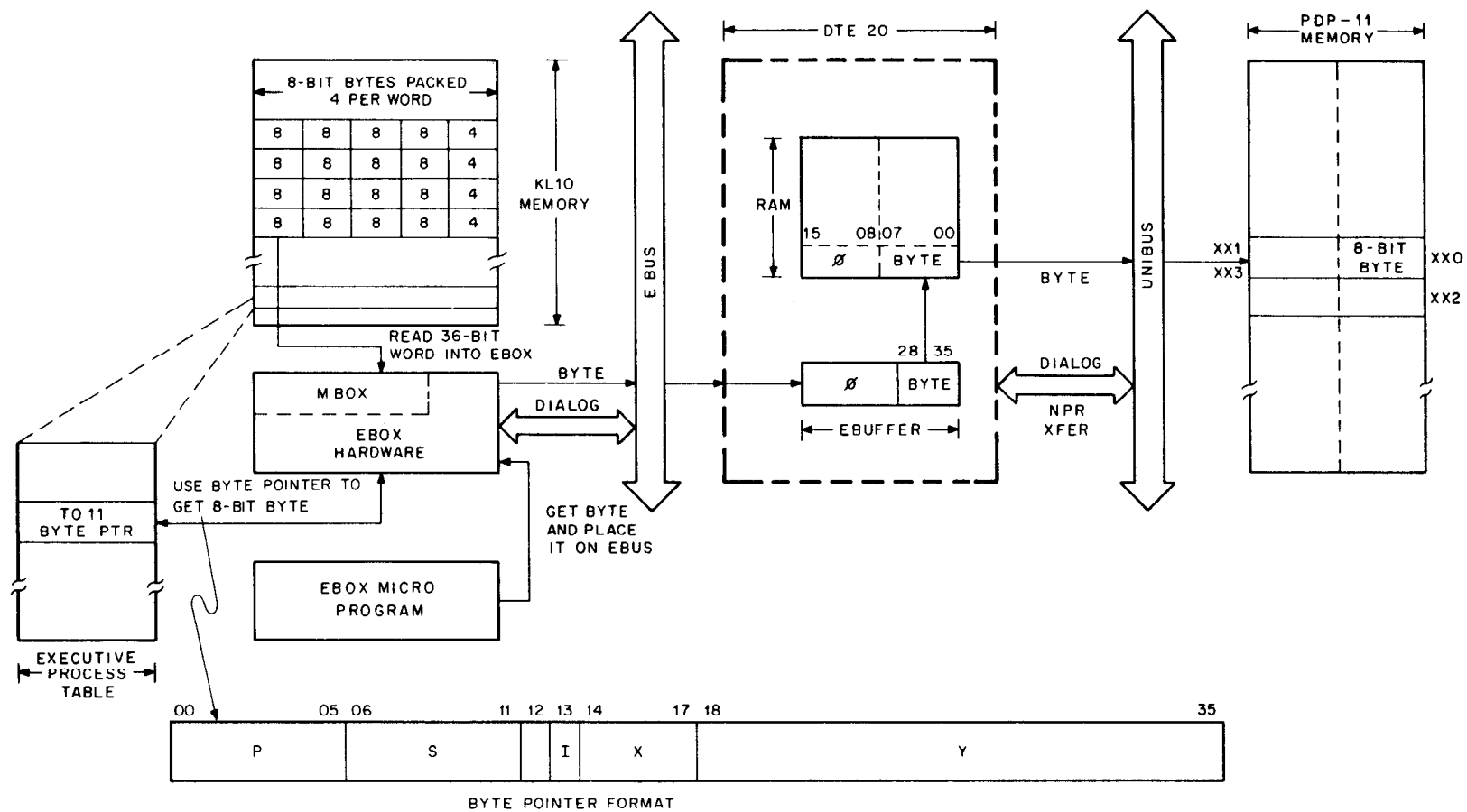


Figure 1-6 TO11 Byte Transfer Overview

1.4 BYTE TRANSFER FUNCTION

During the byte transfer function, the DTE20 transfers fields of information between the PDP-11 and the EBox. On the KL10 side, the fields are of variable length and are accessed through a PDP-10 byte pointer. On the PDP-11 side, the fields are either 8 bits wide and are stored in consecutive bytes or are 16 bits wide and are stored in consecutive words. If the field into which the information is being stored is narrower than the field from which it was read, as many of the rightmost bits as will fit are stored. If the field into which the information is being stored is wider than the field from which it was read, the information is right-aligned and padded with zeroes on the left.

To perform a transfer, the following actions must be done:

- The PDP-11 should specify the transfer rate (delay between transfers) and address bits 17-16 (this can be done once at system startup). If it is not specified, an undetermined transfer rate will occur to one of the four 32K memory regions.
- The PDP-11 must specify whether byte or word mode is to be used in the PDP-11.
- The sender must specify the address of the source string. The KL10 controls the address of the data either to or from the KL10 via byte pointers in the EPT. The PDP-11 controls the address on its side via two locations in the DTE (one word for each direction of transfer).
- The receiver must specify whether it alone (scatter write) or both CPUs are to receive normal termination interrupts (I bit = 1).

Information in the form of bytes may be stored in the PDP-11 as either one variable sized byte per PDP-11 16-bit word (1 to 16 bits of data) or one variable sized byte per 8-bit PDP-11 byte (1 to 8 bits of data). Byte addresses are specified in the KL10 using regular KL10 byte pointers in the EPT. Byte pointers are interpreted in Exec Virtual Address space.

CAUTION

The index field of the byte pointers should be zero. Otherwise, the EBox will index using the current contents of the Executive or User Index register at the time of the transfer. Indirection should not be used because the indirect word will not be incremented as with all byte pointer operations.

1.5 ERROR OVERVIEW

The DTE20 will generate/check parity on Deposit/Examine data (36 bits). It will not check or generate parity for CONI, CONO, DATAO, or API words. The software will check for errors by examining the termination words. The parity scheme also imposes one restriction on the byte pointer used for TO11 transfers. A byte size larger than 16 bits cannot be used unless the bits to the left of the rightmost 16 bits contain even parity. If a parity error occurs, the error termination bit status and the EBus parity error flag status will be set. If an Examine operation was in progress when a TO11 transfer operation has an error termination due to an EBus parity error, it is not possible for the software to determine if the Examine operation has a parity error. The EBus parity error is fatal, and is treated so by the Monitor. When a parity error occurs, the bad data is stored in the RAM and can be retrieved for error reporting. The DTE20 sometimes swaps the left and right bytes for byte mode prior to writing the bytes into the RAM. Therefore, the termination TO11 address word should be examined to determine if the left and right halves were swapped. If the termination address is even, the bytes were swapped. (This applies only to transfers in byte mode.)

1.6 DIAGNOSTIC OVERVIEW

The interface contains many features that enable diagnosing of the interface. It is designed to be diagnosed using three basic methods:

1. Without using or disturbing the EBus
2. With loopback on the EBus but without the KL10 or without the KL10 running
3. With the KL10 running.

The interface is primarily checked out in a single-step manner. Full speed operation may only be checked with a running KL10; DIAG1 contains the Diagnose 10/11 Interface bit. When DIAG1 is set, the following occurs. The interface clock is disabled and single step operation commences. Interrupts are inhibited from being sent to the KL10. The interface operates in the normal manner except that EBus operations never complete because no interrupts are issued to the KL10. Therefore, a bit is provided that enables setting EBus Complete, allowing the operation to continue.

The interface control is run by an up-counter and three decoders. The decoders are selected by the major state flip-flops. The up-counter is loadable by the rightmost four bits of DIAG Word 2. This enables any minor logic state to be executed. The major states are not loadable; however, they naturally cycle until a condition occurs that indicates the operation is ready to take place. These major state bits are readable.

1.6.1 Diagnosing the KL10

All KL10 diagnostic functions and console functions (except Deposit and Examine) are performed over the diagnostic portion of the EBus. This specification explains the operation of the diagnostic bus.

The diagnostic bus contains the following ten signal lines:

DS00-06	Diagnostic Select (DS) Lines – The PDP-11 sends encoded diagnostic functions to the KL10 on these lines. These lines can be read by the PDP-11 at any time, even while the rest of the EBus is active for other devices.
DIAG STROBE	Diagnostic Strobe – This line is asserted to indicate that the Diagnostic Select lines are stable, and that the indicated function should be performed.
DFUNC (Actual Mnemonic is Remove Status)	Diagnostic Function – When true, this causes the KL10 to disable the basic CPU status from the DS lines, switch the translator (only for the DS lines) to convert TTL to ECL, and put the EBus translator under control of DB bits 00 and 01.

1.6.1.1 Diagnostic Bus Control

Diagnostic CPU Status Read – All bits in DIAG Word 1 must be loaded with zeros. The CPU status may then be read from the DS lines after 1 μ s has been allowed for the lines to settle (Figure 1-7).

Diagnostic Functions Only (i.e., no 36-bit transfers) – The desired function code bits should be set along with DIAG Command Start (DIAG1 PDCOMST) and Remove Status (DIAG1 [DFUNC]). This will result in the function being sent to the KL10. When DIAG Command Start is a zero, the function has been sent. All function bits must be loaded with the desired value each time a new command is sent. The DIAG Send bit has no effect upon this operation. DIAG KL10 must not be set or a 36-bit data transfer will take place. This operation should not take more than 2.0 μ s.

1.6.1.2 Diagnostic Functions with 36-Bit Data Transfer

Sending Data to the KL10 – No other operations (i.e., byte string transfers) may be in progress while doing 36-bit diagnostic data transfers. The data should be loaded into DEX WD1-3 (same bit assignments as with a Deposit or Examine). DIAG KL10 should then be set and a Deposit operation should be started. When the transfer is complete (DEXDON SET), the diagnostic function should be loaded as described above, the DIAG KL10, DIAG Send, DIAG Command Start, and DIAG Function set. The operation is complete when DIAG Command Start is on a zero.

Receiving Data From the KL10 – The diagnostic function should be loaded with DIAG KL10 set, DFUNC set (Remove Status), DIAG Send clear, and DIAG Command Start set. When DIAG Command Start is clear, the function is complete and the data is in DEX WD1-3. No other operations (i.e., byte string transfers) may be in progress during this operation.

All the KL10 diagnostic functions are disabled when the privileged restricted mode switch is set to restricted mode. This bit can be tested by Reading Status (RM). When the switch is set to restricted mode, status (RM) is set (i.e., the device is restricted and cannot send diagnostic functions).

1.7 INTERFACE COMMUNICATION

The DTE20 can communicate directly with three devices in the system:

1. EBox via EBus
2. PDP-11 processor via Unibus
3. PDP-11 memory via Unibus.

This communication, when over the Unibus, is in a master-slave relationship (Figure 1-8). During any bus transfer, either the DTE20, the PDP-11 processor, or the PDP-11 memory has control of the bus. The controlling device is considered the bus master, and the device being controlled is considered the slave. Also, communication on the Unibus is interlocked between the DTE20 and either the PDP-11 processor or the memory. Each control signal issued by the master device must be acknowledged by a similar response from the slave device. Thus, communication is independent of bus length and of the response time between the master and the slave. When the DTE20 requests the bus, the handling of the request depends on the location of the interface in a priority structure. The following factors must be considered to determine the priority of the request:

1. The processor's priority is set under program control to one of eight levels using bits 7, 6, and 5 in the processor's Status register. These three bits set a priority level that inhibits granting bus requests (BR) on the same or lower levels.
2. Bus requests from external devices, i.e., DTE20 can be made on any one of five request lines. A non-processor request (NPR) has the highest priority and its request is granted by the processor between bus cycles of an instruction execution.
3. When more than one device is connected to the same bus request line, the one that is electrically closest to the PDP-11 processor has the higher priority.

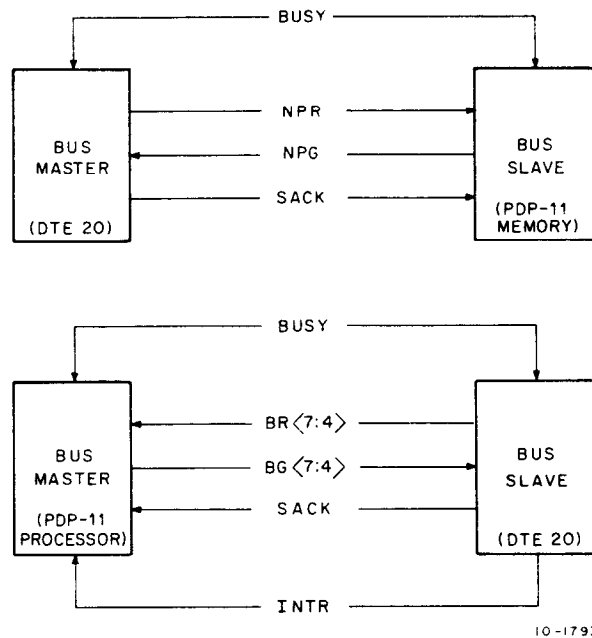


Figure 1-8 Master/Slave Relationship

1.7.1 Data Transfer

Direct memory access data transfers can be carried out by the DTE20 and memory without processor supervision.

This type of transfer is called NPR level data transfer. Normally, NPR transfers are only made between memory and controllers. During NPR transfers, it is not necessary for the PDP-11 processor to transfer the information between the memory and DTE20. The bus structure is such as to enable device-to-device transfers. This allows special controllers to access other devices on the bus as well as memory.

The DTE20 can transfer data at high rates once it gains control of the bus. In addition, the processor's internal state is not affected by this type of transfer. Therefore, the processor can release the bus while an instruction is in progress. The DTE20 can transfer 16-bit or 8-bit bytes to memory at the same speed as the memory cycle time.

1.7.2 Interrupt Requests

Once the DTE20 has gained control of the bus, it can take full advantage of the power and flexibility of the processor by requesting an interrupt. Note that interrupt requests can be made only if bus control has been gained through a BR priority level. An NPR level request cannot be used for an interrupt request.

1.7.2.1 Processor Interrupt Procedure – Assume that the DTE20 is responding to a CONO from the EBox and this CONO is activating the doorbell feature for interprocessor communication. The DTE20 must then interrupt the PDP-11 to inform it that the EBox wishes to communicate. Refer to Figure 1-9. The following takes place:

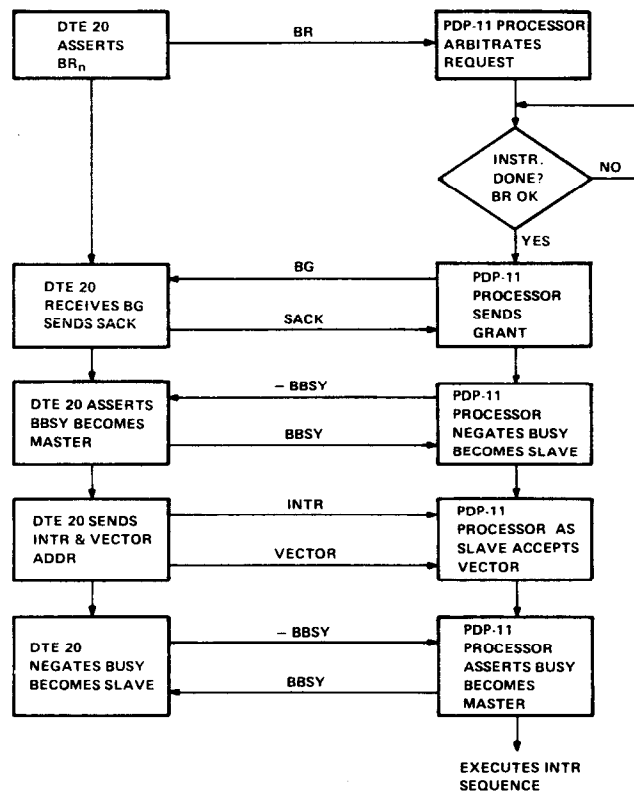
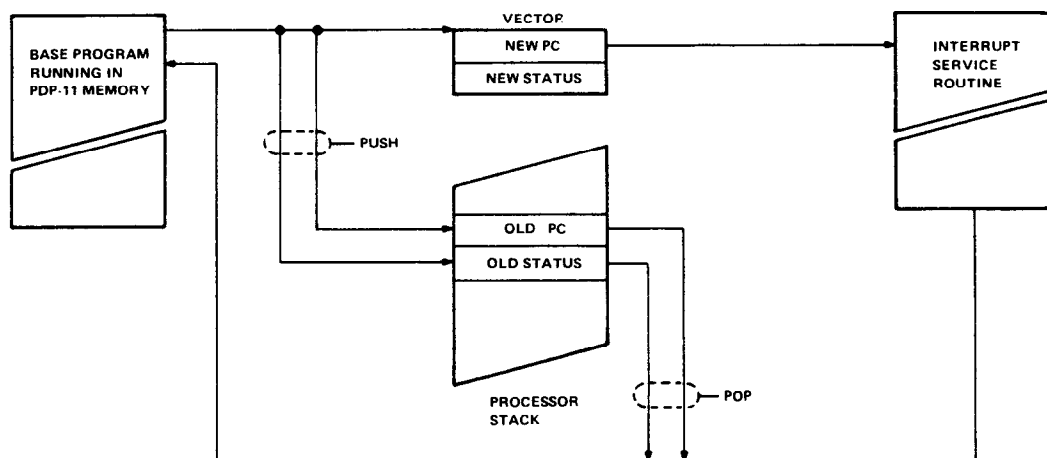
1. Priorities permitting, the processor relinquishes bus control to the DTE20.
2. When the DTE20 gains control of the bus, it sends the PDP-11 processor an interrupt command and the starting address of the device service routine. This is called the Interrupt Vector Address. Immediately following this address is a word to be used as the new processor status (PS) word.
3. The processor pushes the current processor status word and then the program counter (PC) value onto the processor stack. The stack is pointed to by register 6.
4. The new PC and PS (the interrupt vector) are taken from the address specified by the DTE20 and the service routine is initiated.
5. The service routine can cause the processor to resume the interrupted process by executing the return from interrupt (RTI) instruction, which pops the two top words from the processor stack and transfers them back to the PC and PS registers.

1.7.3 Unibus Signal Lines

The PDP-11 Unibus comprises 56 lines. All devices including the processor are connected to these lines in parallel. The bidirectional nature of 51 signal lines permits signals to flow in both directions. The remaining five lines are used for priority bus control. Table 1-1 lists the data transfer signals.

Table 1-1
Data Transfer Signals

Name	Mnemonic	No. of Lines
Data	D (15:00)	16
Address	A (17:00)	18
Control	C0, C1	2
Master Sync	MSYN	1
Slave Sync	SSYN	1
Parity	PA, PB	2
Interrupt	INTR	1
		Total: 41



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Figure 1-9 BR Sequence

Data Lines D(15:00) – The 16 data lines are used to transfer information between the DTE20 and either the PDP-11 processor or PDP-11 memory. The most significant bit is bit 15, the least significant is bit 00.

Address Lines A(17:00) – The 18 address lines are used by the DTE20 to select the PDP-11 memory address used in the current data transfer. The reason for 18 address lines is to extend the total memory capability to 262,144 bytes.

The extension bits are bits 17 and 16. The normal most significant bit is bit 15; the least significant bit is bit 00. Lines A(17:01) specify a unique 16-bit word. In byte operations, A00 specifies the byte being referenced. If a word is referenced as ADR (ADR must be even, because words can be addressed only on even boundaries), the low order byte can be referenced at ADR and the high order byte at ADR+1.

Only 16 bits are supplied by programs as memory references. In the processor, lines A17 and A16 are asserted (forced to 1) whenever the program attempts to reference an address between 160000 and 177777. Thus, the processor converts the 16-bit to a full 18-bit address.

Control Signals – The control signals are divided into three groups: signals that select data transfer operations, signals that allow the master and slave device to communicate, and signals used for parity checking.

1. **Control Lines C(1:0)** – These two bus signals are coded by the DTE20 as well as the PDP-11 processor to control the memory in one of four possible data transfer operations shown in Table 1-2.

Table 1-2
Data Transfer Operations

C1	C0	Operation
0	0	DATI -- data in
0	1	DATIP -- data in pause
1	0	DATO -- data out
1	1	DATOB -- data out byte

2. **Master and Slave Synchronization** – Master Synchronization (MSYN) is a control signal used by the master device to indicate to the slave device that address and control information is present. Slave Synchronization (SSYN) is the slave device response to the master.
3. **Parity Error Indicators** – The PA and PB are used to indicate that a memory parity error occurred on a memory read. The DTE sets the DPS5 MEM PAR ERR flag when a memory parity error is indicated during an NPR transfer initiated by the DTE.

Interrupt (INTR) – This signal is asserted by the DTE20 to start a priority interrupt in the processor.

1.7.3.1 Priority Transfer Lines – The Unibus contains 12 lines classified as priority transfer lines. Four of these are priority bus request lines BR(7:4) and four are the corresponding grant lines BG(7:4); NPG, NPR, SACK, and BBSY complement the priority transfer lines.

Each device of the same priority level passes a grant signal to the next device on the line, unless it has requested bus control; in this case, the requesting device blocks the signal from the following devices and assumes bus control. These 12 lines are described as follows:

1. Bus Request Lines BR(7:4) – These four bus signals are used by the DTE20 to request control of the bus.
2. Bus Grant BG(7:4) – These signals are the processor's response to a bus request. They are asserted only at the end of instruction execution, and in accordance with the priority determination.
3. Non-Processor Request (NPR) – This signal is the bus request from the DTE20 to the PDP-11 processor for a DMA-type bus cycle.
4. Non-Processor Grant (NPG) – This signal is the processor's response to an NPR.
5. Selection Acknowledge (SACK) – This signal is asserted by the DTE20 after receiving Bus Grant (BG). Bus control passes to the DTE20 as soon as the current bus master has completed its operation. If SACK is not received by the processor within 28 μ s of issuing BG, a timeout occurs and the Bus Grant is cleared automatically by the processor.
6. Bus Busy (BBSY) – This signal is asserted by the master, either the DTE20 or PDP-11 processor, to indicate that the bus is being used.

1.7.3.2 Miscellaneous Control Lines

Initialization (INIT) – This signal is asserted by the processor when the START key on the console is pressed, when a RESET instruction is executed, or when a power failure sequence occurs. In the later case, INIT is asserted following the power fail service routine while power is going down, and again when power comes up.

1.7.4 EBus Signal Lines

The EBus consists of 60 signal lines. All devices, including the KL10, are connected to these lines in parallel. The bidirectional nature of 36 of the signals permits some information to flow in both directions. These are the data lines. The remaining 24 signal lines are used for control functions. Table 1-3 lists the signals necessary to effect a data transfer.

Data Lines D(00:35) – The 36 data lines are used to transfer information between the EBox and the DTE20. The most significant bit is bit 00, the least significant bit is bit 35.

Controller Select Lines CS(00:06) – These seven lines are used to select the desired controller for a data transfer. Each controller has a unique select code that is hard-wired on the backplane of the device.

Table 1-3
Data Transfer Signals

Name	Mnemonic	No. of Lines
Data	D (00:35)	36
Controller Sel	CS (00:06)	7
Function	F (00:02)	3
Demand	DEM	1
Acknowledge	ACK	1
Transfer	XFER	1

Function Lines F(00:02) – The function lines specify the type of data transfer or non-data transfer that is to take place. Table 1-4 lists the four implemented functions.

Table 1-4
Data Transfer Commands

F00	F01	F02	Operation
0	0	0	CONO
0	0	1	CONI
0	1	0	DATAO
0	1	1	DATAI

DEMAND (DEM) – This signal line causes the addressed controller to sample the CS lines and the F lines and to decode their meaning. Upon implementing the specified function, TRANSFER and ACKNOWLEDGE are asserted as a response, along with data being placed onto or taken from the EBus as specified by the decoded function.

ACKNOWLEDGE (ACK) – This signal line is necessary to tell the DIA20 I/O Bus Adapter not to respond to the current operation. If the DIA20 does not see ACKNOWLEDGE some period of time after DEMAND is asserted, it will try to perform the transfer. It does not decode the CS lines, as do the standard KL10 devices.

TRANSFER (XFER) – This line is asserted by the selected controller when it is ready to execute the specified function as decoded in F(00:02).

1.7.4.1 Priority Transfer Lines – To perform priority interrupts between the KL10 and its devices, the same basic set of signals is used in a slightly modified form. Table 1-5 lists the necessary signals.

Table 1-5
Priority Transfer Signals

Name	Mnemonic	No. of Signals
Controller Sel	CS (04:06)	3
Controller Sel	CS (00:03)	4
Function	F (00:02)	3
Demand	DEM	1
Acknowledge	ACK	1
Transfer	XFER	1

Controller Select CS(04:06) – During interrupt arbitration, these three lines represent the octal encode of the interrupting channel. The range is 0 through 7.

Controller Select CS(00:03) – These four lines specify the controller or device that the EBox will honor during this interrupt sequence. This is, of course, only a single device or controller, even though several may be interrupting on the same channel. This code will also correspond to the hard-wired physical device number of the appropriate controller or device.

Function F(00:02) – Two functions are generated during the interrupt dialogue; refer to Table 1-6. The first is a code of 4 in F(00:02). It specifies to the interrupting controllers that those being addressed by channel number in CS(04:06) should send their physical controller number by placing them onto the EBus upon sensing DEMAND. The second function is a code of 5 in F(00:02). It specifies to the interrupting controllers or devices that one has been selected. The selected one will see CS(00:03) as the same number as its physical controller number.

Table 1-6
Priority Transfer Commands

F00	F01	F02	Operation
1	0	0	PI SERVED
1	0	1	PI ADDRESS IN

ACKNOWLEDGE (ACK) – Same as for data transfers.

TRANSFER (XFER) – In the case of interrupts, the device selected for service by the EBox will place a special function on the EBus data lines D(00:35). Refer to Figure 1-2, API Word Format.

The vector interrupt locations for the PDP-11 are as follows: 774, 770, 764, 760 for the first, second, third, and fourth interfaces on a single PDP-11 respectively. The high-order PDP-11 address bits are listed in Table 1-7.

**Table 1-7
PDP-11 Device Registers**

Interface	Assignment
0	774400
1	774440
2	774500
3	774540

All of the necessary registers for implementing the specified types of data or non-data transfers have been included in the interface. In general, the majority of these registers are addressable by the PDP-11 for read or for write. They are not selectable from the EBox.

1.8 INTERFACE DATA AND CONTROL BUFFERING

To facilitate efficient interprocessor data transfers, with minimum intervention by either the EBox or PDP-11 processors, a storage medium in the form of a semiconductor Random Access Memory (RAM) containing 16 words \times 16 bits per word of storage has been included as a part of the interface. The access time of the RAM is about 125 ns. The available RAM storage is sufficient to contain all of the necessary control and data words used to perform the DTE20's four major hardware operations as a free standing element. In addition, the RAM can be loaded and read under the direction of a diagnostic program resident in the PDP-11 processor and can also be used to control the DTE20 during diagnostic operations.

1.8.1 Addressable Register Summary

Table 1-8 provides a summary of all of the internal addressable locations within the DTE20. Sixteen locations are listed; twelve are RAM locations and the remaining four are register locations.

Diagnostic Word 3 – This word can be read at any time from the PDP-11 processor. It consists of interface control signals and addresses, along with the TO10 byte mode bit.

Status – This register consists of an EBox portion and a PDP-11 portion. The detailed bit assignments for both are given in Tables 1-13, 1-14, 1-15, and 1-16. Register bit assignments generally consist of Done and Error flags for the various operations, a flag for each processor to interrupt the other, and miscellaneous other flags.

NOTE

Each machine has its own separate copy of each status bit, except for the doorbells (e.g., there is a 10 TO10 Normal Termination flag and an 11 TO10 Normal Termination flag).

Diagnostic Word 2 – This word is similar to Diagnostic Word 3 in that it can be read by the PDP-11 processor at any time simply by addressing the appropriate register within the DTE20. Under diagnostic control, this word can be written to control the DTE20 minor states in a single pulse fashion. Also, because no real interrupts are sent to the EBox during diagnosis of the DTE20, a bit in this word can enable the appropriate flag to set to simulate a response from the EBox as if it responded to the interrupt. Finally, it can enable the current major state to lock out any changes in that state until such time as it is desired to do so.

The remaining registers are RAM locations and are summarized, together with the DTE programming information, in Tables 1-9 through 1-19 of this section.

**Table 1-8
Addressable Register Summary**

Register Name	Accessible By:	PDP-11 INSTR	DTE20 ADR	KL10 INSTR	FCN CODE
DIAG3	PDP-11	DATO, DATI	XXX36	—	—
STATUS	BOTH PDP-11 and KL10	DATO, DATI	XXX34	CONO, CONI	0,1
DIAG2	PDP-11	DATO, DATI	XXX32	—	—
DIAG1	PDP-11	DATO, DATI	XXX30	—	—
TO11 DATA	PDP-11	DATO, DATI	XXX26	—	—
TO10 DATA	PDP-11	DATO, DATI	XXX24	—	—
TO11 ADR	PDP-11	DATO, DATI	XXX22	—	—
TO10 ADR	PDP-11	DATO, DATI	XXX20	—	—
TO11 BYTE CNT	PDP-11	DATO, DATI	XXX16	—	—
TO10 BYTE CNT	BOTH PDP-11 and KL10	DATO, DATI	XXX14	DATAO	2
ADDRESS WORD 2	PDP-11	DATO, DATI	XXX12	—	—
ADDRESS WORD 1	PDP-11	DATO, DATI	XXX10	—	—
DATA WORD 1	PDP-11	DATO, DATI	XXX06	—	—
DATA WORD 2	PDP-11	DATO, DATI	XXX04	—	—
DATA WORD 3	PDP-11	DATO, DATI	XXX02	—	—
DELAY COUNT	PDP-11	DATO, DATI	XXX00	—	—

Table 1-9
Deposit or Examine Word Formats

Word	Bits	Function
DEXWD1	15-04	Must be zero, reserved by DEC
	03-00	KL10 data bits 0-3
DEXWD2	15-00	KL10 data bits 4-19
DEXWD3	15-00	KL10 data bits 20-35
TENAD1	15-13	Address space
	12	Deposit bit 1 = deposit 0 = examine
	11	PRTOFF if 1 protection and relocation is off for examines and deposits for a restricted mode DTE
	10-09	Must be zero, reserved by DEC
	08-07	Must be zero, reserved by DEC
	06-00	High order KL10 address bits (13-19)
TENAD2	15-00	Low order KL10 address bits (20-35)

Table 1-10
TO10 Transfer Word Format

Word	Bits	Function
DLYCNT	15-14	Unibus address bits 17-16. Specifies two high-order bits of 18 bit PDP-11 address used in 18 bit byte transfer addresses. Transfer cannot cross a 32K boundary. TO10 and TO11 transfers must be in the same 32K bank.
	13-00	<p>NEGATIVE DLY COUNT – The software specifies how many 500-nanosecond units of delay are to occur between each byte on byte transfers in either direction. The delay also applies before the first byte. During the transfer operation the DTE up counts a copy of this count in the ABC register, once each 500 nanoseconds, until bit 13 = 0.</p> <p align="center">NOTE</p> <p>The count is incremented by 1 and then the hardware tests bit 13 of ABC for = 0. Therefore both values of 17777 and 00000 are equivalent to no delay.</p>
TO10AD	15-00	Byte address of source string. This is updated by the DTE as each byte is transferred. At the end of a transfer, it points to the byte (word) which would have been transferred next from PDP-11 memory. The update is by +1 for byte mode and +2 for word mode.
TO10BC	15	If a 1, this bit interrupts both processors at the completion of the current transfer. If a 0, it interrupts the -10 only.
	14-12	Must be zero, reserved by DEC.
	11-00	Negative byte count.
TO10DT	15-08	<p>High order byte</p> <p align="center">PDP-11 byte mode: equal to 0 PDP-11 word mode: bits to become KL10 data bits 20-27</p>
	07-00	Low order byte bits to become KL10 data bits 28-25

Table 1-11
TO11 Transfer Word Format

Word	Bits	Function
DLYCNT	15-14	Same as for TO10 transfer — see Table 1-10.
	13-00	Same as for TO10 transfer — see Table 1-10.
TO11	15-00	Byte address in PDP-11 memory of where to store next byte received from EBox. This word is updated as each byte (word) is transferred. At the end of a transfer, it points to the byte (word) that would have been transferred next. The update is by +1 for byte mode and +2 for word mode.
TO11BC	15	I Bit — If 0, on normal termination interrupt only the PDP-11. If 1, on normal termination interrupt both the PDP-11 and EBox. If an error occurs, the I bit is ignored and both the PDP-11 and EBox always get an error termination interrupt.
	14	Z Stop — If 1, stop on a null character received from the EBox, after storing it in PDP-11 memory. The TO11AD is not incremented so that the next transfer can start by overwriting the null character if desired.
	13	TO11BM — If 1, set byte mode in the DTE, if 0, set word mode in the DTE for TO11 transfer.
	12	Must be zero, reserved by DEC.
	11-00	Negative byte count
TO11DT	15-08	High order byte PDP-11 byte mode: KL10 bits 28-35 or 20-27 PDP-11 word mode: KL10 bits 20-27
	07-00	Low order byte PDP-11 word mode: KL10 bits 28-35 PDP-11 byte mode: KL10 bits 20-27 or 28-35

**Table 1-12
DATAO DTE Function**

Bits	Function
0-22	Must be zero, reserved by DEC
23	TO11IB – This is the “I” bit. If 1 set TO10IB. If 0, clear TO10IB. If 1, the EBox has set the “I” bit for a TO10 byte transfer. Both the EBox and the PDP-11 will be interrupted on normal termination. If 0, the EBox has not set the “I” bit for a TO10 byte transfer. Only the EBox will be interrupted on normal termination. The EBox may then reset the TO10 byte pointer, before reloading the TO10 byte count and performing a scatter read.
24-35	Negative Byte Count – The twos complement of the number of characters left to transfer until a TO10 normal termination occurs. A -1 will transfer one character to the EBox before a normal termination. A 0 will transfer 0 bytes before a normal termination.

Table 1-13
CONI DTE Function

Bits	Function
0-19	Read as zeros
20	RM — a 1 in this bit indicates that the DTE is in restricted mode, a 0 in this bit indicates that the DTE is in privileged mode.
21	DEAD11 — a 1 in this bit indicates that the PDP-11 power is not correct (the Unibus signal “AC LOW” is asserted) and that no transfers can take place.
22	TO11DB — a 1 in this bit indicates that the EBox has requested a PDP-11 doorbell interrupt and is waiting for the PDP-11 to take some action.
23-25	Read as zeros.
26	TO10DB — a 1 in this bit indicates that the PDP-11 has requested a doorbell interrupt and is waiting for the EBox to take some action.
27	TO11ER — a 1 in this bit indicates that an error occurred during a TO11 transfer.
28	Read as zero
29	TO11DN — a 1 in this bit indicates that a TO11 transfer was completed and an error did not occur. The “I” bit had been set by the PDP-11. The transfer is completed if: <ul style="list-style-type: none"> 1. The byte count became equal to zero. or 2. The PDP-11 had set the “Z” bit and a null character was encountered.
30	TO10DN — a 1 in this bit indicates that the byte counter for the TO10 transfer became equal to zero and an error did not occur.
31	TO10ER — a 1 in this bit indicates an error (PDP-11 memory parity or Unibus timeout error, but not EBus Parity error) occurred during the TO10 transfer.
32	PIOENB — a 1 in this bit indicates that the DTE is enabled to perform examines, deposits and byte transfers at PI Level 0 by the EBox.
<p align="center">NOTE</p> <p>The DTE is automatically enabled if the PDP-11 is privileged even though this bit is 0.</p>	
33-35	The current PI channel assignment for doorbell interrupts, byte transfer normal and error terminations.

Table 1-14
CONO DTE Bit Function

Bits	Function
18-21	Must be zero, reserved by DEC.
22	TO11DB – causes a doorbell interrupt in the PDP-11, setting the 10 request interrupt flag in the DTE status register. This flag can only be cleared by the PDP-11.
23	CR11B – clears the reload PDP-11 button in the DTE.
24	SR11B – sets the reload PDP-11 button in the DTE. Setting this bit in the status register initiates the ROM bootstrap in the PDP-11.
25	Must be zero, reserved by DEC.
26	CL11PI – clear the PDP-11 requesting 10 interrupt flag in the DTE status register.
27-28	Must be zero, reserved by DEC.
29	CLTO11 – clear both the TO11 normal termination, and also the TO11 error termination flags in the DTE.
30	CLTO10 – clears both the TO10 normal termination, and the TO10 error termination flags in the DTE.
31	PILDEN – loads the PI Interrupt Channel number from bits 33-35 and PI Level 0 enabled from bit 32.
32	PIOENB – enables PI0.
33-35	PI Channel Number. Loaded if bit 31 is equal to 1.

Table 1-15
DATO DTE Status Function

Bits	Function
15	DON10S – If 1, set TO10 normal termination status (TO10DN). This bit is provided for diagnostic purposes only. Setting it via a DATO does not terminate a transfer in progress.
14	DON10C – If 1, clear TO10 normal termination status (TO10DN).
13	ERR10S – If 1, set TO10 error termination status (TO10ER). This bit is provided for diagnostic purposes only. Setting it via a DATO does not terminate a transfer in progress.
12	ERR10C – If 1, clear TO10 error termination (TO10ER).
11	INT11S – If 1, set 10 request PDP-11 interrupt (TO11DB). This results in a PDP-11 vector interrupt.
10	INT11C – If 1, clear 10 request PDP-11 interrupt (TO11DB). This enables more doorbell interrupts to the PDP-11 to occur.
09	PERCLR – If 1, clear the PDP-11 memory parity error flag (11MPE).
08	INT10S – If 1, set request 10 interrupt (TO10DB). This results in a vectored interrupt to EPT location $142 + 8 * n$.
07	DON11S – If 1, set TO11 normal termination flag (TO11DN). This bit is provided for diagnostic purposes only. Setting this bit does not terminate a transfer in progress.
06	DON11C – If 1, clear TO11 normal termination flag (TO11DN).
05	INTRON – If 1, enable DTE to generate PDP-11 BR requests. Clearing or setting this bit does not clear any interrupts waiting.
04	EBUSPC – If a 1, clear EBus parity error.
03	INTROF – If 1, disable DTE from generating PDP-11 BR requests. Clearing or setting this bit does not clear any interrupts waiting.
02	EBUSPS – If 1, set EBus parity error.
01	ERR11S – If 1, set TO11 error termination flag (TO11ER). This bit is provided for diagnostic purposes only. Setting it does not terminate a transfer in progress.
00	ERR11C – If 1, clear TO11 error termination flag (TO11ER).

Table 1-16
DATI DTE Status Function

Bits	Function
15	TO10DN — The TO10 byte count became 0 or the PDP-11 program set DON10S. TO10DN will not be set if an error termination occurred, i.e., TO10ER.
14	Read as zero, this bit is unused.
13	TO10ER — an NPR Unibus parity error (DIAG3 [NUPE]), PDP-11 memory parity (status [11MPE]), or a Unibus timeout (no bit) occurred during a TO10 byte transfer, or the PDP-11 program set the status bit (ERR10S). Status bit (TO10DN) will not be set, if an error termination occurred. Thus, PDP-11 programs must test for both TO10DN and TO10ER.
12	RAMIS0 — The data out of the RAM location is all 0s. This bit is provided on a read for diagnostic purposes only. It has no meaning and is unpredictable unless the DTE is being single stepped.
11	TO11DB — The 10 has requested (via CONO DTEN) a PDP-11 doorbell interrupt.
10	DEXWD1 — This bit is provided for diagnostic purposes only. It has no meaning and is unpredictable unless the DTE is being single stepped.
09	MPE11 — Indicates that the PDP-11 memory had a parity error during a data fetch for a TO10 byte transfer. Parity errors are detected only if the PDP-11 has the MF11UP or MP11LP memory parity option.
08	TO11DB — The PDP-11 has requested a -10 doorbell interrupt (INT10S) and the -10 has not yet cleared the bit (via CONO DTEN) using CL11PI.
07	TO11DN — The TO11 byte count became equal to 0 (TO11BC = 0), the transfer stopped on a MU11 character (status bit NULSTP = 1), or the PDP-11 program set status bit DON11S.
06	EBSEL — E Buffer Select. This bit is provided for diagnostic purposes only. It has no meaning and is unpredictable unless the DTE20 is being single stepped.
05	NULSTP — Null Stop. The TO11 transfer stopped because the stop bit was set (TO11BC [Z Stop]) = 1.
04	B PAR ER — EBus Parity Error. The DTE detected an EBus parity error during a TO11 byte transfer or examine transfer.
03	RM — If 1, the attached PDP-11 is in restricted mode. If 0, the attached PDP-11 is in privileged mode. The value of this bit is determined by the setting of the privileged switch on the DTE20.
02	DEXON — The last deposit or examine operation has been completed. No interrupt occurs. The PDP-11 must watch for this bit to be set after every deposit or examine. The DTE20 clears status bit DEXON whenever a deposit or examine is started (by loading TENAD2).
01	TO11ER — an error occurred during a TO11 byte transfer or the PDP-11 program sets the status bit ERR11S. Status bit TO11DN will not be set if an error termination occurred. Thus, programs must test for both TO11DN and TO11ER.
00	INTSON — Interrupts on. If 1, the DTE is enabled for PDP-11 BR requests. If 0, it is disabled (INTRON enables, INTROF disables).

Table 1-17
DATI/DATO DTE DIAG Word 1

Bits	Function	
	DS REMOVE STATUS FALSE and all DS bits = 0 (Any DS bits = 1 are considered illegal)	DS REMOVE STATUS TRUE
	Receive processor status bits.	Observe up to 128 DS bits asserted by the DTE.
15-12	Unused	
		NOTE
11	DS04-1 = KL Clock Error Stop. The KL10 internal clock (32 MHz) has frozen due to a hardware malfunction of one of the following: CRAM, DRAM, Fast Memory Parity Error, or Field Service test condition.	Unless the DS Bits are asserted without DCOMST (Diagnostic Command Start), this will always read as zeros because DCOMST clears the register at the end of a diagnostic cycle.
10	DS05-1 = RUN (1). The microcode examines this flag between functions. The microcode enters a Halt Loop if this flag is off. This flag is under control of the PDP-11, using two diagnostic functions. The KL10 cannot affect RUN.	
09	DS06-1 = HALT (1). This signal is set when the microcode enters the Halt Loop and clears the Signal when it leaves the Loop.	
08	DEX – Deposit or Examine major state. WRITE: Must be zero. READ: A 1, indicates interface major state is deposit or examine.	
07	TO10 – READ: a 1, indicates interface major state is TO10 transfer. 0 indicates not in TO10 transfer state. DFUNC (Remove Status) – WRITE: A 1, causes the EBox to stop sending basic status on the DS lines, so that a loopback test can be performed on the DS lines or a DIAG FUNC can be sent to the EBox via the DS lines. If any of the DS lines are set (by the DTE) the result is an “OR” of the bits set in the DTE and EBox status.	
06	TO11 – READ: A 1 means interface major state is TO11 transfer. WRITE: Must be zero.	
05	D1011 – Diagnose 10/11 interface. READ: If a 1, the DTE is in 10/11 diagnostic mode, i.e., it will diagnose itself. If a 0, it is not in 10/11 diagnostic mode. WRITE: If a 1, set DTE to 10/11 diagnostic mode. This mode is used to diagnose the DTE itself. If a 0, leave 10/11 diagnostic mode.	

Table 1-17 (Cont)
DATI/DATO DTE DIAG Word 1

Bits	Function
04	<p>VEC04 – Vector Interrupt Address bit 4:</p> <p>READ: Vector interrupt address bit 4</p> <p>PULSE-WRITE: If a 1, generate a single clock cycle. If 10/11 diagnostic mode (D1011 status bit) is also set.</p>
03	<p>DIKL10 – READ: This bit is read as zero.</p> <p>WRITE: If a 1, and the DTE is in privileged mode, put the DTE into KL10 diagnostic data transfer mode. Subsequent deposits and examines become diagnostic functions instead of accessing KL10 memory. If a 0, put the DTE in normal data transfer mode.</p>
02	<p>DSEND – READ: This bit is read as zero.</p> <p>WRITE: If a 1, send data (TO10) during a diagnostic bus transfer. If a 0, receive data (TO11) during a diagnostic bus transfer.</p>
01	<p>This bit is unused and must be zero on a write. It is read as zero.</p>
00	<p>DCOMST – Diagnostic command start.</p> <p>READ: If a 1, a diagnostic command is in progress.</p> <p>WRITE: If a 1, and the DTE is switched to privileged mode, diagnostic command start is set. If a 0, diagnostic command start is cleared.</p>

Table 1-18
DATI/DATO DIAG Word 2

Bits	Function
15	RFMAD0 – RAM File Mixer Address 0. READ: The contents of RFM address 0. WRITE: Must be zero.
14	RFMAD1 – RAM File Mixer Address 1. READ: The contents of RFM Address 1. EDONES – WRITE: If a 1, set EBus done. If a 0, clear EBus done.
13	RFMAD2 – RAM File Mixer Address 2. READ: The contents of RFM Address 2. WRITE: Must be zero.
12	RFMADR3 – RAM File Mixer Address 3. READ: The contents of RFM address 3. WRITE: Must be zero.
11-07	Unused – READ: Read as zeros. WRITE: Must be zero.
06	DRESET – DTE Reset. READ: Read as zero. WRITE: If a 1, reset the DTE.
05	Unused – READ: Read as zero. WRITE: Must be zero.
04-01	READ: Read as zeros. WRITE: Loads 04, 03, 02, 01 into minor state counter 8, 4, 2, 1 for diagnostic use only. (During normal operation must be zero.)
00	Unused – READ: Read as zero. WRITE: Must be zero.

Table 1-19
DATI/DATO DIAG Word 3

Bits	Function																		
15	<p>SWSLLT – Swap Select Left</p> <p>READ: CNT1 [N] Swap Select LT.</p> <p>WRITE: Must be zero.</p>																		
14	<p>DPS4 [N] Parity (1) H</p> <p>READ: DPS4 [N] Parity flop is on a one. Diagnostic use only.</p> <p>WRITE: Must be zero.</p>																		
13-08	<p>Captured Unibus Parity Error Information.</p> <p>READ: Ann indicates Unibus register address bit, Dnn indicates Unibus data bit, when a Unibus parity error is detected.</p> <table> <tr> <td>TIME</td><td>UNIBUS DATA BITS</td></tr> <tr> <td>Initially</td><td>D15 D14 D13 D12 D11 A00</td></tr> <tr> <td>1st Shift</td><td>D10 D09 D08 D07 D06 A00</td></tr> <tr> <td>2nd Shift</td><td>D05 D04 D03 D02 D01 A00</td></tr> <tr> <td>3rd Shift</td><td>D00 A04 A03 A02 A01 A00</td></tr> <tr> <td>4th Shift</td><td>D15 D14 D13 D12 D11 A00</td></tr> <tr> <td>.</td><td>.</td></tr> <tr> <td>.</td><td>.</td></tr> <tr> <td>.</td><td>.</td></tr> </table> <p>WRITE: Must be zero.</p>	TIME	UNIBUS DATA BITS	Initially	D15 D14 D13 D12 D11 A00	1st Shift	D10 D09 D08 D07 D06 A00	2nd Shift	D05 D04 D03 D02 D01 A00	3rd Shift	D00 A04 A03 A02 A01 A00	4th Shift	D15 D14 D13 D12 D11 A00
TIME	UNIBUS DATA BITS																		
Initially	D15 D14 D13 D12 D11 A00																		
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2nd Shift	D05 D04 D03 D02 D01 A00																		
3rd Shift	D00 A04 A03 A02 A01 A00																		
4th Shift	D15 D14 D13 D12 D11 A00																		
.	.																		
.	.																		
.	.																		
07-06	<p>Unused</p> <p>READ: Read as zeros.</p> <p>WRITE: Must be zeros.</p>																		
04	<p>DUPE – DATO Unibus Parity Error .</p> <p>READ: If 1, a DATO Unibus parity error has been detected by the DTE.</p> <p>CDD – Clear DUPE and DURE error flags.</p>																		

Table 1-19 (Cont)
DATI/DATO DIAG Word 3

Bits	Function
03	<p>WEP – Write even (bad) parity.</p> <p>READ: Read the status of the write even Unibus parity flip-flop.</p> <p>WRITE: If a 1, write even Unibus parity. Results in DTE generating even (bad) parity on all Unibus transfers which have parity. If a 0, the DTE will generate odd (good) parity on all subsequent Unibus transfers which have parity. This bit is provided for diagnostic purposes to check the parity networks.</p>
02	<p>DURE – DATO Unibus receive error.</p> <p>READ: A Unibus receiver error has occurred.</p> <p>WRITE: Must be zero.</p>
01	<p>NUPE – NPR Unibus parity error.</p> <p>READ: If a 1, a Unibus parity error has occurred on an NPR (byte) transfer.</p> <p>CNUPE – WRITE: Clear NUPE.</p>
00	<p>TO10BM – TO10 byte mode.</p> <p>READ: Read as zero.</p> <p>WRITE: If a 1, TO10 byte transfers are to be performed in byte mode from the PDP-11 memory. If a 0, TO10 byte transfers are to be done in word mode from PDP-11 memory.</p>

1.9 BUS OPERATION

Functionally, the DTE20 operates in two ways. One way is an operation that fetches data; the other is an operation where the data must be loaded by an operating program. In the first method, a single bus operation may access the interface from the PDP-11 to read or write data (or control information) into the interface RAM file. This is done by using DATI and DATO instructions and involves the Unibus. This type of operation activates the Interface Control Logic long enough for the RAM access. No dialogue, other than the normal dialogue that would take place between the PDP-11 and any standard peripheral device, i.e., MSYN, SSYN, etc., occurs. Similarly, the PDP-11 can read or write status information to or from the interface using this same mode of operation. In the second method, the interface detects the loading of control information from the PDP-11, or from both the PDP-11 and KL10 processors, and begins processing this information. The interface initiates an internal timing sequence that includes the necessary interprocessor dialogue. The result of this operation is to transfer information between the two processors using both the EBus and the Unibus, where the direction of transfer is a function of the operation being performed.

The DTE20 performs four basic hardware operations:

- DEX (Deposit or Examine)
- TO11 Transfer/TO10 Transfer
- Interprocessor Doorbell.
- Diagnostic Functions

Multiple transfers take place for both TO11 and TO10 transfers; however, the source and destination differ. In the TO11 transfer, the source of the data is the KL10 memory and the destination is the PDP-11 memory. The situation is reversed for TO10 transfers: the source is the PDP-11 memory and the destination is the KL10 memory.

The DEX (Deposit or Examine) operation differs from a TO10 or TO11 transfer operation by the fact that a single transfer occurs. Also, no interrupt is generated to the PDP-11 upon completion of the operation.

The interprocessor doorbell is unique in that it uses only the "peripheral bus control logic" (i.e., the BR Control and the EBus Dialogue Logic) and does not initiate the internal time state logic.

Data entering the DTE20 on the EBox side does so in 36-bit words, which are converted into 16-bit words within the interface and stored in the RAM FILE. From there, the buffered data word can be transmitted to the PDP-11 under control of the Interface Control Logic by the NPR facility. Data entering the DTE20 on the PDP-11 side does so in 16-bit words that are stored in the RAM FILE. From there, the buffered word can be transmitted to the EBox under the control of the Interface Control Logic, using the interrupt control and the EBox side interrupt logic. This transfer also involves the E-Buffer register.

Two basic classes of transfers can be performed in terms of implementation. Table 1-8 contains a list of PDP-11 addresses given to select the appropriate RAM address within the interface, the functional name for that particular RAM slot, and a description of that slot's usage during the appropriate interface operations.

The first class is Deposit and Examine and deals with an address in KL10 memory and a data word that is either sent or received to or from KL10 memory as specified by the address word. These two operations involve five temporary RAM storage slots for address and data.

The second class is TO11 transfer, or TO10 transfer, and deals with a Delay Count word, a Byte Count word, an address word, and a data word. All of these words must have storage space in the RAM FILE. Before transfers for either class of operation begin, the necessary words that control the particular transfer must be supplied, by the processor, to the RAM FILE.

Refer to Figures 2-1 and 2-2. The PDP-11 can read or write all RAM locations and also the Diagnostic and Status registers via the Unibus. These registers have internal addresses (shown in brackets []); for example the Status register is address [16]. To set up a transfer within the interface, the PDP-11 performs DATO instructions while addressing the appropriate RAM locations. The EBox cannot address any of the RAM locations and, in fact, is only required to supply one piece of control information. This is the TO10 Byte Count word, necessary in the TO10 transfer operation. It is supplied by performing a DATAO DTE X instruction in the EBox. The TO10 Byte Count word will be placed into a temporary Buffer register, E B HOLD, where it will reside until the Interface Control Logic can store it in its slot in the RAM FILE. The Status register contains bits that allow both processors to communicate. This is necessary to negotiate transfers. The feature is referred to as "the interprocessor doorbell," and is implemented via the appropriate interrupt logic, with the interrupt control and the Status register.

To summarize, both processors communicate and negotiate the particular operation to take place. Next, the appropriate RAM slots are loaded by the PDP-11 or EBox accordingly and the interface, using detection logic in the data control, starts up the interface via the Interface Control Logic. At this time, the interface contains all the necessary information in order to complete the specified transfer or transfers, including the ability to use either interrupt facility as necessary.

1.10 PROGRAMMING EXAMPLES

Generally, the PDP-11 program sets up the interface by reading status conditions and loading control parameters, and by performing the appropriate sequence of instructions.

The format is:

INSTR ADR1, ADR2

where ADR1 is the symbolic address of a particular PDP-11 general purpose register (one of eight) within the processor (R0-R7).

ADR2 is the symbolic address of the memory location or device being addressed by this instruction. For example:

MOV DLYCNT, @ RAM0.

In this example, the MOV instruction moves the word in symbolic location DLYCNT into the location addressed by the number in symbolic location RAM0. The @ symbol indicates indirect addressing.

If the contents of RAM0 is the appropriate DTE20 address for the Delay Count word, i.e., XXXX00, then the value in DLYCNT will be moved (loaded) into the DTE20 delay count slot in the RAM (Figure 1-10).

The interprocessor doorbell feature will allow the PDP-11 and KL10 processors to talk to each other via the DTE20 interrupt facilities. To interrupt the EBox, the PDP-11 performs the following:

MOV INT10S,@ STATUS; Ring the KL10 doorbell.

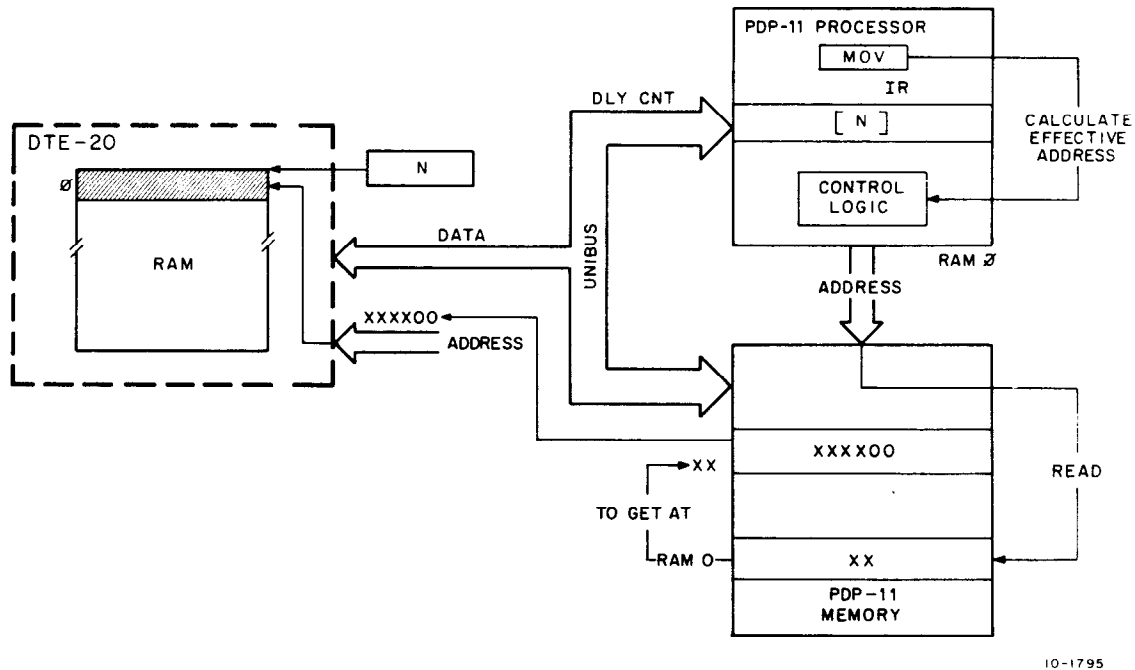


Figure 1-10 Load DLY Count

Assume location Instruction +2 contains a single one in bit position 08; this is necessary in order to set the flag in the DTE20 that causes a programmed interrupt to the EBox. Also, assume location Status contains the address of the Status register in the DTE20, XXXX34. The execution of the MOV instruction by the PDP-11 processor causes the appropriate flag in the interface to set. This action initiates a programmed interrupt to the EBox (Figure 1-11).

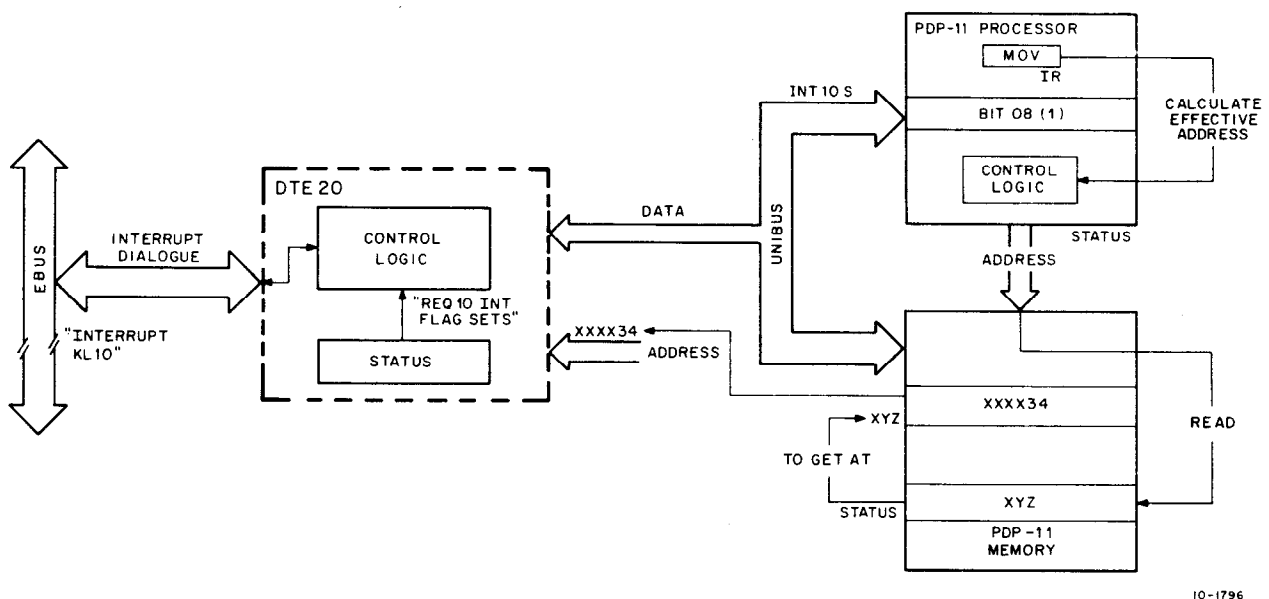
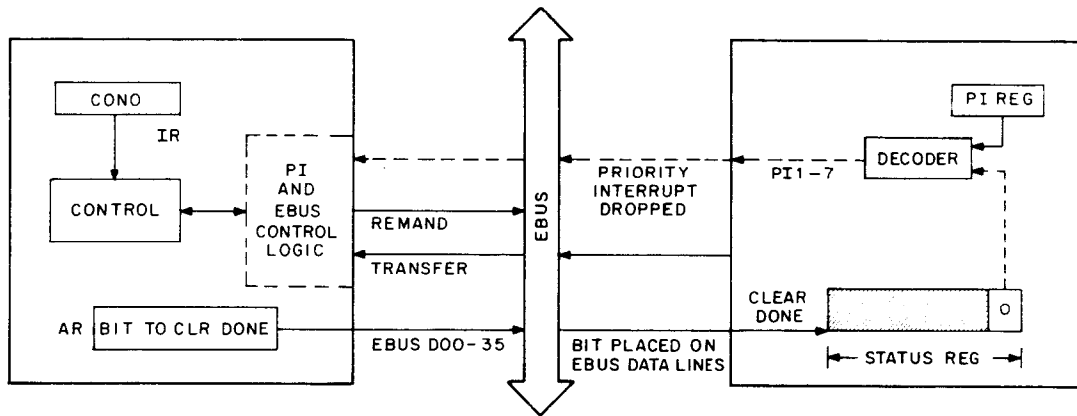


Figure 1-11 Ring KL10 Doorbell



10-1798

Figure 1-13 CONO Simplified

